

0.18- μm Light-Harvesting Battery-Assisted Charger–Supply CMOS System

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Abstract—Wireless microsensors in hospitals, factories, and farms can manage and save lives and resources. Although tiny batteries cannot sustain them for long, harvesters can because ambient energy is abundant. Photovoltaic cells are popular in this regard because they output close to $100\times$ more power from solar light than piezoelectric, electrostatic, and thermoelectric generators can from motion and heat. But since mm cells can only supply μW 's of the mW 's that microsystems can draw, and light is not always available, battery assistance is necessary. So to supply functions and sustain operation across extended periods, the system should extract maximum ambient power, draw minimal battery assistance, and deliver as much power as possible. The 0.18- μm CMOS harvester presented here does this, draws $10\text{--}100\ \mu\text{W}$ from a $3 \times 3 \times 1\text{-mm}^3$ cell and assistance from a battery to supply a 1-mW load and recharge the battery with excess cell power. The switched-inductor charger–supply regulates 1-V within $\pm 25\ \text{mV}$ with $73\%\text{--}86\%$ power-conversion efficiency and keeps the cell within 1% of its maximum power point. This way, the cell outputs $100\ \mu\text{W}/\text{mm}^2$ from solar light and $1\ \mu\text{W}/\text{mm}^2$ from direct indoor light.

Index Terms— Ambient light energy, harvester, CMOS photovoltaic (PV) cells, microsystem, switched-inductor converter, wireless microsensor, charger, and power supply.

I. PHOTOVOLTAIC MICROSYSTEMS

Wireless microsensors in humans, hospitals, homes, and factories can monitor, process, and report information [1]–[2] that can save lives, energy, and money. Unfortunately, tiny on-board batteries cannot supply power for long, and recharging or replacing thousands of batteries or nodes in difficult-to-reach places and across wide networks is oftentimes impracticable. The environment, however, offers plenty of ambient energy in light, motion, heat, radiation, and other forms that transducers can harness to energize microsystems [3]–[5].

Photovoltaic (PV) cells, for example, can generate $15\text{-mW}/\text{cm}^2$ from solar light, which is orders of magnitude higher than what piezoelectric, electrostatic, electromagnetic, and thermoelectric generators can from motion, radiation, and heat [6]–[7]. Unfortunately, sunlight is not always available, and indoor lighting is a poor substitute. Plus, millimeter cells only capture a small fraction of the incoming light. So the only way the intermittent microwatts that small PV cells generate can sustain a wireless transmitter, for example, which draws

milliwatts at a time, is with assistance from an on-board battery like Fig. 1 shows.

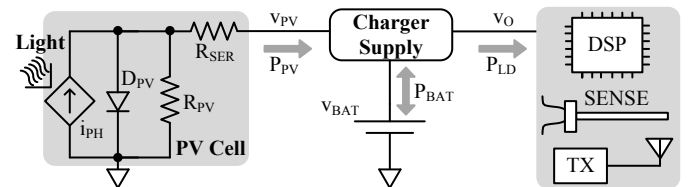


Fig. 1. Battery-assisted energy-harvesting photovoltaic microsystem.

Since small sensors can idle between sensing and transmission events, they can, between these times, consume nanowatts [1], [2], and [8] of the microwatts that PV cells supply. A wireless microsystem can therefore replenish its battery V_{BAT} with excess PV power between heavily loaded periods. So if loading events are sufficiently sparse and short term, V_{BAT} can charge long enough to help the system supply high-power loads.

For maximum functionality and life, the system should draw maximum power from the PV cell [9]. And for maximum integration, the battery should be small, so the system should require little battery assistance. The charger–supply should also deliver as much power as possible. In this context, Sections II and III explain how the controller switches the power stage to draw and deliver power from the PV cell and the battery to supply the load, and when possible, to charge the battery. Sections IV and V describe how the system draws maximum photovoltaic power, regulates the output, and supplies the load. Sections VI and VII discuss how the prototyped system performs and compares against the state of the art, drawing conclusions in Section VIII.

II. CHARGER–SUPPLY SYSTEM

Although PV cells can stack to produce higher voltages, stacked cells that share the same silicon CMOS substrate leak substantial power [8], [10], and [11]. So when confined to the same area, one cell produces more power than several in series. This is why one $0.27\text{--}0.32\text{-V}$ PV cell feeds the system in Fig. 1. A $1.4\text{--}1.8\text{-V}$ super capacitor can fill the role of the battery because $0.18\text{-}\mu\text{m}$ devices often break at $1.8\ \text{V}$. And although loads can sustain a range of supply voltages, $1\ \text{V}$ is a practical example because, while keeping power consumption low, $1\ \text{V}$ can still accommodate many power-consuming circuits [2]. The power stage should therefore be able to boost $0.27\text{--}0.32\ \text{V}$ to $1\ \text{V}$ and $1.4\text{--}1.8\ \text{V}$ and buck $1.4\text{--}1.8\ \text{V}$ to $1\ \text{V}$.

To deliver as much of the power it receives as possible, the power stage must itself consume little power. Switched inductors are usually more efficient in this respect than

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switched capacitors. This is because, for the same voltage conversion, switched capacitors normally employ more switches that require gate-drive energy [7], [11]. Linear regulators lose even more power because they can drop 200–300 mV, whereas switches can drop less than 10–50 mV. Plus, linear regulators cannot boost. So for functionality and maximum efficiency, a switched inductor implements the charger–supply function in Fig. 1. But since power inductors are bulky, the power stage in Fig. 2, like in [12]–[15], relies on only one.

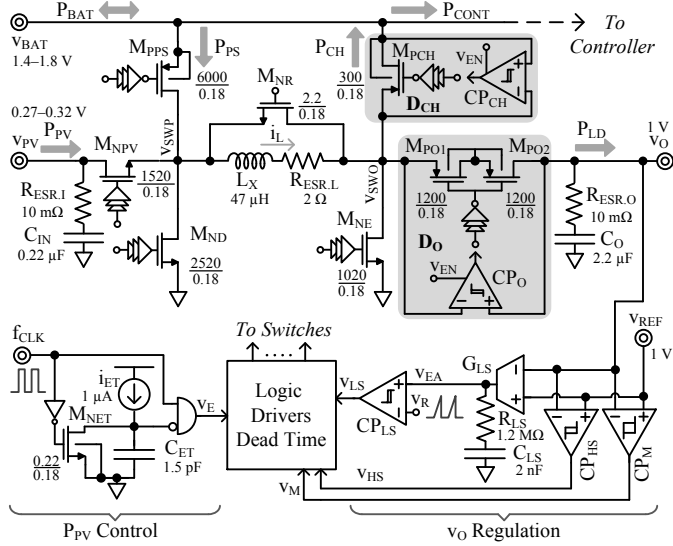


Fig. 2. Battery-assisted photovoltaic charger–supply system.

The purpose of the controller in the bottom of Fig. 2 is to determine and establish the switching sequence described later in Section III. For this, it performs two basic functions. One is to set how much power the system should draw from the photovoltaic cell and the other is to keep the output voltage near its 1-V target across loads and operating conditions. From this, it determines which switching sequence to activate, which digital logic and gate drivers then implement. Other than that, embedded dead-time logic keeps adjacent power switches from conducting simultaneously, which would otherwise short v_{PV} to v_{BAT} or v_{BAT} to v_O and therefore overload v_{PV} or v_{BAT} . And since v_{PV} is less than 0.4 V, v_{BAT} supplies all internal components.

III. POWER STAGE

A. Power Flow

When heavily sourced, the PV cell v_{PV} generates enough power P_{PV} to supply the load at v_O with P_{LD} and charge the battery v_{BAT} with P_{CH} . Since P_{PV} is insufficient when lightly sourced, however, v_{BAT} supplies the deficiency to v_O with P_{PS} . Through all this, the controller draws power P_{CONT} from v_{BAT} . So, v_{PV} is a source, v_{BAT} is sometimes a source and sometimes a load, and the controller and the output are both loads.

B. Conduction Mode

To transfer energy, the switched inductor L_X energizes and drains from a source to an output in alternate phases of a switching cycle. Since power levels in microsystems are

generally low, L_X 's dc current I_L is low. So to keep L_X conducting a low dc current continuously without ever discharging its output with negative current, the system must switch L_X fast enough to keep L_X 's current ripple Δi_L low. The challenge with this is gate-drive losses from frequent cycles can pull substantial power from v_{BAT} with respect to the load P_{LD} . This means, power-conversion efficiency is low.

Alternatively, L_X can draw and deliver larger, but infrequent energy packets in discontinuous-conduction mode (DCM). This way, L_X energizes to a high peak current $i_{L(PK)}$ and drains to zero, and to keep L_X 's average current low, L_X idles across extended periods. So in the case of the charger–supply in Fig. 2, the switches configure L_X to draw and deliver infrequent energy packets from v_{PV} or v_{BAT} to v_O or v_{BAT} , depending on P_{PV} 's reach. Table I and the following subsections describe how the switches connect across modes to achieve this functionality.

To shut L_X , all transistors near v_{SWO} open. But before that, v_{SWO} is near v_O or v_{BAT} . So when the switches open, v_{SWO} 's parasitic capacitance C_{SWO} holds energy. L_X and C_{SWO} therefore exchange this residual energy until conduction losses exhaust it. To shorten and suppress the ringing effect that this energy has on v_{SWO} , M_{NR} (like in [13]) closes when L_X finishes delivering its last energy packet. Opening all other switches and closing both M_{NE} and M_{ND} similarly suppresses these oscillations, except switching so many large power transistors requires much more gate-drive energy than M_{NR} does because M_{NR} is much smaller. Unsuppressed, these oscillations produce noise that the controller could misinterpret to inadvertently transition the switching network into an undesired state.

Since all NMOS transistors sit directly on the substrate, their bulks connect to ground, which is the most negative potential in the system. To keep M_{PPS} 's and M_{PCH} 's body diodes off, their bulks connect to the highest potential, v_{BAT} . But since the switch that M_{PO1} and M_{PO2} implement connects to v_O 's 1 V, connecting the bulk to v_{BAT} 's 1.4–1.8 V reduces their gate drive to such an extent that switch-on resistance becomes excessive. This is why M_{PO1} and M_{PO2} connect in series as one switch, to block each other's body diodes without sacrificing gate drive. With their bulks tied to their intermediate node, M_{PO2} 's body diode blocks M_{PO1} 's when v_{SWO} swings above v_O and M_{PO1} 's blocks M_{PO2} 's when v_{SWO} swings below v_O .

TABLE I. SWITCHING STATES

Switching States	M_{NPV}	M_{NE}	$M_{PO1,2}$	M_{PCH}	M_{PPS}	M_{ND}
v_{PV} energizes L_X to ground	On	On	Off	Off	Off	Off
L_X drains from v_{PV} to v_O	On	Off	On	Off	Off	Off
L_X drains from v_{PV} to v_{BAT}	On	Off	Off	On	Off	Off
v_{BAT} energizes L_X to v_O	Off	Off	On	Off	On	Off
L_X drains from ground to v_O	Off	Off	On	Off	Off	On

C. Lightly Sourced

When the PV cell's power P_{PV} is not enough to supply the load P_{LD} , v_{BAT} supplies the difference. But first, L_X delivers P_{PV} to v_O in the form of one energy packet E_{PV} per clock cycle t_{CLK} . For this, switches M_{NPV} and M_{NE} in Fig. 2 energize L_X across t_{PE} in Fig. 3. M_{NPV} , M_{PO1} , and M_{PO2} then drain L_X

from v_{PV} to v_O . This way, L_X 's i_L rises to 5 mA and falls to zero to deliver 40 μW across 25 μs to v_O .

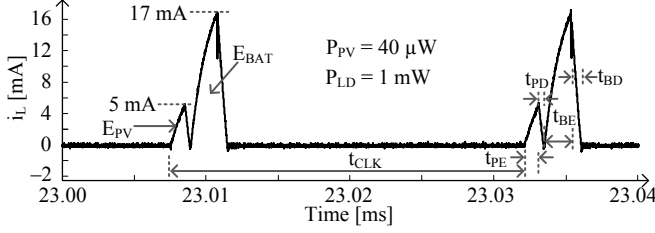


Fig. 3. Measured inductor current when lightly sourced.

To assist the PV cell, the system draws an energy packet E_{BAT} from v_{BAT} . So similarly, M_{PPS} , M_{PO1} , and M_{PO2} energize L_X from v_{BAT} to v_O and M_{NDE} , M_{PO1} , and M_{PO2} then drain L_X into v_O . So i_L rises to 17 mA across t_{BE} in Fig. 3 and falls to zero to deliver the remaining 960 μW to the load.

D. Heavily Sourced

When PV power P_{PV} exceeds load power P_{LD} , the system delivers surplus power to the battery v_{BAT} . But first, L_X satisfies the load. So M_{NPV} and M_{NE} energize L_X from v_{PV} and M_{NPV} , M_{PO1} , and M_{PO2} drain L_X from v_{PV} to v_O once per cycle for several cycles, as Fig. 4 shows. After L_X satisfies the load, M_{NPV} and M_{NE} continue to energize L_X from v_{PV} , but now M_{NPV} and M_{PCH} direct L_X 's energy packets to v_{BAT} until the load again requires energy.

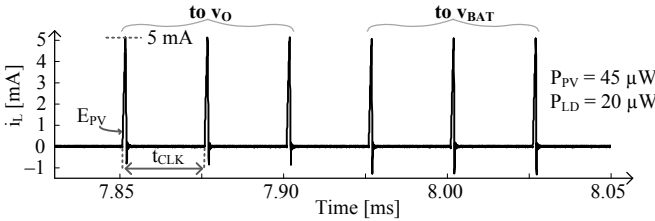


Fig. 4. Measured inductor current when heavily sourced.

E. Switch Dimensions

The underlying mechanism that dictates the dimensions of MOS switches in the power stage is power consumption. On resistance R_{ON} and gate capacitance C_G are important in this respect because R_{ON} dissipates ohmic power P_R and C_G requires gate-drive power P_G to toggle a transistor between switching states [7], [8]. So since R_{ON} and C_G both climb with increasing channel length L , all channel lengths in Fig. 2 are the shortest allowable length, 180 nm.

R_{ON} falls and C_G rises with wider channels. Channel width W should therefore be wide, but not beyond the point that the rise in P_G cancels the fall in P_R . With this guide, 1520 μm for M_{NPV} and 1020 μm for M_{NE} in Fig. 2 balance the ohmic and gate-drive losses that carrying fixed energy packets from the PV cell induces when generating 100 μW . 6000 μm for M_{PPS} and 2520 μm for M_{ND} similarly balance their losses when they transfer energy packets from v_{BAT} that help sustain half the full-range 1-mW load when PV power is 100 μW .

To keep L_X 's current i_L from reversing direction, de-energizing transistors M_{PCH} , M_{PO1} , and M_{PO2} should open when i_L just reaches zero, which is when L_X finishes draining. So when the voltage across M_{PCH} and M_{PO1} – M_{PO2} falls to nearly zero, comparators CP_{CH} and CP_O open M_{PCH} , M_{PO1} , and

M_{PO2} . In this case, 300 μm for M_{PCH} and 1200 μm for M_{PO1} and M_{PO2} ensure their nonzero voltages are high enough for CP_{BAT} and CP_O to perceive.

IV. PHOTOVOLTAIC POWER

A. Maximum Power Point

A PV cell is fundamentally a PN-junction diode D_{PV} that generates photon current (i_{PH} in Fig. 1) when light energy liberates electron–hole pairs and the built-in potential across the junction pulls the pairs apart to opposing terminals [8]. As the voltage across the cell climbs, i_{PH} delivers more photon power P_{PH} . But with a higher voltage, D_{PV} also sinks more power to ground. So v_{PV} should be high, but not beyond the point that the rise in D_{PV} 's power cancels the rise in P_{PH} . In other words, the cell outputs maximum PV power P_{PV} under a given light intensity at one particular v_{PV} setting, and any deviation from this maximum power point $v_{PV(MPP)}$ reduces P_{PV} from its maximum possible value $P_{PV(MPP)}$. In the case of the PV cell tested and shown in Fig. 5, output power when exposed to solar light can reach 100 $\mu\text{W}/\text{mm}^2$ at 0.32 V, at the maximum power point $v_{PV(MPP)}$ and $P_{PV(MPP)}$. And when exposed to an indoor source that is 2 m away, the cell can output no more than 1 $\mu\text{W}/\text{mm}^2$.

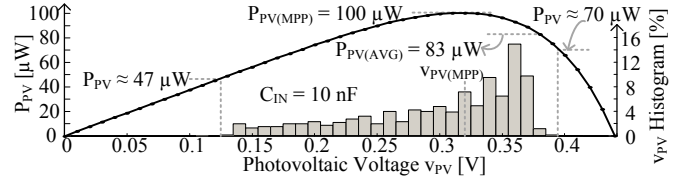


Fig. 5. Power profile and voltage histogram of the photovoltaic cell.

B. Control

The energy packet that the system in Fig. 2 draws from the PV cell v_{PV} and its frequency set how much power the cell delivers with P_{PV} . Here, a clock f_{CLK} sets the frequency and a bias current i_{ET} into a capacitor C_{ET} sets the time t_{PE} across which L_X energizes from v_{PV} . With the energizing time set, L_X 's i_L rises and peaks to $i_{L(PK)}$:

$$i_{L(PK)} = t_{PE} \left(\frac{v_L}{L_X} \right) = t_{PE} \left(\frac{v_{PV}}{L_X} \right), \quad (1)$$

where L_X 's voltage v_L across t_{PE} is v_{PV} . So fixing t_{PE} sets L_X 's energy E_L to $0.5L_X i_{L(PK)}^2$.

In this case, i_{ET} and C_{ET} fix t_{PE} to 1 μs . For this, f_{CLK} 's short pulse prompts M_{NET} to discharge C_{ET} , whose low voltage impels the AND gate to trip v_E high, and with it, start t_{PE} . i_{ET} then charges C_{ET} , and when C_{ET} 's voltage surpasses the threshold voltage of the AND gate, v_E falls to end t_{PE} . This way, v_{PV} delivers energy E_L to L_X that later reaches v_O . But since L_X drains from v_{PV} to v_O , v_{PV} also sends energy during the de-energizing period t_{PD} . To determine how much v_{PV} delivers to v_O , first consider that, for L_X to exhaust $i_{L(PK)}$ from v_{PV} to v_O , t_{PD} must be

$$t_{PD} = i_{L(PK)} \left(\frac{L_X}{v_L} \right) = i_{L(PK)} \left(\frac{L_X}{v_O - v_{PV}} \right). \quad (2)$$

And across t_{PD} , v_{PV} delivers $0.5t_{PD}i_{L(PK)}$ charge q_D , so E_D is $q_D v_{PV}$ and P_{PV} is what E_L and E_D produce across t_{CLK} :

$$P_{PV} = \frac{E_L + E_D}{t_{CLK}} = \frac{0.5L_X i_{L(PK)}^2 + (0.5t_{PD} i_{L(PK)}) v_{PV}}{t_{CLK}}. \quad (3)$$

Ultimately, fixing t_{PE} establishes $i_{L(PK)}$, E_L , and E_D and adjusting the clock frequency f_{CLK} sets P_{PV} . In the case of Fig. 2, i_{ET} is a pre-determined value that sets how much energy L_X delivers per cycle and f_{CLK} is off chip and manually adjustable so that incrementing f_{CLK} until P_{PV} peaks tunes v_{PV} to $v_{PV(MPP)}$, to the maximum power point $P_{PV(MPP)}$. Tuned this way when i_{ET} is 1.0 μA , t_{PE} in Fig. 3 is 1 μs and i_L rises to 5 mA, so P_{PV} is 40 μW when f_{CLK} is 40 kHz.

C. Output Power

Since L_X is not always connected to v_{PV} , i_{PV} charges the cell's capacitance when disconnected from L_X and i_L discharges it when connected to L_X . Unfortunately, the resulting variation in v_{PV} from Fig. 6 reduces P_{PV} . The purpose of C_{IN} in Fig. 2 is to reduce this ripple, to keep v_{PV} near its optimal MPP setting. For this, C_{IN} captures and supplies what L_X and v_{PV} do not. Since L_X conducts for a small fraction of t_{CLK} to sustain P_{PV} , and i_L is therefore much higher than i_{PV} across this time, C_{IN} supplies most of i_L 's charge q_L . So to limit the input ripple to Δv_{PV} , C_{IN} should be roughly

$$C_{IN} = \frac{\Delta q_C}{\Delta v_{PV}} \approx \frac{\Delta q_L}{\Delta v_{PV}} = \frac{0.5v_{LE} t_{PE}^2 + 0.5v_{LD} t_{PD}^2}{\Delta v_{PV} L_X}, \quad (4)$$

where v_{LE} and v_{LD} are L_X 's energizing and drain voltages v_{PV} and $v_O - v_{PV}$.

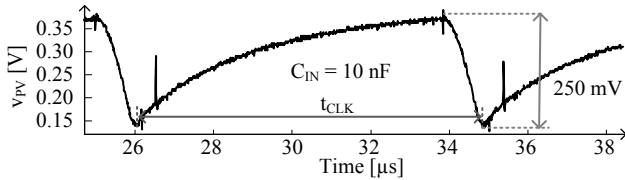


Fig. 6. Measured photovoltaic voltage.

To keep the PV cell at its maximum power point $P_{PV(MPP)}$, v_{PV} should be steady at 0.32 V, which only happens when output current i_{PV} is 312 μA . But since L_X is not always connected to v_{PV} , i_{PV} is not steady. The input capacitor C_{IN} can absorb and output the difference; but still, C_{IN} cannot keep v_{PV} from altogether changing. This means, the cell, on average, outputs less power than $P_{PV(MPP)}$. With 10 nF, for example, v_{PV} in Figs. 5 and 6 ripples between 0.13 and 0.39 V. v_{PV} dips to 0.13 V when the system draws an energy packet from v_{PV} , and since D_{PV} leaks exponentially less current at lower voltages, C_{IN} charges more quickly when v_{PV} is lower. v_{PV} is therefore more often near its peak than its valley, and v_{PV} averages to 0.3 V and PV power to 83 μW , which is less than $P_{PV(MPP)}$'s 100 μW .

Not surprisingly, higher input capacitances suppress v_{PV} 's ripple Δv_{PV} in Fig. 7, from 548 mV with the 10 pF that a probe adds to the board to 6 mV when C_{IN} is 1 μF . Above 100 nF, variations in the maximum possible average power are minimal because P_{PV} in Fig. 5 is less sensitive to small v_{PV} fluctuations near its maximum power point $P_{PV(MPP)}$. So with 220 nF, which produces ± 16 mV ripple, PV power is 99% of

$P_{PV(MPP)}$, and marginally higher with higher C_{IN} values. Below 100 nF, P_{PV} is more sensitive. Plus, the system lengthens t_{CLK} when drawing less PV power, so C_{IN} 's ripple grows quickly with lower P_{PV} . As a result, $P_{PV(AVG)}$ drops 60 μW when C_{IN} falls to 1 nF. Interestingly, variations are less severe below 1 nF. This is because the cell's inherent capacitance C_{PV} begins to dominate and saturate the effects of C_{IN} . Generally, the PV cell outputs more power when C_{IN} is higher, but since larger C_{IN} 's occupy more board space and P_{PV} is less sensitive to C_{IN} above 100 nF, raising C_{IN} beyond 100–200 nF is difficult to justify.

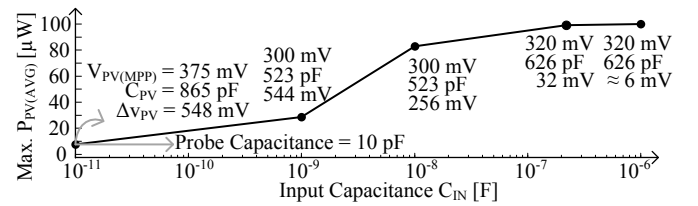


Fig. 7. Measured photovoltaic power across input capacitance.

v_{PV} 's maximum power point $V_{PV(MPP)}$ shifts 20 mV from 300 to 320 mV when C_{IN} rises above 1 nF. The drift is more severe below 1 nF because the ripple pulls v_{PV} below ground. So with only 10 pF, $V_{PV(MPP)}$'s variation is not only higher but also in the opposite direction (countering effects of a negative voltage).

V. OUTPUT CONTROL AND REGULATION

A. Lightly Sourced

When lightly sourced, the output v_O receives a fixed energy packet E_{PV} from the PV cell v_{PV} and a variable energy packet E_{BAT} from the battery v_{BAT} . The aim of the controller in this mode of operation is to determine the size of E_{BAT} that is necessary to keep v_O near its target v_{REF} . Transconductor G_{LS} and comparator CP_{LS} in Fig. 2 close a pulse-width modulation (PWM) feedback loop about v_O for this purpose, to set how long L_X should energize from v_{BAT} , and in the case of Fig. 3, to set t_{BE} to 1.7 μs so that i_L rises to 17 mA.

Operationally, G_{LS} compares v_O and v_{REF} to generate an error signal v_{EA} that C_{LS} filters into a slow-moving signal and CP_{LS} converts to energizing time t_{BE} . For this, CP_{LS} compares v_{EA} with a clocked ramp v_R . This way, CP_{LS} trips its output v_{LS} high when v_R 's ramp begins and low when v_R surpasses v_{EA} , the pulse width of which sets t_{BE} . So if a load suddenly pulls v_O below v_{REF} , v_{EA} rises, and v_R requires more time to surpass v_{EA} . As a result, v_{LS} 's pulse width is longer and L_X draws more energy from v_{BAT} to supply the load.

Output Ripple: The purpose of capacitor C_O is to suppress variations in v_O . For this, C_O receives excess energy from v_{BAT} 's E_{BAT} and supplies it to the load when needed, when L_X idles. For example, E_{BAT} supplies more power when L_X energizes and drains across t_{BE} and t_{BD} in Fig. 3 than the load requires, so across these times, C_O charges and v_O rises 22 mV in Fig. 8. Across the rest of the switching cycle, when L_X idles and L_X delivers E_{PV} , C_O supplies what the system cannot, so v_O falls to produce the ripple shown. In this mode, f_{CLK} sets the operating frequency of the system.

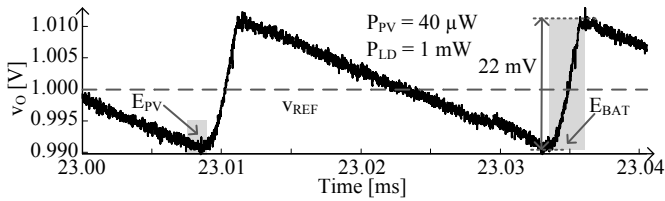


Fig. 8. Measured output when lightly sourced.

Load Regulation: Since L_X idles between deliveries, the full load P_{LD} discharges C_O , and heavier loads pull v_O further. v_O suffers this penalty even after the feedback loop compensates by raising the size of v_{BAT} 's energy packet E_{BAT} because C_O always supplies all of P_{LD} when L_X idles. This is why v_O 's ripple increases with heavier loads in Fig. 9. So when loaded with up to 1 mW, the PWM loop that G_{LS} and CP_{LS} close regulates v_O to 1 V within $\pm 4\text{--}\pm 11$ mV.

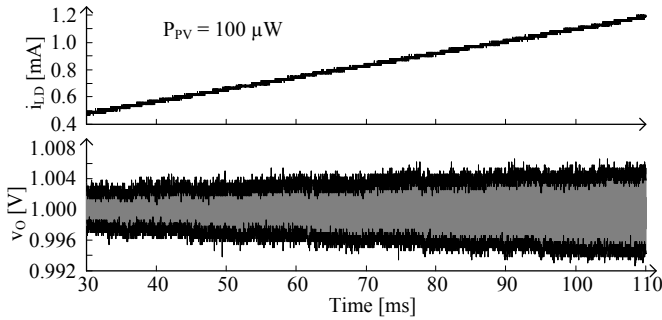


Fig. 9. Measured output when load current climbs.

Stability: G_{LS} 's voltage gain and CP_{LS} 's ramp translation to time [16]–[17] set the low-frequency gain across the loop. Since out-of-phase zeros and inductor poles disappear in discontinuous-conduction mode (DCM), C_O only introduces one pole p_O that C_O 's equivalent series resistance $R_{ESR,O}$ later limits with one in-phase zero z_{ESR} [17]. Except, G_{LS} 's output resistance R_{EA} , R_{LS} , and C_{LS} establish the dominant pole of the loop, R_{LS} introduces a phase-saving zero that offsets the phase lost with p_O , and since $R_{ESR,O}$ is low at 10 m Ω , z_{ESR} is well above the bandwidth of the loop. This way, with only one dominant pole, the loop gain reaches the system's bandwidth f_{0dB} at -20 dB per decade with close to 90° of phase margin, which means, the loop is stable.

B. Heavily Sourced

When heavily sourced, the PV cell v_{PV} supplies more power with P_{PV} than the load P_{LD} requires. So after satisfying the load, the system directs excess PV power to the battery v_{BAT} . The aim of the controller in this mode is to determine where to steer v_{PV} 's energy packets. The hysteretic comparator CP_{HS} in Fig. 2 closes a feedback loop about v_O for this purpose.

Output Ripple: When P_{LD} discharges C_O to the extent that v_O falls 25 mV below v_{REF} , at 6.1 ms in Fig. 10, CP_{HS} trips its output v_{HS} high. This prompts the power stage to steer E_{PV} 's to v_O , and because P_{PV} supplies more than P_{LD} sinks, C_O 's v_O rises during this time. When E_{PV} 's raise v_O 25 mV above v_{REF} , at 7.9 ms, CP_{HS} trips v_{HS} low. This commands the network to steer E_{PV} 's to v_{BAT} , until again, P_{LD} pulls v_O 25 mV below v_{REF} at 10.4 ms, after which the process repeats.

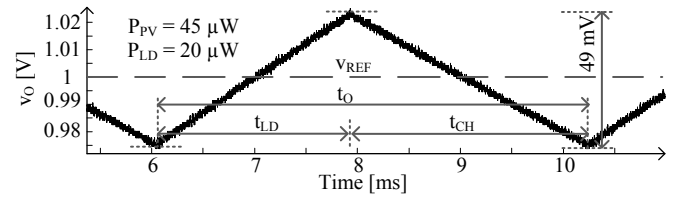


Fig. 10. Measured output when heavily sourced.

Load Regulation: When heavily sourced, the hysteretic loop that CP_{HS} closes regulates v_O in Fig. 10 to 1 V within ± 25 mV across load levels. Since CP_{HS} fixes v_O 's ripple in this mode, and heavier loads decelerate v_O 's rise and accelerate v_O 's fall, when not receiving E_{PV} 's, v_{BAT} 's charge time t_{CH} shortens with heavier loads. v_O 's rise time t_{LD} , on the other hand, lengthens when receiving E_{PV} 's with heavier loads because loads draw power away from C_O . As a result, t_{CH} and t_{LD} nearly cancel between 30 and 60 μ W, which is why the overall period t_O and corresponding operating frequency f_O in Fig. 11 remain nearly constant at 2.3 ms and 439 Hz in that region. Lighter loads, however, extend t_{CH} more than they shorten t_{LD} , and vice versa for heavier loads. As a result, t_O rises with both lighter and heavier loads to produce the valley response shown, and f_O shifts between 109 and 439 Hz.

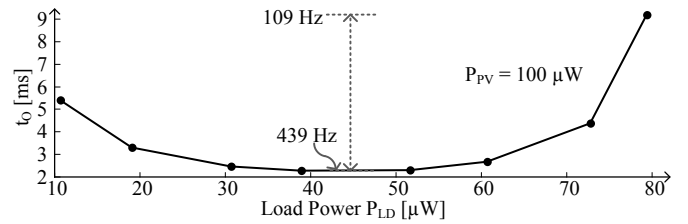


Fig. 11. Measured output period across load power when heavily sourced.

Stability: Since L_X is still in DCM when heavily sourced, out-of-phase zeros and inductor poles are absent. So C_O introduces a pole p_O that C_O 's low $R_{ESR,O}$ limits with an in-phase zero z_{ESR} at a frequency that is well above the system's bandwidth f_{0dB} [17]. CP_{HS} 's propagation delay is so short that the pole CP_{HS} establishes is well above f_{0dB} , so p_O is dominant. This way, the loop gain reaches f_{0dB} at -20 dB per decade with nearly 90° of phase margin, which means, the loop is stable.

C. Mode Transitions

Hysteretic comparator CP_M in Fig. 2 determines which mode of operation the system adopts. If load power P_{LD} overwhelms what PV power P_{PV} can supply, for example, and the system is at first in the heavily sourced mode, P_{LD} discharges C_O and v_O falls. v_O continues to fall past CP_{HS} 's lower threshold, after CP_{HS} commands the network to steer all E_{PV} 's to v_O , because E_{PV} 's cannot sustain P_{LD} . When v_O falls below CP_M 's lower threshold, though, CP_M 's output v_M rises to shift the system into high gear, into the lightly sourced mode.

If on the other hand, the system is in lightly sourced mode and P_{LD} drops to the point P_{PV} can sustain P_{LD} , E_{PV} 's and E_{BAT} 's overwhelm P_{LD} . As a result, C_O overcharges and v_O rises to CP_M 's upper threshold. This trips v_M down to shift the system into low gear, into the heavily sourced mode. In all, CP_M shifts modes when v_O rises above and falls below its 1-V reference v_{REF} by, in this case, roughly 75 mV. Notice this 150-mV hysteretic window is wider than CP_{HS} 's 50-mV

counterpart. This ensures CP_M does not interfere with the feedback loop that controls v_O when heavily sourced.

When P_{LD} is just beyond the reach of PV power P_{PV} , though, the network can switch back and forth between modes. This happens because, when CP_M draws assistance from the battery v_{BAT} , the network cannot switch fast enough to extract and deliver an arbitrarily small energy packet, so v_{BAT} 's E_{BAT} can oversupply v_O . In Fig. 12, for example, P_{LD} overloads P_{PV} by only $20 \mu\text{W}$, so even past CP_{HS} 's lower 25-mV threshold (at 3.3 ms), P_{LD} continues to pull v_O . The system shifts into lightly sourced when v_O reaches CP_M 's lower 75-mV threshold (at 5.2 ms). But since v_{PV} and v_{BAT} oversupply v_O , v_O does not stop rising until CP_M shifts the system back into heavily sourced. Except again, P_{LD} overloads P_{PV} , v_O falls back, and the process repeats until P_{LD} is high enough to sink all of the power that v_{PV} and v_{BAT} supply.

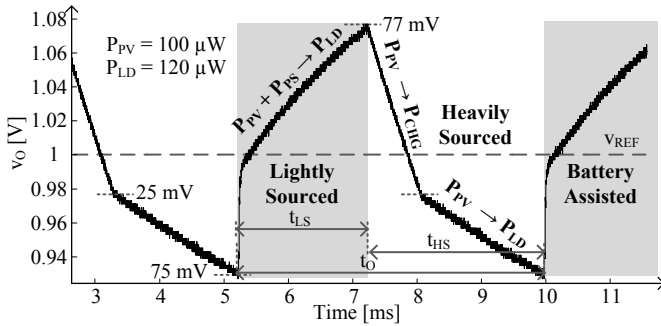


Fig. 12. Measured output when load power just exceeds PV power.

Load Regulation: Since CP_M 's propagation delay is short, CP_M reacts to vast and sudden changes in load power P_{LD} within one switching cycle. In Fig. 13, for example, v_O falls quickly when P_{LD} rises from $20 \mu\text{W}$ to 1 mW at 11 ms . But as soon as v_O falls 75 mV below 1 V , CP_M shifts the system into the lightly-sourced region. In this mode, energy packets from the battery arrest and reverse v_O 's fall. E_{BAT} 's similarly raise v_O after P_{LD} drops from 1 mW to $20 \mu\text{W}$ at 24 ms . But when v_O rises 77 mV above 1 V , CP_M shifts mode to, again, arrest and reverse the rise. This way, v_O 's excursions remain within $\pm 77\text{ mV}$ of v_{REF} , which means v_O remains within $\pm 7.7\%$ of its target across regions, load levels, and load dumps.

Once a rising 1-mA load dump transitions the system into lightly sourced, v_O rises and reaches steady state after 4 ms . The reason for this delay is that the PWM loop requires multiple clock cycles to adjust the energy packet that the battery supplies. And when a falling 1-mA load dump shifts the system into heavily sourced, CP_{HS} quickly commands the system to steer all PV energy packets to the battery. As a result, the load pulls v_O down without interruptions until CP_{HS} senses that v_O reaches CP_{HS} 's lower threshold of 0.975 V . In other words, the system always reacts within one cycle. And since v_O never overshoots, the phase margin of the feedback loops that G_{LS} and CP_{LS} , CP_{HS} , and CP_M close to regulate v_O when lightly sourced, heavily sourced, and across transitions is about 90° .

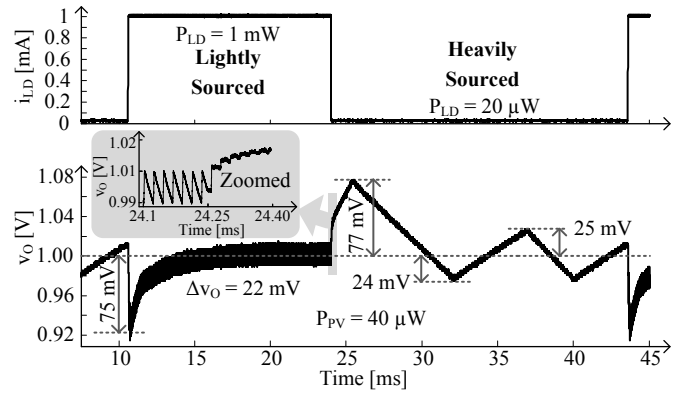


Fig. 13. Measured output in response to rising and falling load dumps.

Operating Frequency: In the heavily sourced region, like Fig. 11 and now Fig. 14 demonstrate, the switching period t_0 rises with v_O 's rise time t_{LS} when loads climb to $80 \mu\text{W}$. Between 90 and $150 \mu\text{W}$, P_{LD} and power losses are just beyond the reach of P_{PV} , but still below what E_{BAT} can supply across t_{CLK} , so the network shifts between modes like Fig. 12 shows. At and past $160 \mu\text{W}$, E_{BAT} no longer oversupplies v_O , so E_{PV} and E_{BAT} in lightly sourced fashion supply P_{LD} across every clock cycle, which means t_0 is t_{CLK} and f_{CLK} is 83 kHz .

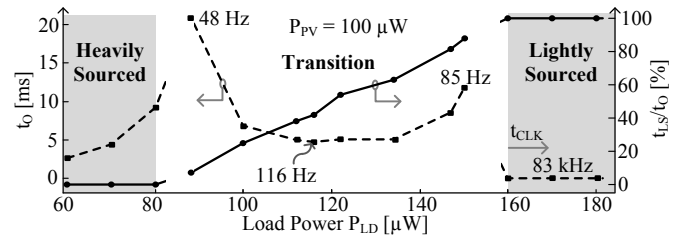


Fig. 14. Measured output period across load power.

When transitioning between modes, heavier loads extend v_O 's rise time t_{LS} (when lightly sourced) because less of E_{BAT} reaches C_O when P_{LD} sinks more power, so t_{LS} rises with P_{LD} . Heavier loads, however, also shorten heavily sourced time t_{HS} because they accelerate v_O 's fall. Between roughly 110 and $135 \mu\text{W}$, their effects cancel, so t_0 remains fairly constant at 4.5 ms . Between 90 and $110 \mu\text{W}$, heavier loads extend the rise time t_{LS} more than they shorten the fall time t_{HS} , and vice versa between 135 and $150 \mu\text{W}$, so t_0 is higher in both cases and f_0 shifts from 48 to 116 Hz .

VI. PROTOTYPED HARDWARE

The $610 \times 610\text{-}\mu\text{m}^2$ fabricated $0.18\text{-}\mu\text{m}$ CMOS die and the $4 \times 4\text{-mm}^2$ SOIC package that houses it in Fig. 15 house the MOS switches, drivers, comparators, logic, timer circuit, and transistor in Fig. 2. L_X 's $47 \mu\text{H}$, C_{IN} 's $0.22 \mu\text{F}$, and C_O 's $2.2 \mu\text{F}$ are off chip, and L_X occupies $3 \times 3 \times 1.5\text{ mm}^3$ and C_{IN} and C_O each occupy $1.6 \times 0.8 \times 0.9\text{ mm}^3$. For testability, the $3 \times 3 \times 1\text{-mm}^3$ PV cell v_{PV} from Hamamatsu, the compensating $2\text{-nF}\text{-}1.2\text{-M}\Omega$ $C_{LS}\text{-}R_{LS}$ filter; and the maximum power-point tracking clock f_{CLK} [9] are also off chip. This PV cell generates $100 \mu\text{W}/\text{mm}^2$ when exposed to solar light and $1 \mu\text{W}/\text{mm}^2$ when exposed to an indoor source that is 2 m away.

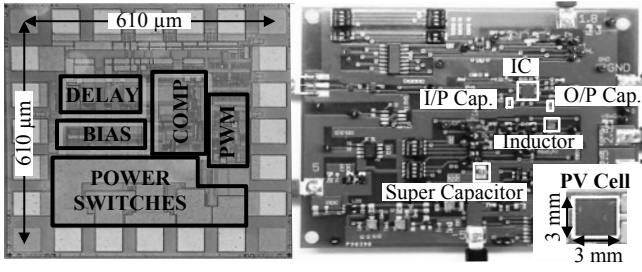


Fig. 15. Photographs of the die, board, and photovoltaic cell.

A. Power-Loss Management

Unfortunately, the switches and the controller in Fig. 2 dissipate ohmic, gate-drive, and quiescent power. But as already mentioned in Section III.E, selected switch dimensions balance ohmic and gate-drive losses when the PV cell supplies 100 μW and the load sinks 500 μW , which is half its full range. Under these conditions, when lightly sourced, the switches dissipate 35.2 μW , as Table II shows. But when only loaded with 40 μW , the switches burn less power at 5.55 μW because the system is no longer drawing assistance from the battery. And with 2 Ω of equivalent series resistance, L_X 's $R_{\text{ESR},L}$ burns 7.70 μW when lightly sourced and 5.55 μW when heavily sourced.

TABLE II. SIMULATED ENERGY- AND POWER-LOSS DISTRIBUTION

Blocks	Energy per Cycle [pJ]	Average Power [μW]
CP_M	7.86	0.68
Heavily Sourced (when $P_{\text{PV}} = 100 \mu\text{W}$ and $P_{\text{LD}} = 40 \mu\text{W}$)		
CP_{HS}	25.3	2.20
CP_O	26.9	2.34
CP_{CH}	16.4	1.42
$R_{\text{ESR},L}$	31.3	2.72
Switches	66.8	5.55
Lightly Sourced (when $P_{\text{PV}} = 100 \mu\text{W}$ and $P_{\text{LD}} = 500 \mu\text{W}$)		
G_{LS}	80.7	7.02
CP_{LS}	8.43	0.73
CP_O	86.2	7.50
$R_{\text{ESR},L}$	88.5	7.70
Switches	405	35.2

To keep controller losses low, the PWM loop that G_{LS} and CP_{LS} close turns off when the system is heavily sourced, and CP_{LS} and its ramp v_R operate only when L_X energizes from v_{BAT} , when determining when to end L_X 's energizing period t_{BE} . This way, G_{LS} and CP_{LS} dissipate 7.02 μW and 0.73 μW only when lightly sourced. Similarly, CP_{CH} and the hysteretic loop that CP_{HS} closes engage only when heavily sourced. CP_{CH} , however, operates only when L_X charges v_{BAT} , and CP_{HS} only across t_{PE} , when delivering energy to v_O , so CP_{CH} and CP_{HS} consume 1.42 μW and 2.20 μW only when heavily sourced. CP_M draws little quiescent power across both modes to burn 0.68 μW . Like CP_M , CP_O also operates across both modes, but only when L_X delivers energy to v_O , when determining when to stop supplying v_O . This way, CP_O dissipates 7.50 μW when lightly sourced and 2.34 μW when heavily sourced.

Response delays in CP_O and CP_{CH} extend $M_{\text{PO1,2}}$'s and M_{PCH} 's connection times. This can be problematic because keeping $M_{\text{PO1,2}}$ and M_{PCH} closed after *delivering* energy packets *draws* power from their intended recipients, from C_O

when supplying the load and from C_{BAT} when charging C_{BAT} . To minimize this drain, $M_{\text{PO1,2}}$'s and M_{PCH} 's resistances are slightly higher than the values that minimize their ohmic and gate-drive losses. This way, the voltages $M_{\text{PO1,2}}$ and M_{PCH} produce are high enough to keep CP_O 's and CP_{CH} 's delays low. Therefore, while still lower than other switches and L_X 's $R_{\text{ESR},L}$, the slight rise in $M_{\text{PO1,2}}$'s and M_{PCH} 's losses is much lower than the drain loss that lower voltages across $M_{\text{PO1,2}}$ and M_{PCH} would have caused.

B. Power-Conversion Efficiency

Efficiency η_C refers to the fraction of power drawn that reaches the output. Since the PV cell supplies the load and charges the battery when heavily sourced, battery power P_{BAT} in this mode is part of output power P_O and η_C is the fraction of P_{PV} that reaches v_{BAT} as P_{BAT} and v_O as P_{LD} :

$$\eta_{\text{C}}|_{\text{HS}} \equiv \frac{P_O}{P_{\text{IN}}} = \frac{P_{\text{LD}} + P_{\text{BAT}}}{P_{\text{PV}}} \quad (5)$$

When lightly sourced, however, the system derives power from the PV cell and the battery, so P_{BAT} is part of input power P_{IN} and η_C in this mode is the fraction of P_{PV} and P_{BAT} that reaches the load as P_{LD} :

$$\eta_{\text{C}}|_{\text{LS}} \equiv \frac{P_O}{P_{\text{IN}}} = \frac{P_{\text{LD}}}{P_{\text{PV}} + P_{\text{BAT}}} \quad (6)$$

Notice that the system first drew from the PV cell (when heavily sourced) the battery energy delivered when lightly sourced. So to deliver battery energy, the system loses power during both the heavily- and lightly-sourced states, which when considered across time, η_C as just defined comprehends. Regardless, ohmic and gate-drive power for the switches and duty-cycled power to the controller keep the system from delivering as much power as it receives, so η_C is never 100%.

Across modes, the η_C defined and graphed in Fig. 16 peaks at 86% when load power is 0.5 mW and PV power is 100 μW because switch dimensions balance ohmic and gate-drive power at this setting. η_C falls with heavier loads and lower PV power because quadratic ohmic losses when conducting energy packets outpace linear increases in drawn battery power. η_C also falls with lighter loads because gate-drive and non-duty-cycled controller losses do not scale with output power, so losses become a larger fraction of the power delivered. And since G_{LS} and CP_{LS} in the PWM loop consume more power than CP_{HS} in the hysteretic loop, efficiency is generally lower when lightly sourced than when heavily sourced.

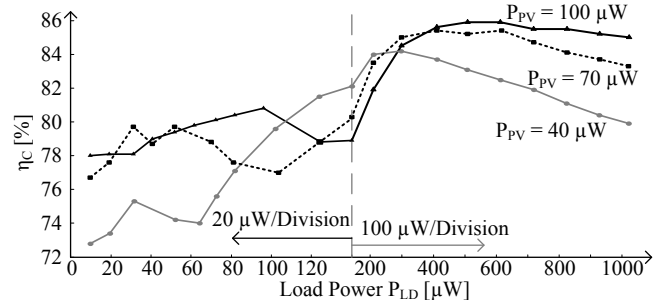


Fig. 16. Measured power-conversion efficiency across load and PV power.

VII. CONTEXT

Although switched-capacitor networks in [18] and [20] from Table III occupy less space, they draw less than 10 μW with less than 50% power-conversion efficiency. Switched inductors in [19], [21], and here may sacrifice board space for one off-chip inductor, but they also draw hundreds of microwatts with more than 60% efficiency. Although conversion efficiencies in [19], [21], and here are largely comparable, [19] does not regulate its output, and the output ripple in [21] grows substantially with load current. And without regulation, [19] must enlist a regulator to supply the load, the additional losses of which reduce efficiency.

The charge-supply presented here regulates its output within ± 25 mV across loads and operating modes in steady state and within ± 77 mV across 1-mW load dumps. Even though the controller consumes more power at 3–30 μW (for better regulation) than [21] does at 400 nW, conversion efficiency is nevertheless 3%–5% higher. This is because the power stage is more efficient across PV and load power, and system components operate only when needed. Plus, [21] draws battery power when PV power is sufficient to supply the load. This means, the system transfers PV energy twice, first from the cell to the battery and then from the battery to the load, so losses are greater and efficiency is lower. However, integrating the 1-V reference and the clock into the chip, which are now off chip for experimental purposes, can dissipate another 1 μW [2], so conversion efficiency can be 0.1%, 1%, and 10% lower than Fig. 15 shows when delivering 1 mW, 100 μW , and 10 μW to the load.

Unlike in [21] and [22], which also draw battery assistance, the system here draws assistance only when the PV cell cannot

supply the load, which saves battery energy. Plus, when drawing assistance, this system still supplies PV power to the load, so battery assistance is lower and the savings is greater. And although the system in [13] shares common traits with the one here, the PV cell in [13] rarely produces more power than the load demands, so the charging path that directs excess power to the battery is a simple diode. This is why charging efficiency in [13] (according to simulations because [13] does not show experimental results) does not surpass 70%. Here, the system modifies the charging path to produce (according to measurements of an actual prototype with a $3 \times 3 \times 1\text{-mm}^3$ PV cell) 2%–16% higher power-conversion efficiencies.

VIII. CONCLUSIONS

The 0.18- μm light-harvesting battery-assisted charger-supply presented here draws 10–100 μW from a $3 \times 3 \times 1\text{-mm}^3$ photovoltaic (PV) cell and up to 1 mW from a battery to supply a 0–1-mW load. The switched inductor regulates 1 V within ± 25 mV in steady state and within ± 77 mV across 1-mA load dumps with 73%–86% efficiency, and charges the battery with excess PV power. The system also keeps the PV cell within 1% of its maximum power point (MPP) with 220 nF across the cell and within 17% with 10 nF. Staying near the MPP with high power-conversion efficiency is important because light is not always available, indoor lighting is a weak source, small cells draw little power, and tiny batteries deplete easily. This is why understanding and accounting for how the converter affects the PV cell and how the system consumes power is essential in PV-supplied microsystems.

TABLE III. PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	PV Chargers		PV Charger-Supplies		
	ISSCC '14 [18]	ISSCC '11 [19]	TCAS I '13 [20]	ISSCC '13 [21]	This Work
Power Stage	Switched C	Switched L	Switched C	Switched L	Switched L
Technology	0.18 μm	0.25 μm	0.18 μm	0.18 μm	0.18 μm
v_{BAT}	4 V	3 V	3.6 V	3 V	1.8 V
PV Cell	0.84 mm^2	Emulated	0.07 mm^2		$3 \times 3 \times 1 \text{ mm}^3$
v_{PV}	0.14–0.5 V	0.5–2 V	0.44–0.5 V		0.27–0.32 V
Δv_{PV}				10 mV	30 mV
P_{PV}	< 10 μW	< 10 mW	< 80 nW		< 100 μW
v_{O}	—	—	0.45 V	1 V, 1.8 V	1 V
Δv_{O}	—	—		$\propto i_{\text{LD}}$	–24/+25 mV
Load-Dump Resp.	—	—			–75/+77 mV
Load Power	—	—	72 pW–90 nW	1 μW –1 mW	0–1 mW
Response Time	—	—			2.5 ms
L_{X}	—	1 mH	—		47 μH , 2 Ω $3 \times 3 \times 1.5 \text{ mm}^3$
C_{IN}					220 nF
C_{O}					2.2 μF
f_{CLK}	500 Hz–19 MHz		100 kHz	< 20 kHz	8–85 kHz
Controller Power	170 pW–3 nW	2.4–3.5 μW		< 400 nW	3–30 μW
$P_{\text{PV}}/P_{\text{PV(MPP)}}$					99.2%
η_{C}	35%–50%	60%–83% (1 Cell) 60%–87% (> 1 Cell)		68%–83%	73%–86%

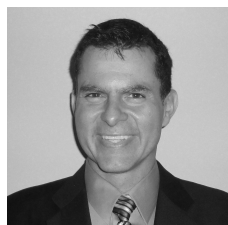
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