Autonomous and Programmable 12-W 10-kHz Single-Cell Li-Ion Battery Tester

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Abstract—Portable electronics like laptops are ubiquitous nowadays and they depend on batteries for power. Unlike traditional power supplies, batteries have limited capacity, cycle life, power capability, and many other restrictions. To improve battery performance or select the best battery for an application, engineers need to accurately extract the battery’s parameters through a series of experiments. Existing battery testers often fall short in current flexibility, accuracy, and battery voltage range, thus cannot accommodate all the necessary experiments and different battery types with a single setup. In this paper, a 12-W battery tester using linear charger/discharger and bipolar power supply is proposed. The tester can provide programmable current profile up to 3.3 A and 10 kHz with a wide battery voltage range to accommodate for different battery types. The tester can also regulate battery voltage and perform constant voltage charge and discharge. A prototype is implemented, and the testing capabilities are demonstrated with common battery experiments using a commercial 18650 cylindrical battery. The experimental results show the tester’s excellent current accuracy and flexibility.

Index Terms—Programmable tester, Li-ion batteries, charger, discharger, alternating current, internal resistance, state of charge (SoC).

I. BATTERIES IN MICROELECTRONICS

Batteries are popular energy sources to portable electronics such as cellphones, wireless headphones, and laptops. Components inside the device, including the digital-signal processors (DSPs), data converters, power amplifiers, antennas, and sensors, depend on the battery to operate as shown in Fig. 1. As the world’s demand for microelectronics continue to grow, the battery market is expected to expand steadily. It is projected that the global market size for lithium-ion batteries will double in the next five years to $91.9 billion [1].

Despite the continuous development of battery technologies, there are still many challenges and limitations. The parameters that restrict a battery’s performance and applications include capacity, cycle life, series resistance, self-discharge, power capability, and energy density [2-5]. To understand the battery’s limitations and explore methods to improve battery performance, it is necessary to experimentally extract the battery’s parameters and conduct rigorous testing [6].

However, battery testing procedures are often lengthy and prone to errors, which calls for an accurate and autonomous tester. For example, the cycle life test for a typical Li-ion battery requires hundreds of charge-discharge cycles, which can take months to complete [7, 8]. Furthermore, the necessary experiments to fully characterize a battery require the tester to source/sink programmable current with high accuracy, which cannot be done with conventional power supplies. Batteries like lithium ions also have strict requirements on the operating voltage, and a constant current–constant voltage (CC–CV) charge is necessary to prevent overcharging.

Among the battery testers investigated, [9-11] can source and sink programmable current. [9, 10] can source and sink a large current, which is necessary when testing batteries with high power capability such as electric vehicle batteries. However, they are both limited in current ripple frequency and battery voltage range. Commercial linear testers [12, 13] have high accuracy and wide battery voltage range, but their slow response time limits the maximum current ripple frequency that can be applied.

In this paper, we propose a compact 12-W battery tester that is capable of charging and discharging the battery with arbitrary current profile up to 3.3 A and 10 kHz. The proposed tester has a high bandwidth, high accuracy, seamless CC–CV transition, and can discharge the battery below 0 V. The tester is based on the linear charger proposed by our group in [14].

The rest of the paper is organized as follows: Section II discusses the tester circuit and operation. Section III demonstrates the testing capability. Section IV reviews and compares the tester’s performance with the state of the art.

II. PROPOSED BATTERY TESTER

A. Charger

A linear charger is implemented to source programmable current for the battery as shown in Fig. 2. The linear charger contains two negative feedback loops: a current loop to regulate battery current iB and a voltage loop to regulate battery voltage vB. The current loop consists of transconductance amplifier A_{GP}, MOSFET M_p, resistor R_p, R_p1, R_p2, and R_p3. The voltage loop consists of op amp A_{VP}, diode D_p, MOSFET M_p, current-sense resistor R_s, and battery internal resistance R_b.

During constant current (CC) operation, the voltage loop is off because v_B is lower than the reference voltage V_{BH}, and A_{VP} outputs a voltage close to the negative power supply, forcing diode D_p to be off. Meanwhile, the current loop has high gain
due to the high impedance at $v_{GH}$. $AGP$’s input voltage $v_{NH}$ is regulated to be approximately equal to $v_{PH}$, which is set by the reference voltage $v_{RH}$. $v_{PH}$ is then level-shifted by the resistor divider $R_P1$ and $R_P2$ to reach a higher voltage at $v_C$. The voltage across $R_P$ induces a current $i_B$ to flow to the battery. $R_P1$ and $R_P2$ are chosen to be relatively high resistance to ensure most of the current through $R_P$ flows into the battery. $R_{P3}$ compensates for the voltage drop across $R_P1$ due to the input current of $AGP$ and $R_{P3} = R_{P1} \parallel R_{P2}$.

To analyze the current loop gain, the current loop is “broken” at node $v_C$. When a small signal is injected, the voltage-divided fraction of the signal reaches $v_{NH}$ and gets amplified by $AGP$’s transconductance $GGP$. The output current flows into the total impedance at the gate of $MP$ and determines the gate voltage $v_{GH}$. $MP$ responds to $v_{GH}$ by pulling current $i_B$, which flows through $R_P$ and sets the voltage $v_C$. The current loop gain is

$$A_{LGI} = \frac{R_{PH}}{R_{P1} + \frac{R_{PH}}{R_{P2}}},$$

where $R_{PH}$ is the input resistance of $AGP$ and $g_{MP}$ is the transconductance of $MP$. $Z_{GH}$ is the total impedance at $v_{GH}$:

$$Z_{GH} = R_{GO} \parallel Z_{V(CL)} \parallel \frac{1}{sC_{GH}},$$

where $R_{GO}$ is the output resistance of $AGP$, $C_{GH}$ is the gate capacitance of $MP$, and $Z_{V(CL)}$ is the closed-loop impedance of the voltage loop.

The small signal gain of the current and voltage loops during CC operation are shown in Fig. 3(a). The current loop has one low-frequency pole $p_G$ at the gate of $MP$ at around 1 kHz. All the other parasitic poles occur above 0-dB frequency $f_{0dB}$, which results in a stable phase margin of 90° and a bandwidth of 10 MHz. The voltage loop’s gain is below -30 dB across the frequency spectrum and does not interfere with the current loop operation.

When the charger transition from CC to CV operation, the total impedance at $v_G$ decreases as $DP$ becomes forward biased. Therefore, $A_{LGi}$ decreases and $A_{LGV}$ increases simultaneously. As shown in Fig. 3(c), the current loop’s dominant pole $p_G$ is pushed to a higher frequency as the gate impedance decreases. The voltage loop interacts with the current loop and introduces a zero-pole pair $(z_{LGV}, p_{LGV})$ in $A_{LGV}$. The phase margin is always higher than 90 degrees because $z_{LGV}$ precedes $p_{LGV}$. On the other hand, $A_{LGV}$ only has one dominant pole $p_{AVP}$ with all other zeros/poles above $f_{0dB}$ as shown in Fig. 3(d), thus has a stable phase margin of 90 degrees.

To further investigate the zero-pole pair in $A_{LGi}$, $Z_{V(CL)}$ in (2) can be expressed as

$$Z_{V(CL)} = Z_{V(OL)} \parallel Z_{V(CL)} \parallel \frac{1}{sC_{GH}},$$

where $Z_{V(OL)}$ is the open-loop impedance looking into $DP$. When $Z_{V(CL)}$ is high, $Z_{V(CL)} \parallel Z_{V(OL)}$ dominates the closed-loop impedance and $Z_{V(CL)}$ increases as $A_{LGV}$ decreases. Because $Z_{V(CL)}$ dominates the total gate impedance at low frequencies, $Z_{GH}$ will increase. Therefore, $AGP$’s output current will flow into a higher impedance, which introduces a zero $z_{LGV}$. When $C_{GH}$’s impedance dominates $Z_{GH}$ at higher frequencies, the effect of the zero is reversed and a reversal pole $p_{LGV}$ is introduced.

B. Discharger

The charger topology described previously is modified to form a discharger using a negative supply voltage as shown in Fig. 4. The negative supply provides the needed headroom for $R_N, M_N$. 

![Fig. 2. Proposed charger.](image)

![Fig. 3. Simulated loop gain in CC, CV, and CC–CV.](image)
and Rs to discharge the battery below 0 V without pushing Mn into triode region or decreasing the discharge current. The current loop consists of transconductance amplifier AGN, MOSFET Mn, resistor RN, RN1, RN2, and RN3. The voltage loop consists of op amp AVN, diode DN, MOSFET Mn, current-sense resistor RS, and RB. The major difference is that AGN is connected in inverting amplifier configuration to generate a negative voltage vD with a positive reference voltage vRL.

During CC operation, DN is reverse-biased, and the voltage loop is turned off. The current loop has high gain due to high gate impedance. As VB decreases close to the reference voltage vBL, the diode starts conducting and the gate impedance decreases due to AVN’s low output resistance. Therefore, the voltage loop gains strength while the current loop loses strength. During CV operation, the voltage loop dominates, and the current loop gain is diminished by the low gate impedance. The small signal gain of the discharger resembles the charger circuit shown in Fig. 3, thus will not be repeated here.

C. Prototype

The charger and discharger described above are designed and implemented with a PCB. A prototype tester is completed with benchtop instruments as shown in Fig. 5. Reference voltage vRH, vRL, vBH, and vBL are provided by function generators. The charge current and discharge current are sensed using Kelvin connection with a 100 mΩ current-sense resistor RS. The charger/discharger output voltage VO and battery voltage VB are acquired using digital multimeters (DMMs) and oscilloscopes. Battery temperature TB is acquired using a thermistor. The experimental setup is shown in Fig. 6.

The circuit components are chosen to accommodate battery current up to 3.3 A. The minimum regulation current needs to overcome the noise current injected into the battery. The noise current is measured to be 50 mA RMS, thus the minimum regulation current is determined to be 10x higher at 500 mA. The supply voltage VDD and VSS are chosen to minimize the drain-source voltage of the MOSFETs while guaranteeing operation in saturation, so that the conduction loss and heat generation is reduced. To further manage the heat produced by the MOSFETs, heat sinks and small fans are used to improve the heat transfer between the MOSFETs and the ambient air, maintaining MOSFET temperature below 50 °C.

The DC power supplies, function generators, DMMs, and oscilloscopes are controlled by a PC using LabVIEW through the GPIB interface. To accommodate for rigorous testing, all experiment procedures are programmed in LabVIEW to achieve fully autonomous testing. The acquired data is exported in Excel format at the end of the experiment for analysis.

Both hardware and software protections are implemented in the prototype tester to ensure the tested Li ion operates within the safe voltage, current, and temperature range and prevent potential hazards such as irreversible performance degradation, thermal runaway, or even explosion [15-17]. The voltage loops of the proposed circuit regulate VB between vBH and vBL to avoid overcharging and overdischarging. The power supply’s current limit is set to the maximum iB to prevent overcurrent. LabVIEW software is programmed to terminate the experiment when monitored VB, iB, or TB exceed the user-specified range.

III. TESTING CAPABILITY

The prototype tester is used to perform common tests with three commercial Li ions detailed in Table I. All test batteries are cycled five times prior to testing to ensure stable capacity decay. Because the test procedures and the tester’s operation are the same for all three batteries, the results from NCR18650B are presented for demonstration in the following discussion.

A. Energy

A battery’s energy information can be extracted through a charge-discharge cycle as shown in Fig. 7. The cycle can be divided into five sections: CC charge t(CCC), CV charge t(CCV),...
rest \(t_{R1}\), discharge \(t_D\), and rest \(t_{R2}\). The fully depleted battery’s initial open-circuit voltage is \(v_{OC1}\). During \(t_{C(CC)}\), constant charge current \(i_C(CC)\) is applied to the battery and \(v_B\) rises. During \(t_{C(CV)}\), \(v_B\) is held at \(v_{CV}\) while charge current \(i_C\) is slowly decreased to the chosen cutoff level \(i_{CO}\). The fully charged battery is rested for \(t_{R1}\) while \(v_B\) undergoes relaxation to reach open-circuit voltage \(v_{OC2}\).

During \(t_0\), the battery is discharged with constant current \(i_0\) to discharge cutoff voltage \(v_{CO}\). The fully discharged battery is rested during \(t_{R2}\), and the open-circuit voltage of the battery returns to the initial value \(v_{OC1}\). The sharp rise/drop \(\Delta v_{CR}, \Delta v_{CF}, \Delta v_{DF}, \Delta v_{DFR}\) are due to the voltage across internal resistance \(R_B\) when a current is suddenly applied or removed.

**Capacity**: The charge capacity is the amount of charge \(q_B(TOT)\) that can be extracted from a fully charged battery:

\[
q_B(TOT) = \int_0^{t_B} i_d dt.
\]

For demonstration, the parameters \(i_C, v_{CV}, i_{CO}, v_{CO}, t_{R1}, t_{R2}\) are chosen to be 1.625 A, 4.2 V, 65 mA, 3.25 A, 2 V, 30 minutes, and 30 minutes. \(i_d\) is integrated to obtain a capacity of 3187 mAh.

**Energy Efficiency**: The energy efficiency for the charge-discharge cycle is the ratio of the energy that can be extracted from the battery during discharge (\(E_D\)) and the energy that is delivered to the battery during charge (\(E_C\)):

\[
\eta_E = \frac{E_D}{E_C} = \frac{\int_0^{t_B} i_d v_B dt - \int_0^{t_B} i_C v_B dt}{\int_0^{t_B} i_C v_B dt}.
\]

The energy efficiency is usually much lower than 100% due to energy loss through \(R_B\), \(E_C\), \(E_D\), and \(\eta_E\) for the cycle described previously are calculated to be 44.0 kJ, 37.7 kJ, and 85.5%, respectively.

**State-of-Charge**: A battery’s state-of-charge (SoC) is the fraction of remaining charge compared to the total charge capacity and can be calculated as:

\[
\text{SoC} = \text{SoC}_0 + \frac{\Delta q_X}{q_B(TOT)} = \text{SoC}_0 + \frac{\int_0^{t_B} i_d dt}{q_B(TOT)},
\]

where \(\text{SoC}_0\) is the initial SoC and \(\Delta q_X\) is the charge injected or extracted from the battery during \(t_X\). When the battery is initially discharged to the cutoff voltage \(v_{CO}\), its \(\text{SoC}_0\) is defined to be zero. Therefore, the battery’s SoC at any instance can be calculated by integrating the measured \(i_d\) if \(q_B(TOT)\) is known.

**Fig. 7.** Typical charge-discharge cycle.

**Fig. 8.** (a) Experimental \(v_{OC}-\text{SoC}\), and (b) ICA results.

**Estimating the battery’s SoC is important as it provides the user with information on usable charge left in the battery. One method to estimate the battery’s SoC is through the relationship between open-circuit voltage \(v_{OC}\) and \(\text{SoC}\) [18, 19]. To obtain this relationship, the charge-discharge cycle shown in Fig. 7 is modified with low \(i_C\) and \(i_D\) so that the voltage across \(R_B\) is small [18]. For demonstration, \(i_C\) and \(i_D\) are chosen to be C/20 (162.5 mA) and the rest time \(t_{R1}\) and \(t_{R2}\) are chosen to be 2 hours.

The battery’s \(\text{SoC}\) with respect to time is calculated from measured \(i_d\) and \(q_B(TOT)\) using (7) with \(\text{SoC}_0\) defined to be zero. \(v_B\) is then plotted against \(\text{SoC}\), and the charge voltage curve \(v_C\) and discharge voltage curve \(v_D\) are averaged to obtain \(v_{OC}\) as shown in Fig. 8(a). \(v_C\) is at a slightly higher voltage compared to \(v_D\) due to \(R_B\). The estimated \(v_{OC}\) does not consider the hysteresis effect of the battery and assumes a constant \(v_{OC}\) at an \(\text{SoC}\) whether the battery was charged or discharged [20].

Similarly, Incremental Capacity Analysis (ICA) uses a charge-discharge cycle with low current to observe the battery’s ability to hold charge. ICA investigates the amount charge increment (\(\Delta q_b\)) for a voltage increment (\(\Delta v_{B}\)), which can also be interpreted as the capacitance of the battery \(C_b\) at an instance. For demonstration, \(\Delta q_b\) is fixed to be 2.71 mAh, corresponding to 1 minute of CC charging at C/20 (162.5 mA). The \(\Delta q_b/\Delta v_{B}\) curve derived from \(v_C\) in Fig. 8(a) is shown in Fig. 8(b).

The nonlinearity of \(v_B\) in Fig. 8(a) translates to the peaks and troughs of \(C_b\) in Fig. 8(b). The peaks in the ICA plot correspond to the region where \(v_C\) rises slowly with \(\text{SoC}\) and have been linked to specific chemical reactions in Li-ion batteries [18]. Therefore, ICA can reflect the electrochemical properties of the battery and be used to estimate its state of health [21].

Another method to extract the relationship between \(v_{OC}\) and \(\text{SoC}\) is shown in Fig. 9. The battery is fully charged using alternating intervals of current pulse \(t_C\) and rest \(t_R\). \(v_B\) can be obtained at the end of each \(t_R\). Similarly, the battery is discharged negative current pulses. For demonstration, the current pulse duration and rest time are both set to be 10 minutes. The amplitude of the charge current \(i_C\) and discharge current is set to be C/10 (325 mA).

For a Li-ion battery with known chemical properties, the diffusion coefficient of the lithium ions can also be obtained using the open-circuit voltage change \(\Delta v_{OC}\) with respect to the charge variation \(\Delta \text{SoC}\) and time \(t_C\) during a pulse. This method is...
commonly referred to as the Galvanostatic Intermittent Titration Techniques (GITT) [22, 23].

B. Internal Resistance

Internal resistance $R_B$ is a parameter that depends on temperature, SoC, and cycle life [24]. $R_B$ is a major source of power loss during battery operation and limits the battery’s power capability. Therefore, it is necessary to measure $R_B$ to accurately characterize a battery. Several common methods to measure $R_B$ are discussed in this section.

Transient Resistance: The battery’s transient resistance $R_{B(TR)}$ is the resistance on the conducting path and can be observed when $i_B$ increases or decreases sharply. One common method to measure $R_{B(TR)}$ is by applying two load currents that simulate the battery’s real operating conditions as shown in Fig. 10(a). The test battery is discharged with $i_1$ during $t_1$ and $i_2$ during $t_2$. $R_{B(TR)}$ is the ratio of the instantaneous voltage change $\Delta v_{R(TR)}$ and current change $\Delta i_B$:

$$R_{B(TR)} = \frac{\Delta v_{R(TR)}}{\Delta i_B}.$$ (8)

For demonstration, $R_{B(TR)}$ is obtained automatically at six different SoC’s as shown in Fig. 10(b). The current step is applied during the interval $t_{STEP}$. $i_1$, $i_2$, $t_1$, and $t_2$ are chosen to be 1 A, 0.5 A, 2 minutes, and 1 minute, respectively. After each $t_{STEP}$, the battery is discharged for $t_D$ to a new SoC and rested for $t_R$ (30 minutes). It can be observed that $R_{B(TR)}$ is significantly larger at 5% SoC, which is caused by the depletion of charge carriers. $R_{B(TR)}$ remains stable across the other SoC’s.

Hybrid Pulse Power Characterization (HPPC) is another test profile that can be used to obtain $R_{B(TR)}$. As shown in Fig. 11, a charge current pulse of duration $t_C$ is applied to the battery, followed by a period of rest $t_R$ and a discharge current pulse of duration $t_D$. $t_C$ and $t_D$ are small, so the battery’s SoC remains approximately constant. $\Delta v_{R(TR)}$ is the instantaneous voltage rise due to $R_{B(TR)}$. In addition, chemical reactions like charge transfer and ionic diffusion in Li ions contribute to the total internal resistance $R_{B(TOT)}$. Assuming change in SoC contributes to negligible $v_B$ rise, $R_{B(TOT)}$ including the effect of chemical reactions [25] can be calculated using the voltage change across the entire pulse $\Delta v_{R(TOT)}$ and the current pulse amplitude $\Delta i_B$:

$$R_{B(TOT)} = \frac{\Delta v_{R(TOT)}}{\Delta i_B}.$$ (9)

For demonstration, $t_C$ and $t_D$ are chosen to be 18 seconds each with an amplitude of 1 A, and $t_R$ is 15 minutes. The pulses are applied when the battery’s SoC is approximately 50%. $R_{B(TR)}$ during charge and discharge are calculated to be 150 mΩ and 152 mΩ. $R_{B(TOT)}$ during charge and discharge are calculated to be 176 mΩ and 175 mΩ.

AC Resistance: The battery’s AC resistance $R_{B(AC)}$ can be measured by applying a sinusoidal current of amplitude $i_{B(AC)}$, commonly chosen at 1 kHz, and measuring the corresponding sinusoidal voltage response $v_{B(AC)}$. $i_{B(AC)}$ is chosen so that $v_{B(AC)}$ is less than 20 mV to preserve linearity [26]. Fig. 12 shows $v_{B(AC)}$ generated by the prototype tester and the recorded $v_{B(AC)}$. Using $R_{B(PP)} = \frac{v_{B(PP)}}{i_{B(PP)}}$, $R_{B(AC)}$ is calculated to be 147 mΩ at 1 kHz, 50% SoC.

$R_{B(AC)}$ can be measured across a frequency range by varying the frequency of the excitation signal. The test battery’s $R_{B(AC)}$ is measured from 5 Hz to 100 kHz with 10 points per decade at 50% SoC, and the resulting resistance spectrum is shown in Fig. 13. It can be observed that a minimum resistance $R_{B(AC)}$ occurs at approximately 4.5 kHz. $R_{B(AC)}$ rises sharply at higher frequency due to the wire inductance.

C. Other Tests

Several battery tests that the tester can perform but are not demonstrated due to time or safety concerns are discussed here:

Overdischarge: Overdischarge is a common form of battery abuse and its effects on Li ions include capacity degradation, increased self-discharge, and internal short circuit [16]. To measure the capacity degradation due to overdischarge, the capacity test described previously is performed before and after the battery is discharged below the specified cutoff voltage. The tester’s capability to discharge the battery below 0 V allows various degrees of overdischarge to be investigated. The capacity degradation is the change in capacity.
Relaxation: A battery’s relaxation behavior is often investigated to determine the needed rest time \( t_R \) after charge/discharge for the battery to reach equilibrium. To investigate the effect of relaxation, the battery is charged/discharged to the desired SoC, and the current is removed. Different parameters of the battery can then be measured and compared when \( t_R \) is varied. For example, [27] investigates the accuracy of SoC estimation using \( V_{OC} \) when \( t_R \) is changed. [28] compares the accuracy of EIS performed on the battery after different \( t_R \).

Cycle life: Cycle life is defined as the number of charge-discharge cycles a battery can endure before its capacity reduces to a predefined percentage (commonly 80%) of the initial capacity. To perform a cycle life experiment, the test battery is repeatedly charged and discharged with the cycle shown in Fig. 7. The charge current and discharge current can be defined by the user to investigate the effect of current profiles on battery performance [29, 30].

D. Fault Detection

It is important to detect faulty Li-ion batteries to prevent potential hazards. A faulty Li-ion typically shows an abnormal decrease in capacity or increase in resistance [2]. The abnormal capacity degradation can be detected by measuring the battery’s capacity across multiple full discharges using (5). The internal resistance can be measured by injecting a small sinusoidal current and observing the voltage response. A battery with resistance higher than the typical range can be deemed as faulty.

Models that describe battery behaviors with electrical circuit components can also be used to detect faults [6, 31, 32]. The voltage and current data measured by the tester can be fitted to the battery model to generate estimated values for the battery’s inductive, capacitive, and resistive components. Values that lie outside the typical range can indicate the battery as faulty.

IV. PERFORMANCE AND LIMITATIONS

A. Output Current/Voltage Accuracy

The charge/discharge current values are determined by control voltages \( V_{RH} \) and \( V_{RL} \) when current loop regulates. \( V_{RH} \) and \( V_{RL} \) are compensated due to the gain and offset error of the system. The compensated control signals are

\[
V_{RH} = \alpha_H (V_{DD} - iC \cdot R_f) \left( \frac{-R_2}{R_1 + R_2} \right) + \beta_H,
\]

\[
V_{RL} = -\alpha_L (V_{DD} + iD \cdot R_N) \left( \frac{R_2}{R_3} \right) + \beta_L,
\]

where \( \alpha_H, \beta_H \) are the charger’s gain and offset compensation, and \( \alpha_L, \beta_L \) are the discharger’s gain and offset compensation. The system is calibrated by sweeping \( V_{RH} \) and \( V_{RL} \) separately. \( iC \) from the ideal, uncompensated, and compensated signals are shown in Fig. 14. For a standard \( iC \) of 1.625 A and \( iD \) of 3.25 A, the current error before compensation is 5.9% and 3.1%. After compensation, the error is less than 0.46% for \( iC \) and 0.31% for \( iD \). To investigate the tester’s consistency across cycles, the battery is charged (with constant \( iC \) of 812.5 mA) and discharged for 40 cycles. Measured \( iC \) shows no significant variation from cycle to cycle, and the 3\( \sigma \) limit for \( iC \) across 40 cycles is calculated to be ±1.8 mA.

The output voltage accuracy during CV charge/discharge is degraded by electronic noise, component heating, and the offset and gain error of op amp \( A_\text{VP} \) and \( A_\text{VN} \). After first-order compensation for the gain and offset error, the output voltage during CV charge at 4.2 V is sampled at 1 kHz and averaged. The worst-case remaining voltage error is measured to be 0.048%.

B. Output Current Rise Time

The tester’s maximum output current frequency depends on the rise/fall time of the current, which is affected by the current-loop bandwidth and slew rate. Since the current loop has a wide bandwidth of 10 MHz, the rise time will be mostly limited by slew rate due to the time it takes for \( A_{\text{GP}}/A_{\text{AGN}} \) to charge and discharge the gate capacitance of \( M_P/M_N \). Therefore, the worst-case output current frequency limit is for full-swing AC signals. For a 3.3 A pk-pk sinusoidal current with an offset of 1.625 A, the maximum frequency without significant distortion is observed to be approximately 10 kHz.

The step response of the charge/discharge current loops are measured to determine the slew rate of the system as shown in Fig. 15. Excitation \( V_{RH} \) and \( V_{RL} \) are applied so that \( iC \) and \( iD \) transition from 0 A to 1.63 A and 3.25 A, respectively. The rise time \( t_S \) for \( iC \) and \( iD \) measured from 10% to 90% of the steady state current \( i_{SS} \) is approximately 12 µs. The 5% settling time \( t_S \) for \( iC \) and \( iD \) measured 80 µs and 29 µs. The maximum current (\( i_{\text{MAX}} \)) and minimum current (\( i_{\text{MIN}} \)) is 1.7 A and 1.4 A when \( iC \) settles, and 3.3 A and 3.2 A when \( iD \) settles. The slew rate is calculated to be 140 mA/µs.

C. Measurement Accuracy

The voltage measurement accuracy is mainly limited by various sources of noise and the components’ temperature drift. The PCB components such as resistors, MOSFETs, and amplifiers inject electronic noise to the circuit. The noise voltage at the battery terminal is measured to be 6.2 mV. Accounting for the DMM’s error of 0.063%, the worst-case voltage measurement accuracy is 0.31% for a minimum \( V_{RB} \) of 2.5 V. The effect of noise is reduced as the voltage is sampled at 1 kHz and averaged. The voltage measurement resolution is limited by the DMM to be 2.5 µV.

Battery current \( i_B \) is converted to a voltage with current-sense resistor \( R_S \) and measured by the DMM. The current
The system achieves a peak current of 120 A, but the current generate the AC and DC components of the current separately.

However, the tester’s AC current frequency is limited to 5 kHz source current up to 200 A with a current error of 0.04%.

Linear dischargers. The tester can sink current up to 600 A and DC-DC converter with a current sink consists of 12 parallel programmable current by combining the charge current from a proposed in this work and the state of the art (SoA). [9] achieves linear dischargers.

Table II summarize the performance of the battery tester

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<td>140 mA/µs</td>
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</tbody>
</table>

measurement accuracy is limited by current noise and the variation of $R_S$. The chosen $R_S$ has a value of 100 mΩ, tolerance of 1%, and temperature coefficient of 50 ppm/°C. The tolerance error is minimized by measuring $R_S$ with the DMM prior to the experiment. The maximum temperature rise of $R_S$ within the design current range (50 mA to 3.3 A) is 20 °C, resulting in a 0.1% change to the resistance. The current noise is measured to be 50 mA RMS, which dominates the current measurement error. The measurements are averaged to reduce the effect of noise.

Battery temperature $T_B$ is obtained by measuring the resistance of a high-accuracy thermistor mounted to the surface of the test battery. Because the battery temperature remains within the range 20 °C to 30 °C throughout the experiments, the worst-case resistance error based on the datasheet is 1.27%, resulting in a temperature measurement error less than 0.38 °C.

D. Limitations

The proposed tester uses linear charger/discharger topology, and its efficiency limits the maximum current supported by the tester. The charger’s efficiency is the ratio of the power delivered to the battery and the power drawn from the supply. Considering the dominating power loss from $M_P$, $R_P$, and $R_S$, the theoretical efficiency is calculated to be 54.6%-61.5% during a standard charge at 1.625 A. The efficiency variation is due to $v_B$’s variation during charge. The charger’s efficiency is measured to be 57.7% when $v_B = 3.86$ V and $i_B = 1.625$ A. On the other hand, the discharger’s efficiency is not well-defined as the power drawn from the battery is fully dissipated.

The efficiency of the proposed tester and the corresponding power loss limits the maximum charge/discharge current to 3.3 A without overheating the MOSFETs. Several methods to achieve higher battery current include better thermal management, adaptive supply voltage to decrease MOSFET losses [31], and parallel branches of charger/discharger to distribute current stress [9].

E. Comparison with the State of the Art

Table II summarize the performance of the battery tester proposed in this work and the state of the art (SoA). [9] achieves programmable current by combining the charge current from a DC-DC converter with a current sink consists of 12 parallel linear dischargers. The tester can sink current up to 600 A and source current up to 200 A with a current error of 0.04 %. However, the tester’s AC current frequency is limited to 5 kHz and the minimum battery voltage is 1.5 V.

In [10], a battery tester that can output programmable current is implemented by controlling multiple buck converters to generate the AC and DC components of the current separately. The system achieves a peak current of 120 A, but the current accuracy of the system is limited to 1.5% and the highest AC current frequency is 2 kHz. A similar system with two buck converters is implemented in [11] and a high current error of 10% is observed in the system.

Commercial battery testers in [12, 13] use linear topologies and operate in the similar power range as the proposed testers. [12] displays lower applied voltage and current error than the proposed solution. However, the rise time of the current is higher, which limits the maximum AC current frequency that can be applied to the battery. Similarly, [13] shows a lower applied voltage error, yet its current rise time is much slower. [13] has the same 0 V minimum discharge voltage while [12] can discharge batteries to -5 V.

Because the SoA testers’ dimensions are not specified and they operate at different power levels, the considerations for form factors are discussed. Component size and heat management are two main factors that limit the overall solution size. Because heat generation is proportional to power loss, linear testers require more robust heat management systems compared to the more efficient switched testers. On the other hand, switched testers require bulky inductors while linear testers have smaller individual components. The proposed solution has a dimension of 140×241×27 mm³ without the benchtop instruments. Additional PCB area is given to $M_P$/$M_N$ and $R_P$/Rs to lower heating and fit the heat sinks and small fans.

V. Conclusions

The 12-W battery tester proposed in this paper can automatically perform various common battery tests with a single setup. The tester exhibits excellent stability and a wide battery voltage range. The current loop’s 10-MHz bandwidth allows the tester to generate arbitrary charge/discharge current up to 10 kHz, the highest among the state of the art. The generated current is within 0.46% of the desired value during a standard charge/discharge, which is comparable to the existing testers. Additionally, the tester’s voltage loop provides reliable battery voltage regulation and seamless CC–CV transition.

Further works include (i) Integration of sensing and charger/discharger circuit to decrease solution size and minimize parasitic capacitances. (ii) Implement adaptive supply voltage [33] to decrease heat dissipation, increase tester efficiency, and increase maximum current level. (iii) Incorporate parallel branches of charger/discharger to accommodate higher current.

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