High-PSR LDOs: Variations, Improvements, and Best Compromise

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Abstract—Low-Dropout Regulators (LDOs) are used to power noise sensitive applications. Power Supply Rejection (PSR) is a performance metric that measures the LDO’s ability to reject noise. Improving PSR has been the focus of many research groups. However, the state of the art does not recognize the best PSR enhancement schemes and collate them under comparable grounds. Further, the pass transistor’s diode connection (through the Gate-Drain capacitance) impacts the PSR, and this effect is not quantified in the state of the art. This research aims to bridge these gaps first by explicating the constitution of a high PSR LDO. Then, the impact of the pass transistor’s parasitics on PSR are quantified. Following this, the best state of the art PSR enhancement schemes are analyzed and simulated over a high-PSR core under similar conditions. This study reveals the strengths and limitations of each scheme, which unfolds each technique’s applications. Results convey that the LDO Filter yields the best PSR improvement at low frequencies, Series feedback at mid frequencies, and RC filter at high frequencies. Assessment concludes that Series Feedback provides the best compromise with respect to PSR enhancement.

Index Terms—Analog, LDO, Linear Regulators, Power supply rejection (PSR), SPICE

I. LDOs IN ANALOG SYSTEMS

Supplying and regulating power is fundamental to the operation of electric systems. The wide range of applications from Portable electronics, Defense applications, microsensors, Automotive electronics, etc. cannot sustain themselves without energy, and cannot function without a stable power supply [1].

Fig. 1: Typical Power-Supply System.

Switching regulators (SL) efficiently regulate power but have limited bandwidths, typically around 370 kHz [2]. They suffer from poor load dump responses, causing the supply voltage to droop in the event of a load step. SLs have large ripple at their outputs, which manifests as Power Supply noise. Digital loads (logic gates) are not very sensitive to such noise and can function optimally under such supply conditions. Analog loads such as ADCs, PLLs, Amplifiers, and Mixers are susceptible to supply ripple and require low noise power supplies.

In typical applications, a low-dropout regulator (LDO) is used in series with SLs to reject noise and provide a clean regulated voltage [1]. Characterized with higher bandwidths, LDOs respond faster to load disturbances, yielding smaller voltage droops in the event of load steps. The LDO’s regulated output can be used to power noise sensitive Analog loads. PSR is a measure of how much input ripple is suppressed by the LDO. Modern applications like medical imaging demand high PSR (>50 dB) [3], especially in mid frequencies (0.1–1 MHz), where SLs switch and induce noise. This has motivated researchers to investigate techniques to enhance the PSR of LDOs.

The State of the art presents numerous techniques to improve the PSR of LDOs [4–11], but fails to compare the best techniques under similar conditions. This work aims to bridge this gap by quantifying these effects both mathematically and graphically.

The purpose of this research is to first recognize the design factors affecting PSR and establish a high-PSR core LDO. This is covered in Section II. Sections III and IV present the best State of the art techniques that improve PSR. These techniques are applied as layers of concepts over the established core, and SPICE simulations reveal the PSR improvements. The highlighted strengths and limitations assist in assessing the conditions under which the said techniques offer maximum benefits. Section V compares the techniques discussed in this work, followed by Conclusions in Section VI.

II. HIGH-PSR CORE

An LDO with high PSR is essential to reject supply noise generated by SLs. Fig. 2 depicts a typical LDO consisting of an Error Transconductor (GE) and a low output impedance Buffer (AB) that close a negative feedback loop around pass transistor MP. This loop is stabilized, the output voltage (vo) is established as a function of the reference voltage (VR) and the feedback resistors (RFB1, RFB2). Implementing MP using PMOS transistors results in low dropout voltages when compared with NMOS pass transistors. Further, a replica LDO topology [13] offers a more predictable stability response, but suffers from poor load regulation due to the unregulated loading [14]. Thus, a single transistor MP is suitable.

Fig. 2: Typical LDO composition.
A. Loop Gain

The LDOs loop gain depicted in Fig. 3 can be analyzed by considering the poles/zeros established at each node. Each node contributes to a pole whose frequency is given by the RC frequency associated with that node, giving rise to poles pDC, pBO, and pO. Further, the current limiting effects of RC (ESR of CO) and resistance Re establish zeroes (ZE, zo) with their respective capacitances that boost phase margins. The DC loop gain (ALGO) and the output impedance (RO) can be expressed as:

\[ A_{LGO} = G_{E} R_{EO} A_{B} B_{mP} R_{0} \left( \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \right), \]  \hspace{1cm} (1)

\[ R_{O} = (R_{FB1} + R_{FB2}) |I_{fDSP}|, \]  \hspace{1cm} (2)

Fig. 3: LDO’s Loop gain plot depicting poles and zeroes.

With a single pole roll-off, the unity gain bandwidth (f0dB) is the product of the DC loop gain and the location of the dominant pole pD. Depending on the location of the dominant pole, LDO designs could be either output stabilized (pD = pO) [15,16] or internally stabilized (pD = pE) [17,18] :

\[ f_{0dB} = A_{LGO} p_{D} \big|_{p_{D} = p_{E} \ (or \ p_{O})}. \]  \hspace{1cm} (3)

The PSR performance of output and internally stabilized designs are vastly different, and this will be evident in the following sub-sections.

B. Gate Ripple

Since MP is a PMOS, and the input ripple is connected to MP’s source, it is desired to replicate this ripple at MP’s gate to ensure that there is no small signal source-gate voltage. This ensures that there is no noise injection through the gm currents of MP.

There are two ways of replicating the input ripple at the gate:

1. Feed-Forward path

The input ripple is injected to the gate of MP by using a feed-forward path [8,9] as shown in Fig. 4.

Transconductor GfF closes a negative feedback loop around MFF. This loop holds MFF’s source at ac ground, generating feed-forward current if. This feed-forward current is injected into the output of the buffer, and under the condition that RG=RB0, it impresses a voltage at vvo given by:

\[ v_{vo} = i_{f} R_{BO} = \left( \frac{v_{in}}{i_{f}} \right) R_{BO} = v_{in}. \]  \hspace{1cm} (4)

The bandwidth of this loop (fB) should be much greater than the Buffer pole pBO to ensure that the feed-forward path does not hinder the ripple replication until pBO shunts.

2. Current mirror

The other method to replicate supply ripple is to utilize the current mirror in the error transconductor (GE) [1]. Fig. 5 shows the Differential stage of the error transconductor feeding a P-type current mirror, with its equivalent small signal model.

![Figure 5: Supply Noise replication through current mirrors.](image)

The fraction of input ripple (v_in) reaching the output of the error transconductor (v_eo) is denoted by A_DD, and can be calculated by applying superposition:

\[ A_{DD} = \frac{v_{eo}}{v_{in}} = \frac{v_{in} R_{D}}{R_{D} + r_{ds4}} + i g_{34} (R_{D}) |r_{ds4}|, \]  \hspace{1cm} (6)

\[ \frac{v_{eo}}{v_{in}} = \frac{v_{in} R_{D}}{R_{D} + r_{ds4}} + \left( \frac{1}{g_{m3}} + R_{D} \right) |r_{ds4}| \approx 1. \]  \hspace{1cm} (7)

This indicates that the P-type mirror replicates the positive supply ripple at veo and this ripple can propagate to the gate of MP through the buffer AB. This technique is superior to the feed-fw technique since it eliminates the need for additional circuitry, that imposes its own bandwidth and gain constrains, in addition to power consumption. Thus, the designs discussed in this work will use a P-type mirror to replicate supply ripple.

C. PSR

PSR is the inability to amplify supply noise and can be analyzed as the reciprocal of the supply gain (A_IN) [19]. Fig. 6 depicts the voltage divider model of supply gain, where the supply gain is the fraction of the input ripple that reaches the output.

![Figure 6: Voltage divider model of A_IN.](image)

\[ A_{IN} = \frac{1}{PSR} = \frac{v_{o}}{v_{in}} = \frac{Z_{FB} |Z_{B}|}{Z_{T}}. \]  \hspace{1cm} (8)

Z_GP factors the noise coupling effects of MP’s diode connection through CGDP. From the perspective of the output node, the network of CGSP, CGDP, and RBO presents a voltage divided 1/gmP impedance to the supply that decreases with operating frequency (f0). This impedance overwhelms rdsP at frequency fGP1. ZGP keeps decreasing until fGP2 where the effects of RBO disappear, and ZGP flattens out as per (11). Fig. 7(a) depicts the effective impedance ZT as a function of frequency.

\[ Z_{GP} = \frac{1}{g_{p}} = \frac{1}{A_{p}} \left( \frac{1}{sC_{SP}} + \frac{1}{sC_{GDP}} \right), \]  \hspace{1cm} (9)

\[ Z_{GP} |_{0} \approx \frac{1}{r_{dsP}} \approx \frac{1}{g_{mp}} \left( \frac{1}{sC_{SP}} \right) \frac{1}{1} \approx \frac{1}{r_{dsP}}. \]  \hspace{1cm} (10)

fB = A_{BLG} p_{G} \gg p_{BO} p_{G} - \frac{1}{2 R_{PP} s C_{PP}}. \]  \hspace{1cm} (5)
Z_{FB} \approx \frac{C_{GDP} + C_{GSP}}{g_{mp}C_{GDP}}, \quad (11)
\]

\[
Z_{FB} = \frac{1}{g_{mp}R_{E0}A_{B}} = \frac{1}{g_{mp}}, \quad (14)
\]

\[Z_{FB} \text{ captures the effects of shunt feedback at the output of the LDO. At low frequencies, } Z_{FB} \text{ dominates the parallel combination described by (8), resulting in very low } A_{IN} \text{ (and thus, high PSR). As } f_{0dB} \text{ is approached, the effects of shunt feedback disappear, and the supply gain is a function of the external filter components connected at the LDOs output.}
\]

Fig. 7(b) shows the supply gain plots of internally and output stabilized LDOs across frequency. Crossing the dominant pole of the output stabilized design (pO) has no effect on Z_{FB} as per (14), and A_{IN} remains constant. However, crossing the dominant pole of the internally stabilized design (p’O) increases Z_{FB}, and due to this A_{IN} increases beyond p’E.

\[Z_{FB} \approx C_{GDP} + C_{GSP} \approx \frac{1}{g_{mp}C_{GDP}}, \quad (12)
\]

Beyond f_{GP2}, the decreasing Z_{FB} and instability for CF, which is beyond which the noise Z_{GP} couples is constant. Pushing f_{CP2} to higher frequencies helps improve A_{IN}. Without parasitic coupling, this effect is not seen. Instead, Z_{CO} overwhelms Z_{FB} and improves A_{IN} near f_{0dB}.

Beyond f_{GP2} and f_{0dB}, the shunted C_{O} (pO) decreases A_{IN} until zO, at which point R_{C}’s current limiting effects flatten A_{IN}. At f_{0dB}, the output stabilized design offers much lower A_{IN} since pO has shunted, and thus the supply noise has a low impedance path to ground. However, the output pole (p’O) of the internally stabilized design has not shunted at f_{0dB}, and hence offers a higher A_{IN}. Thus, an output stabilized design is desired.

Thus, the established high-PSR core is an output stabilized design with the gate ripple replicated with the help of the P-type current mirror in the error transistor. This core establishes the grounds on which the PSR enhancement techniques discussed in the next sections can be compared.

### III. PRE-FILTERED INPUT

In this section, three techniques are presented which improve the PSR of the LDO. These techniques are applied as layers of concepts over the core that was established in the previous section. Fig. 8 shows the schematics of the three pre-filter techniques, and Fig. 11 shows the simulations of the improved supply gains (A_{IN}) of the LDO upon applying these techniques.

![](Fig. 8: (a) RC, (b) LDO, and (c) CP-NMOS Pre-Filter.)

**A. RC Filter**

This technique uses a simple RC filter to clean up the supply ripple before it reaches the input of the LDO [4]. The cutoff frequency of this filter adds a pole in the supply gain response of the high-PSR core as shown in Fig. 11. The cutoff frequency is chosen to be a decade below f_{0dB} of the core:

\[P_{RC} = \frac{1}{2\pi R_{C}C_{F}} = \frac{f_{0dB}}{10}. \quad (15)\]

A low resistance of R_{F} is desired to minimize static power. This yields a large off-chip capacitor of 1.6 μF for C_{F}, which is a limitation. The ESR of C_{F} establishes a zero (R_{GC}) that flattens the A_{IN} response, and this limits the maximum improvement attainable. The other limitation relates to headroom—the voltage drop across R_{F} adds with the dropout voltage of the core, increasing effective dropout (V_{DO}).

**B. LDO Filter**

This technique cascades two LDOs in series [4]. The filtering regulator LDO_{F} shields the core from the supply ripple. LDO_{F} can be made on-chip, thus requiring an internally stabilized design. This can be designed as a Transconductor (G_{E(F)}) closing a negative feedback loop around pass transistor M_{P(F)}, establishing the dominant pole at the gate of M_{P(F)} (p_{BO(F)}). The unity gain frequency (f_{0dB(F)}) of LDO_{F} is:

\[f_{0dB(F)} = \frac{G_{E(F)}R_{mp(F)}R_{O(F)}}{2\pi C_{P1(F)}}. \quad (16)\]

The design can be approached taking care that f_{0dB(F)} and A_{LG0(F)} should be at least equal to the core’s parameters. This ensures that LDO_{F} effectively shields the core at least until f_{0dB} is reached. These yield G_{E(F)} of 200 μS and R_{E0(F)} of 250 kΩ. As seen in Fig. 11, this technique drastically improves the supply gain at lower frequencies. Being an internally stabilized design, A_{IN} of LDO_{F} degrades beyond the dominant pole p_{BO(F)}, thus degrading the supply gain of the cascaded pair.

Near and beyond f_{0dB(F)}, this technique provides little to no improvement in A_{IN}. Increasing f_{0dB(F)} to orders of magnitude higher than f_{0dB} would present its own design challenges as parasitic poles would jeopardize the stability of LDO_{F}. Since two LDOs are in series, this technique also increases dropout.

**C. Charge-Pumped NMOS Filter**

In [5], an NMOS device was used to cascode the LDO. The gate of the NMOS was biased using an RC filter connected to the input supply. This source follower configuration shields the core from input ripple similar to the RC filter discussed earlier. The RC filter does not dissipate static power, so the resistance can be made large. The drawback is that the dropout is a Gate-Source voltage (500-600mV) above the dropout of the core.
An improvement to this technique is presented in [6]. As shown in Fig. 8(c), a Charge pump of N stages is used to boost the gate drive of the cascode transistor \( M_C \). The effective dropout voltage is a \( V_{\text{DSC(SAT)}} \) above the dropout of the core. \( R_{\text{CPF}} \) and \( C_{\text{CPF}} \) maintain the role of the RC filter to clean up supply ripple. To keep \( M_C \) in the saturated inversion region,

\[
V_{\text{DSC}} = (N + 1)V_{\text{IN}} - 2N\Delta V_{\text{Diode}} - V_{\text{IN}'},
\]

\[
V_{\text{DSC}} = V_{\text{IN}} - V_{\text{IN}'} \geq V_{\text{GSC}} - V_{\text{TNO}},
\]

\[
V_{\text{IN}} < 2V_{\text{Diode}} + \frac{V_{\text{TNO}}}{N}.
\]

This imposes a maximum input voltage constrain. If \( V_{\text{IN}} \) increases beyond this limit, \( M_C \) enters linear region, and the noise from \( V_{\text{IN}} \) directly couples to the input of the LDO. Thus, a single stage charge pump is chosen. Width of \( M_C \) can be designed from choosing \( V_{\text{DSC(SAT)}} \) of 250 mV that yields \( W_C \) of 15 mm. The pole of the RC filter can be chosen to be a decade below \( f_{0dB} \), similar to (15).

The supply gain simulations reveal that while the diodes in the charge pump and the RC filter do filter the input ripple, the input ripple couples to the gate of \( M_C \) \( (V_{ge}) \) through the large gate-drain capacitance \( C_{\text{GDC}} \) of \( M_C \):

\[
V_{ge} = \frac{C_{\text{GDC}}}{C_{\text{GDC}} + C_{\text{CP}}}.
\]

\( M_C \) has a large width and consequently a large \( C_{\text{GDC}} \) of 10pF. This capacitive coupling leads to a large fraction of input ripple being coupled to \( V_{V_{ge}} \) and source follower \( M_{CP} \) replicates this ripple to the input of the core. This yields a minor supply gain improvement (5-6 dB), as depicted by Fig. 11.

The limitations stem from the noise coupling nature, making it unsuitable for high load current applications. Larger loads demand a larger \( W_C \), which increases \( C_{\text{GDC}} \) (and noise coupling), thus decreasing the improvement in \( A_{IN} \). The other limitation is the maximum input voltage constrain induced by the Charge pump mechanism. Finally, the dropout is increased by \( V_{\text{DSC(SAT)}} \) [6] were able to obtain 30 dB of improvement using this technique, reaching 70 dB of PSR at DC. This high improvement is mainly due to the lower target load current.

### IV. SERIES FEEDBACK

The Series feedback (SFB) technique [7] can improve supply gain at mid-high frequencies, without dissipating additional ohmic losses or increasing \( V_{\text{DO}} \). As seen from Fig. 6, lower \( A_{IN} \) can be achieved either by decreasing \( Z_{EB} \), or by increasing \( Z_I \). The LDO’s shunt feedback action already decreases \( Z_{EB} \) in the low-mid frequencies. Extending the frequency range where \( Z_{EB} \) remains low can compromise stability due to parasitic poles. This technique introduces a high frequency series sampling loop that increases the impedance presented to the supply \( (Z_E) \). Fig. 9 depicts the LDO with series feedback.

Transconductor \( G_1 \) and the high pass filter \( (R_{FI}, C_{FI}) \) close a series sampling loop \( (I \text{ loop}) \) around \( M_p \). Note that the series sampling action can be implemented with a mirror PMOS \( (M'_p) \) that is scaled down in size, in series with a sense resistor.

The I loop gains maximum strength based on the cutoff frequency set by the high pass filter \( (p_{BO}) \), chosen to be a decade below the core’s unity gain frequency. The peak loop gain of the I-loop \( (A_{LG(I)(\text{MAX})}) \) is chosen to be 30, and is given by:

\[
A_{LG(I)(\text{MAX})} \approx G_{R_E}R_{BD}.
\]

After attaining the peak value, the loop gain of the I-loop rolls off after \( p_{BO} \) shunts as shown in Fig. 10(a). The loop gain of the outer loop \( (V \text{ loop}) \) that establishes \( V_O \) as a function of \( v_{gc} \) and \( v_{in} \) is also shown. The 0-dB crossing point of the I loop creates a pole \( (p_i) \) in the V loop, which affects \( f_{0dB} \) (60 kHz) and Phase Margin (40°) of the V loop.

Fig. 10(b) depicts the plot of \( A_{IN} \) for the SFB LDO. Due to the effects of \( Z_G \), \( A_{IN} \) increases beyond \( f_{GP1} \) until \( f_{0dB} \). Beyond \( f_{0dB} \), the combined effects of the shunting output capacitor and the increasing strength of the I loop decreases \( A_{IN} \), resulting in a “peaking” effect around \( f_{0dB} \). Once \( A_{LG(I)(\text{MAX})} \) is reached, \( A_{IN} \) flattens. After \( p_{BO} \) shunts, \( f_{GP2} \) is reached and \( R_C \) current limits \( C_O \), \( A_{IN} \) increases, and joins the core’s response at \( f_{0dB} \).

### V. COMPARISON

This section presents a comparison of the various PSR enhancement techniques. Fig. 11 shows the \( A_{IN} \) plots for each technique, and Table 1 provides a quantitative comparison. The LDO filter drastically improves PSR at low frequencies but starts degrading towards the mid-high frequency range. The RC filter utilizes a large off-chip capacitor to improve PSR at high frequencies. The CP-NMOS provides little improvement in PSR due to the noise coupling through parasitics of the large cascading NMOS. Series-FB improves PSR in the mid-high frequency range without compromising \( V_{\text{DO}} \), but at the expense of reduced \( f_{0dB} \) and little quiescent power \( (P_{G}) \) consumed by \( G_1 \).
VI. CONCLUSIONS

This work establishes a high PSR core, investigating the effects of the pass transistor’s diode connection which the state of the art did not account for. By analyzing and simulating the best PSR enhancement techniques in the state of the art, improvements in PSR are revealed, elucidating their potential use cases. The LDO filter provides the best PSR improvement at low frequencies, Series-FB at mid frequencies, and RC filter at high frequencies. Improving PSR (>25 dB) without sacrificing dropout and with little additional power consumption makes Series-feedback utilizing a PMOS current mirror the best compromise with respect to PSR enhancement. Charge pumped NMOS regulators operate in a source follower configuration, and will exhibit frequency spurs at the regulator’s output near and around the Charge pump’s frequency, making PMOS based LDOs with Series feedback superior in performance.

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