Designing Low-Loss Single-Inductor Multiple-I/O (SL–MI/O) CMOS Power Supplies

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***Abstract*—Switched-inductor power supplies are valued for their high efficiency despite the bulkiness of off-chip inductors. When designing compact systems, like many portable consumer electronics and wireless microsensors, single-inductor topologies are preferred. Specifically, single-inductor multi-input and multi-output (SL–MI/O) power supply designs pose unique challenges that have yet to be fully addressed. This paper aims to provide design guidelines for maximizing efficiency in the design of SL–MI/O systems, especially in the sub-5W domain. To simplify the choice between NFETs and PFETs for the multitude of power switches in SL–MI/Os, which is not straightforward, an intuitive metric called the Favorability Index (F_{NP}) is proposed. A new, optimal supply voltage theory is also presented, suggesting that the most efficient voltage to supply power switches' gates is around twice the threshold voltage (v_T). The paper also proposes using dynamic selectors in gate drivers. This allows for blocking cross conduction without increasing v_{SUP} drastically, ensuring efficiency. A two-transistor selector is recommended as a simple implementation, and the tradeoffs are discussed. An example topology is designed using guidelines proposed by the paper to demonstrate the design flow and efficiency improvements.**

***Index Terms*—Multiple I/O, DC-DC converter, switched inductor, optimal supply, favorability index, switching loss, CMOS, SIMIMO, gate driver, efficiency, power loss.**

I. Switched-Inductor Multiple-I/O Power Supplies

SWITCHED-INDUCTOR power supplies are widely used in electronics [1] due to their high efficiency. The prevalence of microelectronics, such as portable electronics and Internet-of-Things (IoT) devices [2], emphasizes the need for higher power density. Consequently, it is preferred to use as few bulky off-chip components as possible, motivating single-inductor power supply designs.

As electronics grow in complexity, the necessity for power supplies to generate multiple voltages rises [3]–[5], calling for multiple-output designs. Similarly, systems with diverse input sources, such as battery-powered or energy-harvesting systems, necessitate multiple-input designs [6]–[8]. Some systems require both multiple inputs and outputs [9]–[11]. This paper refers to all of the above as Single-Inductor Multiple-Input/Multiple-Output (SL–MI/O) designs.

A general SL–MI/O system diagram with input one (v_{I1}) to input N (v_{IN}) and output one (v_{O1}) to output N (v_{ON}) is depicted in Fig. 1. It can be observed that inductor switching nodes v_{SWI} and v_{SWO} connect to many different voltages through a multitude of switches. This introduces design complexities that are not present in single I/O systems.

Bucking high inputs to low outputs requires the input ground switch S_{IG} in Fig. 1 and boosting low inputs to high outputs requires the output ground switch S_{OG} [12]. And while the highest and lowest I/Os should use PFETs and NFETs, respectively, intermediate levels can use either or both.

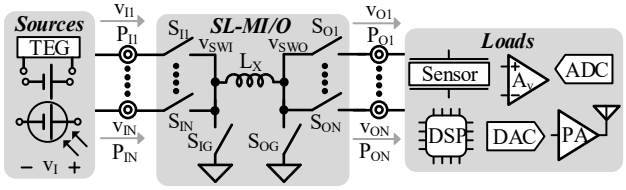

Fig. 1. Switched-inductor multiple-I/O system diagram.

Selection between using an NFET or a PFET for any I/O switch becomes nontrivial. The designer needs to find the most efficient NMOS design among all possible combinations of gate drive voltages and widths. Then the same process needs to be repeated for PMOS, and the results compared. The number of switches to design and the multitude of voltage rails exacerbate the long design process and obscure insights.

With multiple I/O voltages available to use as gate drive supplies, we also want to easily find the most power-efficient voltages to drive the switches. In this paper, an optimal supply theory is derived to aid designers. For sub-5W systems, using a lower gate drive voltage at around twice the threshold voltage (v_T) but wider switches is practical and more efficient.

Furthermore, the complex switching voltages at inductor nodes that can cause unwanted turn-ons of switches (cross conduction). Common methods to block this cross conduction can be inefficient. This paper proposes a low-loss gate driver design alternative that is simple and can block cross conduction efficiently. Designs like hybrid/switched-capacitor power supplies or charge pumps may also experience similar cross conduction [13], making the insights discussed in this paper relevant for a broader range of designs.

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In Sec. II, an analysis of MOSFET selection is presented. The power losses are explicated, and the Favorability Index (F_{NP}) is introduced as an intuitive metric to aid designers. Sec. III proposes and validates the optimal supply theory. Sec. IV introduces the low-loss gate driving scheme, and Sec. V showcases the design flow using concepts of this paper with an example circuit. The paper is concluded in Sec. VI.

II. Favorability Index

A. Theory

The design of power switches is usually governed by losses; control loops are usually ones that determine response time. When designing a power I/O switch, the first consideration is choosing between an NFET and a PFET. Intuitively, one can examine the possible gate drive (overdrive) voltages (v_{GST}) of the two choices to find the less resistive choice, since higher v_{GST} lowers resistance, and therefore lowers the ohmic loss (P_R). However, a higher v_{GST} is not necessarily better, since it also increases gate-charge power loss (P_G).

Hence, during MOSFET selection, it is essential to evaluate all losses at the optimal design point. Then the optimal total losses (P_M') of NMOS and PMOS options should be compared. Because the choice with higher P_R may exhibit lower P_G, and the sum is not necessarily greater.

In this paper, the terms $v_{DD/SS}$ refer specifically to the high-side and low-side gate driver supply voltages for each switch, not global supply rails. The v_{SS}/v_{DD} of an N/PMOS switch is always connected to its source voltage (v_S) unless explicitly stated otherwise. That is because an NFET turns off (the switch opens) when v_{GS} collapse to zero, when the gate voltage v_G drops to v_S. Similarly, a PFET turns off (the switch opens) with collapsed v_{SG}, when v_G rises to v_S. There's no need to drive the v_{GS}/v_{SG} for N/PFET to below zero since the switch is already off, and further gate driving incurs loss.

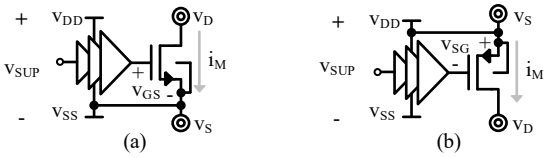

Fig. 2. Power I/O (a) NMOS and (b) PMOS switch.

To derive the losses, we need to first define the effective supply voltage (v_{SUP}). Normally, v_{SUP} is the same as v_{DD} since v_{SS} is usually zero. However, complex voltage rails are common in SL–MI/O designs, and such generalization is not always applicable, so we need to explicitly define:

$$v_{SUP} = v_{DD} - v_{SS}. \tag{1}$$

The on-resistance R_M is calculated in deep triode since that is the operating region of power switches. $v_{DD/SS}$ needs to be selected such that v_G can drive the switches into triode reliably. k_R and k_G can be defined as coefficients to simplify presentations for insight. P_R and P_G can then be derived [12]:

$$\begin{aligned} P_R &= {i_{L(RMS)}}^2 R_M d_{ON} \\ &= \frac{{i_{L(RMS)}}^2 L_M d_{ON}}{K_{N/P}'\left(\left|v_{SUP} - v_T\right|\right) W_M} \equiv \frac{k_R}{K_{N/P}'\left|v_{GST}\right| W_M}, \end{aligned} \tag{2}$$

$$\begin{aligned} P_G &= v_{SUP} q_G f_{SW} \\ &= v_{SUP}\left[C_{OL}\left(2v_{SUP} + \Delta v_{SW}\right) + C_{CH}\left(v_{SUP} + \frac{V_{T0}}{3}\right)\right] f_{SW} \\ &\approx C_{EQ} {v_{SUP}}^2 f_{SW} \equiv k_G {v_{SUP}}^2 W_M. \end{aligned} \tag{3}$$

$i_{L(RMS)}$ is the RMS inductor current, $K_{N/P}'$ is the transconductance parameter, W_M is the channel width, and f_{SW} is the switching frequency. v_T is the threshold voltage with body effect. q_G is the charge needed to charge the gate across v_{SUP}. d_{ON} is the active duty cycle. C_{EQ} is the equivalent approximate gate capacitance. C_{OL} and C_{CH} are the overlap and channel capacitance. L_M is the entire channel length, L_{CH} is the effective channel length and L_{OL} is the overlap length:

$$L_M = L_{CH} + 2L_{OL}. \tag{4}$$

Power switches lose ohmic IV overlap power P_{IV} when transitioning between on and off states, as the current and voltage across the switch crisscross between extreme levels. In consumer microelectronics with sub-5W power, P_{IV} is usually lower than P_R and P_G by at least an order of magnitude. The losses among the gate driver stacks themselves (excluding P_G of the power switch) are also low, since the drivers don't need to be strong to minimize P_{IV}. The overall MOSFET loss (P_M) is therefore approximately the sum of P_R and P_G:

$$P_M \approx P_R + P_G. \tag{5}$$

P_M is a function of a lot of parameters, but when we design a power switch, the parameter we control is primarily the width W_M. Since P_R in (2) is inversely proportional to W_M, and P_G in (3) scales with it linearly, there is an optimal W_M' at which point the loss is at the minimum [12]. We can write:

$$\begin{aligned} \left.\frac{\partial P_M}{\partial W_M}\right|_{W_M'} &= \left.\frac{\partial P_R}{\partial W_M}\right|_{W_M'} + \left.\frac{\partial P_G}{\partial W_M}\right|_{W_M'} \\ &= -\frac{k_R}{K_{N/P}' v_{GST} {W_M'}^2} + k_G {v_{SUP}}^2 = 0, \end{aligned} \tag{6}$$

and therefore

$$W_M' = \sqrt{\frac{k_R / k_G}{{v_{SUP}}^2 K_{N/P}' v_{GST}}}. \tag{7}$$

This W_M' is the optimal width that the switch should be designed at for the lowest loss. In higher-power domains it might not be practical, due to (7) giving very big values that are not achievable with area constraints, or due to P_{IV} becoming the dominant switching loss (which we approximated away). But in microelectronics with sub-5W power, W_M' is accurate and practically achievable.

In order to find W_M', we have to know the constants inside k_R and k_G, such as f_{SW} or $i_{L(RMS)}$. Therefore, W_M' is optimized at one current level. Normally, we can optimize the switch at half the load level, such that the efficiency is centered across

possible load conditions, or optimize it at the most likely load level. If conditions allow and we can sense the output power or currents, we can also segment the switch into multiple parallel MOSFETs to modulate W_M based on the current and keep it approximately W_M' to maximize efficiency.

At W_M', P_M reaches the minimum at P_M'. We can find P_M' by plugging W_M' back into (5) to get:

$$P_M' = P_R' + P_G' = 2P_{R/G}' = 2\sqrt{\frac{k_R k_G v_{SUP}^2}{K_{N/P}' v_{GST}}} \equiv 2\sqrt{\frac{k_T}{k_B}}. \quad (8)$$

k_T and k_B are coefficients defined here only for simpler presentations of derivations later. P_M' is the optimal loss that should be calculated and compared for both NMOS and PMOS switches to justify the choice between them. However, calculating P_M''s of NFETs vs. PFETs for every switch location is tedious for designs with many I/Os. It also lacks insight, which complicates a designer's design process.

A favorability index F_{NP} can be defined to help with MOSFET selection. F_{NP} is the ratio of a switch's P_M' when it is implemented as a PFET versus an NFET. Since it's a ratio of P_M', it takes into account all losses in P_M, including the conduction loss and gate-charge loss. A value of F_{NP} greater than one indicates a lower power loss in an NFET, favoring its use. Conversely, a value smaller than one favors PFETs.

$$F_{NP} \equiv \frac{P_{MP}'}{P_{MN}'} \approx \sqrt{\left(\frac{v_{SUPP}}{v_{SUPN}}\right)^2 \left(\frac{K_N'}{K_P'}\right)\left(\frac{v_{GST}}{v_{SGT}}\right)}. \quad (9)$$

Many variables like f_{SW} and $i_{L(RMS)}$ cancel in F_{NP}, since it's the same switch, and non-dominant terms are approximated away to get (9). For example, the approximated result in (9) assumed that the overlap capacitance and oxide thicknesses between N/PFETs are similar. If they're significantly different, the accurate ratio equation defined in (9) must be used, instead of the approximation. However, even in this case, F_{NP} remains useful for estimation and intuition.

Eq. (9) is derived when the W_M of the switch in question is designed at W_M' for all currents. If the system can only allow one fixed width for the switches, we can only optimize them for one current level, I_{M0}. F_{NP} therefore becomes a function of the current through the switch, i_M, because k_R in W_M''s no longer cancel out when W_M is not W_M' for different i_M's.

However, if the switch is designed at the optimal width W_{M0}' for I_{M0}, at which point $P_{MRN/P0}' = P_{MGN/P0}'$, we can derive in (10) that $F_{NP(S)}$ for fixed width remains constant across i_M. Therefore, F_{NP} remains valid even for fixed-width switches as long as they're sized at W_{M0}' for an I_{M0}. This is an important point because not all systems can employ strategies like segmentation to track W_M to W_M' for all current levels.

$$F_{NP(S)} = \frac{i_M^2 \frac{P_{MRP0}'}{I_{M0}^2} + P_{MGP0}'}{i_M^2 \frac{P_{MRN0}'}{I_{M0}^2} + P_{MGN0}'} = \frac{\frac{P_{MP0}'}{2}\left(\frac{i_M^2}{I_{M0}^2}+1\right)}{\frac{P_{MN0}'}{2}\left(\frac{i_M^2}{I_{M0}^2}+1\right)} = \frac{P_{MP0}'}{P_{MN0}'}. \quad (10)$$

In (9), we can see that a higher K′ and $v_{GST/SGT}$ for a MOSFET type favors it, but a higher v_{SUP} disfavors it with a higher order. If all conditions are equal, an NFET is always better due to its higher carrier mobility. For switches connected to the lowest/highest voltage in the system, F_{NP} is infinite/0. These are already obvious without F_{NP}; but for intermediate voltages, F_{NP} becomes very useful. It can also be observed that F_{NP} changes with voltages, not with currents.

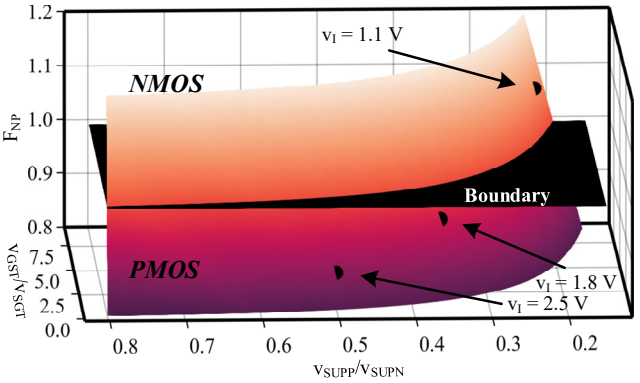

Fig. 3. Calculated favorability index with data points for Sec.II.B.

An example of the different W_M''s of NMOS and PMOS versions of the same switch is plotted below in Fig. 4. The circuit for which this is plotted is presented in the next subsection in Fig. 5. Due to inherently higher carrier mobility, NFET can be smaller. In the example circuit shown in Fig. 5, v_{SGT} is also smaller than v_{GST}, making the difference even more pronounced. However, the PFET can still be more efficient with lower v_{SUPP} thus lower P_G, even with the significantly bigger size, as we'll see in the next subsection.

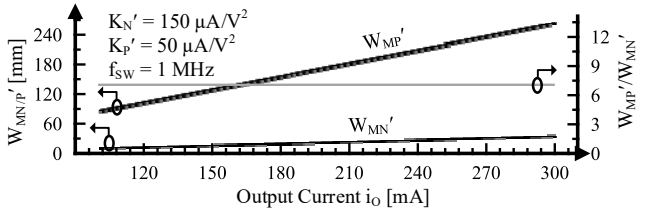

Fig. 4. Calculated W_M' of NMOS versus PMOS switch across i_O.

B. Validation

To see how F_{NP} is applied, we can validate the theory in simulation with a simple buck converter with 1.8 V input, 1 V output, an external 5 V rail, and a nominal load current of 200 mA, as shown in Fig. 5. A buck topology has two switches, the ground switch is connected to the most negative voltage in the system, and it has to be an NFET. For the input switch M_I, we can use F_{NP} to find the optimal choice.

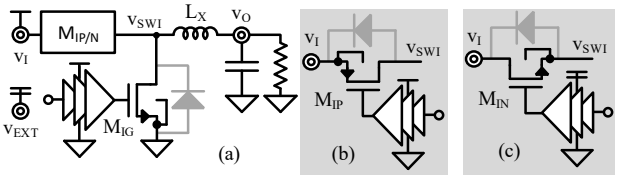

Fig. 5. (a) Buck and (b)-(c) power PMOS and NMOS input switches.

From (9) we can calculate the F_{NP} to be 0.94, which means a PMOS input switch is slightly favored. v_{SUPP} is 1.8 V, v_{SUPN} is 5 V, v_{GST} is 2.5, v_{SGT} = 1.1, K_N'/K_P' is 3. The system is simulated, and the losses incurred by M_I are recorded. The difference between the NMOS loss and PMOS loss, $\Delta P_{MN/P}$, is plotted in Fig. 6. The solid line is the result when the W_M is kept at W_M' across all i_O. The dashed line is when W_M is statically designed at the optimal width $W_{M(200\,m)}$, when the current is 200 mA, and doesn't vary with i_O.

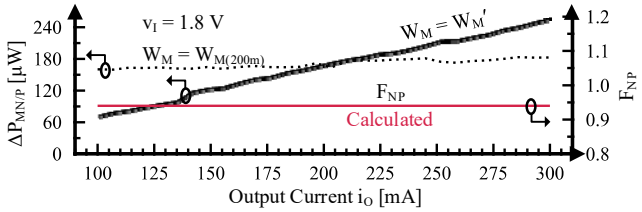

Fig. 6. Simulated N/PMOS loss difference and calculated F_{NP} across i_O.

$\Delta P_{MN/P}$ stays positive, showing that NMOS implementation incurs higher losses, validating the F_{NP} result across current. This is true for both when W_M' is always applied and when W_M is static, validating both (9) and (10). F_{NP} is 0.94 for both when W_M is W_M', or when W_M is $W_{M(200\,m)}$, due to (10).

In (9) and Fig. 6, we've shown that F_{NP} doesn't change across currents as long as we have W_M', or if W_M is designed at W_{M0}' for an I_{M0}. It changes, however, if $v_{GS/SGT}$ or v_{SUP} changes. For example, F_{NP} of the input switch M_I changes with v_I, the different F_{NP}'s at different v_I's are marked in Fig. 3. In a power supply, we usually have defined I/Os that do not change, while the current varies based on load. So F_{NP} only needs to be consulted once during design and remains valid. However, if the system has changing voltages, such as battery chargers, F_{NP} can vary across operating conditions.

We can validate F_{NP} across different input voltages as well. In Fig. 7, the approximated F_{NP} equation in (9) is plotted against the actual simulated input switch losses across v_I at 200 mA. The switches are again kept at W_M' across v_I. The F_{NP} matches the simulated crossing point with good accuracy with small error $v_{I(E)}$, even though only the approximated equation in (9) is plotted instead of the accurate expression.

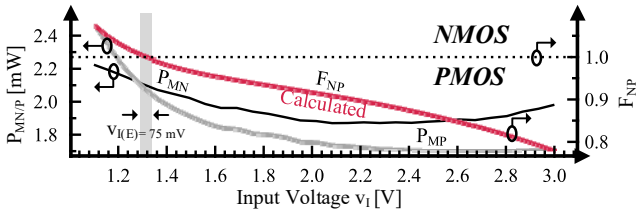

Fig. 7. Simulated N/PMOS loss difference and calculated F_{NP} across v_I.

C. State of the Art

In the state of the art, the selection of MOSFETs is a part of the design that is not discussed. For example, in [14]–[16], the MOSFET implementations are provided as is. Often times, the choice with higher gate drive $v_{GST/SGT}$ is assumed to be the better choice. Therefore, this paper provides another perspective and insight for this rarely discussed design step.

III. Optimal Supply

A. Theory

By observing (8), we can see that after applying W_M', P_M' is no longer a function of W_M, but of the system's parameters and also v_{SUP}. It is important to notice that P_M' does not increase or decrease monotonically with v_{SUP}. Just like the insight we discussed early in Sec. II, a higher v_{SUP} may imply lower P_R, but it also implies a higher P_G. Therefore, there's a sweet spot v_{SUP}'' at which point the overall loss is minimal at P_M''.

When we calculate F_{NP}, we must select and plug in the v_{SUP}'s correctly to approximate this optimal v_{SUP}'' if possible, otherwise we might not be approaching the actual optimal design. To find this optimal supply v_{SUP}'', we take a derivative of (8) with respect to v_{SUP} to find the minimum.

$$\left(\frac{\partial k_T}{\partial v_{SUP}}\right)k_B\Big|_{v_{SUP}''} - \left(\frac{\partial k_B}{\partial v_{SUP}}\right)k_T\Big|_{v_{SUP}''} = 0,$$

$$\rightarrow k_{R0}k_{G0}2v_{SUP}''K_{N/P}'v_{GST} - K_{N/P}'k_{R0}k_{G0}v_{SUP}''^2 = 0 \quad (11)$$

$$\rightarrow v_{SUP}'' = 2v_{GST} = 2\left(v_{SUP}'' - v_T\right)$$

We can derive v_{SUP}'' to be $2v_T$ from (11). It should be noted that the simple $2v_T$ result is derived from approximated equations in (3). The accurate k_G contains fractional v_{SUP} terms that represent gate-to-v_{SW} capacitance that is not fully charged across v_{SUP}. Therefore, the accurate expression is:

$$v_{SUP}'' = v_T + \sqrt{v_T^2 + k_S} \approx 2v_T, \quad (12)$$

where k_S denote small terms we approximated away. Eq. (12) deviates from $2v_T$ in either direction based on the Δv_{SW} as the switch is turning on. This results in the small discrepancy between v_{SUP}'' and $2v_T$ in Fig. 8. But it is still an accurate enough approximation that provides intuition and ease of use.

We can visualize this result in Fig. 8 by plotting P_M across widths and v_{SUP}'s, which are all the variables of a switch within the designer's control. We can find that the minimum is only reached when the switch has both the W_M' and v_{SUP}''.

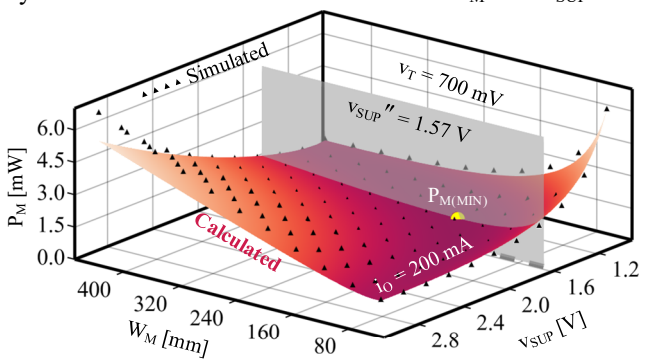

Fig. 8. Calculated and simulated plot of P_M versus W versus v_{SUP}.

Optimal supply theory of $2v_T$ is true no matter the current level, f_{SW}, mobility, etc., so long as W_M' is applied. We can repeat the plot in Fig. 8 at different current levels, shown in Fig. 9. As current changes, W_M' also changes, but v_{SUP}'' stays the same. In the case of a space-constrained design where W_M'

is not achievable, v_{SUP}'' would no longer be $2v_T$. Plugging in the constrained W_M into (11) and (13) yields it, but the result is the solution of a complex and unintuitive cubic function. Therefore, it will not be shown here. But it is still valuable to numerically solve it if needed for an efficient design.

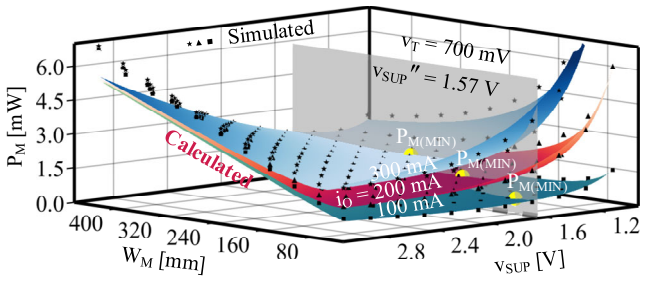

Fig. 9. Calculated and simulated P_M versus W and v_{SUP} at different currents.

With Clairaut's Theorem, we know that finding W_M' then taking a derivative of (8) to find v_{SUP}'' gives the same result as if we were to find v_{SUP}' then W_{M0}''. We can find the minimum more formally by taking the partial derivative of P_M with respect to both, then solving the system of two equations. By solving the system formed by (7) and (13), we can find v_{SUP}'' again as $2v_T$ with (14), which is the same as in (12).

$$\left.\frac{\partial P_M}{\partial v_{SUP}}\right|_{v_{SUP}'} = \left.\frac{\partial P_R}{\partial v_{SUP}}\right|_{v_{SUP}'} + \left.\frac{\partial P_G}{\partial v_{SUP}}\right|_{v_{SUP}'}$$
$$= -\frac{k_R K_{N/P}' W_M}{\left[K_{N/P}' W_M \left(v_{SUP}' - v_T\right)\right]^2} + 2k_G v_{SUP}' W_M = 0. \quad (13)$$

$$2k_G v_{SUP}'' \frac{k_R \left(v_{SUP}'' - v_T\right)^2}{K_{N/P}' k_G v_{SUP}''^2 \left(v_{SUP}'' - v_T\right)} = \frac{k_R}{K_{N/P}'}. \quad (14)$$

To determine whether v_{SUP}'' is the minimum or maximum, we can do the second derivative test and observe the Hessian matrix. And since the Hessian matrix is positive-definite from (15) and (16), v_{SUP}'' is the minimum. And at v_{SUP} bigger than v_T and W_M bigger than zero, it is the global minimal point.

$$H\left(v_{SUP}'', W_M''\right) = \begin{pmatrix} \frac{\partial P_M}{\partial^2 v_{SUP}} & \frac{\partial P_M}{\partial v_{SUP} \partial W_M} \\ \frac{\partial P_M}{\partial W_M \partial v_{SUP}} & \frac{\partial P_M}{\partial^2 W_M} \end{pmatrix}$$
$$= \begin{pmatrix} \frac{2k_R}{K_{N/P}' W_M'' v_T^3} + 2k_G W_M'' & \frac{k_R}{K_{N/P}' W_M''^2 v_T^2} + 4k_G v_T \\ \frac{k_R}{K_{N/P}' W_M''^2 v_T^2} + 4k_G v_T & \frac{2k_R}{K_{N/P}' W_M''^3 v_T} \end{pmatrix} \quad (15)$$

$$\det(H) = 16k_G^2 v_T^2. \quad (16)$$

With both W_M' and v_{SUP}'', we can find the absolute minimum P_M'' at both optimal points by plugging into (5):

$$P_M'' = 2\sqrt{\frac{k_R k_G \left(2v_T\right)^2}{K_{N/P}' \left(2v_T - v_T\right)}} = 4\sqrt{v_T \left(\frac{k_R k_G}{K_{N/P}'}\right)}. \quad (17)$$

However, this is not practically achievable, since we don't have granularity when it comes to the voltages we can use for v_{SUP}. It is usually selected from existing voltages in the system instead since it is generally not efficient to artificially generate a voltage rail just for gate drive. Therefore, in practice, v_{SUP} should be selected from existing I/Os to approximate v_{SUP}''.

So far, v_{SUP}'' is derived from equations that don't consider higher-order effects. But we need to reconcile the theory with devices with significant second-order effects, such as mobility degradation or LDMOS' velocity saturation in the drift region [17]–[19]. If the critical voltage (v_{CRIT}) where the conductivity degrades significantly is reached later than $2v_T$, then v_{SUP}'' is $2v_T$. But if reached earlier, usually in discrete high-voltage LDMOS devices, then the optimal v_{SUP}'' would become v_{CRIT}, since overdriving the MOSFETs above it offers no further benefit yet P_G increases quadratically:

$$v_{SUP}'' \approx \min\left(2v_T, v_{CRIT}\right). \quad (18)$$

B. Validation

We can validate the theory in simulation with the system described before in Fig. 5. We have no flexibility when choosing v_{SUP} for the input switch, since there's only one voltage higher than v_I in the system. But for the input ground switch M_{IG} we have the choice to either choose the 1.8 V input or the 5 V external rail as the v_{DD}. 1.8 V is chosen as the v_{DD} in Fig. 5 based on the optimal supply theory, achieving 29% lower loss compared to choosing 5 V gate drive.

In order to validate the theory, we can sweep the W_M and v_{SUP} of M_{IG} and record the losses that it incurs and plot them against the calculation in Fig. 8. It can be seen that the lowest loss is when v_{SUP} is 1.57 V, approximately $2v_T$, and width is at W_M'. We derived in Sec. III.A that v_{SUP}'' is independent of current levels as long as we have W_M'. Therefore, to validate this claim, the simulation in Fig. 8 is performed again at two different current levels. It can be seen that although the W_M' is different for different currents, the v_{SUP}'' always lands on the plane of $2v_T$, which validates our claim.

To validate our optimal supply theory with measurements, we measured the P_M of an NMOS output ground switch in an asynchronous boost. The input v_I is 1V, the duty cycle is 50%, and the output current is swept from 150 mA to 350 mA.

Since we were limited to discrete components, we cannot sweep the width with granularity. Therefore, we sweep the widths by parallelizing switches and sweeping the number of parallel switches to achieve the same effect. There are 8 parallel switches on the PCB, so if 4 switches in parallel has the optimal width, then we can show the effects of wider-than-optimal or narrower-than-optimal switches on P_M by putting more or less than 4 switches in parallel.

TABLE I

OPTIMAL SUPPLY MEASUREMENT COMPONENTS

Designator	M_1–M_8	GD_1–GD_8	D_1	i_{LD1}
Device	CSD19538Q2	UCC27517	STPS2H100A	PLZ164W

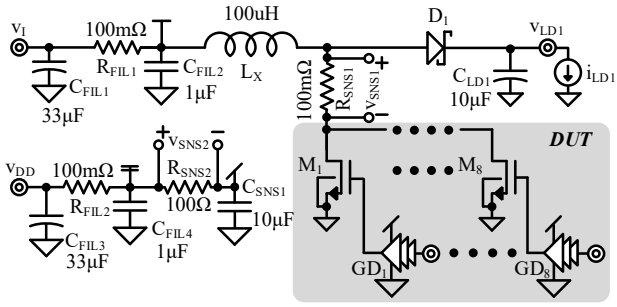

Fig. 10. PCB schematic for testing optimal supply.

Since the device is an LDMOS, there are higher-order effects that need to be accounted for. v_{CRIT} can be measured by putting the device in triode, sweeping v_{GS}, and measuring i_{DS}. We can find in Fig. 11 that the critical voltage is around 5.2 V. This means that v_{SUP}'' is 5.2 V for this switch according to (18), since 5.2 V is smaller than $2v_T$ of 7.8 V. This correlates with our minimal Λ_P point in Fig. 13.

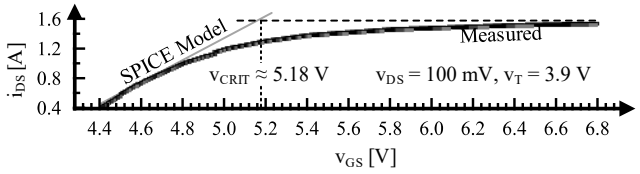

Fig. 11. Measured i_{DS} versus v_{GS} plot for a single discrete switch.

We can further validate the theory by generating a graph like Fig. 8 with measurement data. We sweep the width of the switch by soldering different numbers of the same switch in parallel and sweep the v_{SUP} by supplying the gate drivers with different voltages. We can find that the absolute minimal P_M'' is achieved at v_{SUP}'' of 5.2 V and W_M' of 4 parallel switches, which correlates with our theory.

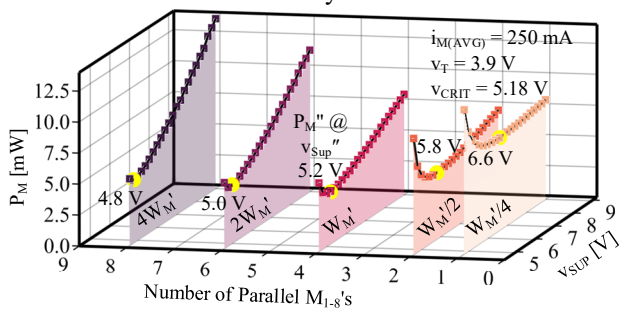

Fig. 12. Measured P_M across v_{SUP} and number of parallel switches.

To conduct the experiments, first the switches are characterized individually to find their v_T, v_{CRIT}, R_{ON}, and generate Fig. 11. Then 1–8 parallel DUT are soldered and switched in an open-loop manner with an FPGA. To measure v_{SUP}'', a control loop is not necessary. The current level that the measurements are conducted with is not chosen arbitrarily.

Being limited by discrete components, we have switches with widths that we cannot design for a specific power level. Therefore, to test our theory, which is based on the width being at W_M', we need to instead go backwards and find the current level at which point the width we have is optimal and do measurements under that condition. To aid us with this effort, we propose a new metric.

In a width-constrained design where W_M is fixed, it might be useful to know the current and v_{SUP} that this W_M is optimal for. We can derive a figure of merit (FoM) for a switch based on the fractional loss equation (19). Fractional loss is the ratio of power losses to input power, which is a common metric for measuring the efficiency of a power supply.

$$\sigma = \frac{P_Q + P_{DT} + P_{M1} + P_{M2} + \cdots + P_{MX}}{P_I}. \tag{19}$$

By removing components in (19) not related to the switch we're investigating, we can get a FoM for a switch (20), which will be called normalized loss Λ_P, with unit W/A, which represents its (in)efficiency at passing a certain current. When measuring how optimal a switch is for passing a certain current, we should look at (20) instead of P_M directly. Because P_M would monotonically increase with i_M and does not carry any information about how efficient it is at passing i_M.

$$\Lambda_P = \frac{P_M}{i_M}. \tag{20}$$

By measuring and finding the minimal Λ_P, we can find the current level at which point the discrete switch's W_M equals W_M'. Λ_P is measured across v_{SUP} and current, and it is found that the optimal average switch current is around 250 mA at a v_{SUP} of 5.2V for 4 parallel switches, as shown in Fig. 13. The tests are therefore conducted at this current level.

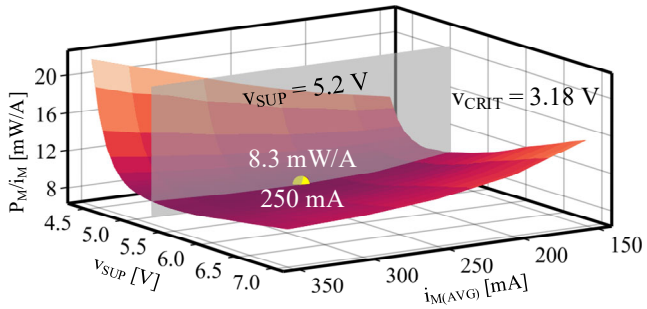

Fig. 13. Measured normalized loss for 4 parallel $M_{1\text{-}4}$ across v_{SUP} and current.

The loss through DUT is measured with R_{SNS1} and R_{SNS2}, as shown in Fig. 10. The voltage drop across R_{SNS1} is measured to get the current that the DUT conducts, which is then combined with the measured R_{ON} from characterization to get P_R. R_{SNS2} and C_{SNS2} filter the gate drive power draw and a DC current can then be measured across R_{SNS2} to get P_G. Furthermore, the quiescent power of the GD ICs are characterized across v_{SUP} and subtracted from the P_G measurements for more accurate gate-charge power results. The power is measured in the same way across 1–8 parallel switches, and v_{SUP} is swept by varying the v_{DD} DC power supply voltage at each parallel switch number, to get Fig. 12.

Due to the limitations of discrete components, it was not possible to find discrete switches with v_T high enough, such

that $2v_T$ is higher than the UVLO of GD ICs, and without significant higher-order effects, such that v_{CRIT} is higher than $2v_T$. However, if an IC were to be fabricated, it would be possible to measure v_{SUP}'' at $2v_T$ like in Fig. 8 and Fig. 9.

C. State of the Art

In state of the art, supply voltages are often selected without discussion, artificially generated high-voltage rails [14], [20], [21], or bootstrap circuits [15], [22], [23]. As we derived earlier, a higher v_{SUP} is detrimental to efficiency unless the width is heavily constrained. Bootstrap circuits usually require large off-chip capacitors that are undesirable for compact single-inductor designs. They are usually motivated by trying to achieve higher $v_{GS/SG}$, but as we derived above, it's not inherently preferable if v_{SUP} also increases. The power losses of bootstrapped gate drivers with integrated capacitors are also rarely investigated rigorously compared to conventional drivers when it is topologically feasible to use either.

The impact of supply voltage on power loss and efficiency is not comprehensively explored, especially in SL–MI/O contexts. This paper aims to provide the theory that can help designers by selecting the correct voltages to supply the gates of power switches to achieve maximum efficiency.

IV. Low-Loss Gate Driver

A. Theory

Normally in simple systems one can tie the v_{SS}/v_{DD} of NMOS/PMOS gate drivers to the source voltage for shutting off the switch, as shown in Fig. 2. However, in SL–MI/O systems, the switching node voltage can go both above and below the I/O voltage that the power switch is connected to. When this happens, body diodes and the channel can conduct I/O current even when the switches are supposed to be off (cross conduction), which is undesirable. Therefore, the gate drivers and the body cannot be hard-wired to either side [24].

Cross conduction is commonly blocked in two ways in low-power domains. One way is to generate extreme voltages. For example, a voltage higher than anything that v_{SW} can switch to can be generated and used to supply the gate of PFETs to keep them off [14], [20]. This is static biasing, as the gate drivers are supplied with static rails. Another common method is to put two MOSFETs in series and connect the body such that the body diodes point to each other [25]–[27]. This is the back-to-back series switches method. The body diode conduction is blocked, and the gates can then be biased with a high voltage, like static biasing, or biased in a way such that the MOS diodes point at each other [24].

Both the above methods can cause significant efficiency degradation. Static biasing requires the gate to now swing to extreme voltages, increasing v_{SUP} and therefore P_G quadratically, moving away from v_{SUP}''. Back-to-back switches put two switches in series which effectively doubles the minimum length of the power switch. The two switches have quadruple the original resistance for the same area, and according to (5), the minimum possible P_M' at least doubles.

In this paper, it is proposed to utilize a dynamic selector that always selects the source terminal of the power switch, which is the terminal with lower potential for NFETs, and the terminal with higher potential for PFETs. This selector often used to bias the body to prevent body diode conduction. But if we connect this selected voltage to the off side of gate drivers, which is the v_{SS} side for NFET and v_{DD} side for PFET, then the gate driver can always shut off the switch successfully.

The selector can be implemented in various ways, but it must operate asynchronously; otherwise, cross conduction would still happen during dead time. One implementation could be a hysteretic common gate comparator connected to two switches [21] that switch v_B between v_S and v_D. This solution is efficient and fast; however, there can still be many design challenges, like quiescent power, ICMR, etc.

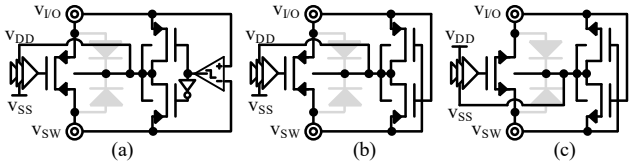

Fig. 14. (a) Generic dynamic selector with comparator. (b) PMOS power switch w/ v_{MAX} selector (c) NMOS power switch w/ v_{MIN} selector.

The simplest implementation with just two switches, depicted in Fig. 14, is recommended. This two-transistor comparator has already seen extensive use in literature [13], [14], [21], [28]–[30]. This paper builds on prior art used for single-I/O implementations to offer gate-driver guidance and solutions that multiple-I/O designs can use to save considerable power. Comparison is achieved by cross-connecting v_G's and v_S's. The two input voltages are usually the v_S and v_D of the power switch in the context of this paper.

When one input voltage is different from another, it causes one selector switch to be more on and the other one off. One selector switch is entirely on if the difference is more than V_{T0}, connecting the output to the correct voltage. This topology can select the lowest/highest voltage with just 2 N/PFETs and operate asynchronously and fast. To illustrate the operation of the selector and the gate drivers, we can look at the operational waveforms in Fig. 15(a).

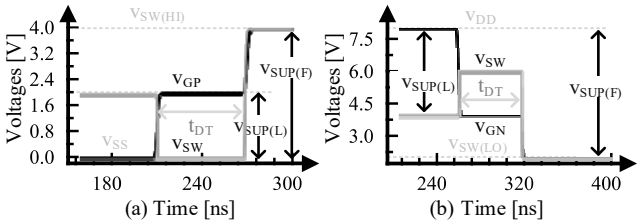

Fig. 15. Simulated v_G and v_{SW} with selector for a (a) PFET and (b) NFET.

This figure shows the gate voltage v_{GP} of a PMOS input switch, and the switching node voltage v_{SW} that it's connected to. Initially the switch is on, with v_{GP} at v_{SS}. Then the switch is opened as v_{GP} rises to the I/O voltage it's connected to. During the dead time $t_{DT,}$ v_{SW} is drained by the dead-time current. Then v_{SW} rises when it's connected to another voltage $v_{SW(HI)}$ that's higher than $v_{I/O}$. The selector selects v_{SW} now as the gate driver supply, and v_{GP} rises to $v_{SW(HI)}$, keeping the switch off.

In other words, v_G only reaches the v_S that it needs to open the switch, sourcing q_{G1} from the lower $v_{SUP(L)}$. Then when v_{SW} is connected to a voltage higher than $v_{I/O}$, v_{MAX} selector supplies the gate now with v_{SW} instead, sourcing q_{G2}, swinging the gate to the full $v_{SUP(F)}$. But during the q_{G2} step, the body, gate, and source are all connected together by the selector. Therefore, only an overlap capacitance in C_{GD} is charged, which is low compared to the rest of the charging losses and can be approximated away. As a result, the gate-charge power when using a selector, $P_{G(SEL)}$, can be much lower than the gate power when the gate is statically biased, $P_{G(Static)}$. $v_{SUP(L)}$ is also more likely to be close to the optimal supply voltage.

$$P_{G(SEL)} = \left[v_{SUP(L)} q_{G1} + \left(v_{SUP(F)} - v_{SUP(L)} \right) q_{G2} \right] f_{SW} \approx k_G v_{SUP(L)}{}^2 f_{SW} < P_{G(Static)} \equiv k_G v_{SUP(F)}{}^2 f_{SW}. \quad (21)$$

B. Tradeoffs

Compared to static biasing or back-to-back switches, the low-loss gate driver method proposed in this paper requires an additional component, the dynamic selector. Therefore, extra design overhead is added. However, if we use the two-transistor design as the selector, the design overhead is low.

The selector itself also introduces its own loss. In the case of the two-transistor design, transistors' widths need to be designed such that the extra resistance it adds to the gate drive path does not increase P_{IV} dramatically. They also cannot be too wide, which increases its own switching loss. However, in sub-5W domain, P_{IV} is usually negligible, therefore the selector can be reasonably small and incur no significant loss.

Since the selector is going to have finite response time, cross conduction can still happen if v_{SW} switches faster than the selector-controlled v_G can respond. But any method of comparison to construct the selector will also be able to respond faster when v_{SW} switches faster, so this is also a manageable loss. For the two-transistor selector specifically, two mechanisms contribute to the response time. First, the selector adds resistance to the gate drive path, which slows down the RC (dis)charging. Second, the selector has a non-operating region when v_S and v_D are similar voltages.

When v_S and v_D are too close to each other, with a difference $|v_{ID}|$ smaller than V_{T0}, neither of the switches is on. The output, therefore, becomes high-impedance until $|v_{ID}|$ rises above V_{T0}, shown below in a DC plot in Fig. 16. The time it takes for $v_{S/D}$ to traverse through the high-impedance zone contributes to the response time. During conduction, the selector output can take some time to reach its final state in the high-impedance region, due to low sub-v_T currents. Therefore, when using this selector, the switch could still have a $v_{SB/BS}$ of around V_{T0} during conduction, resulting in a small body effect.

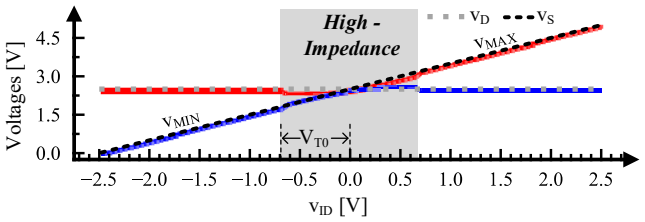

Fig. 16. Simulated two-transistor selector operation in DC.

Cross conduction can happen before the selector responds, but it's not a severe issue as it mainly happens when v_{DS} is low and for a very short interval. Implementing the selector using devices with lower-v_T than the power switch can eliminate this problem, since the switch is off during the high-impedance region. But if low-v_T devices are unavailable, then the widths of the selector should be increased so it recovers from the high-impedance region faster. If the response time is critical, selector topologies like common-gate comparator can be used.

C. Validation

To validate the power savings of the low-loss gate driving scheme, a PCB circuit is designed to measure the gate-charge power of an NMOS power switch connected to an I/O voltage $v_{I/O}$, supplied by a 12 V v_{DD}. The circuit switches a large switch connecting an I/O voltage $v_{I/O}$ to v_{SW}. When the switch is off, a pull down resistor pulls v_{SW} to ground below $v_{I/O}$. This is intended to simulate the switching action inside a SL system without introducing losses in the system beyond the P_G of the DUT. Because the pull down resistor is large, there's negligible conduction loss, and therefore when we measure the loss of the entire system, we get the P_G of DUT (M_9).

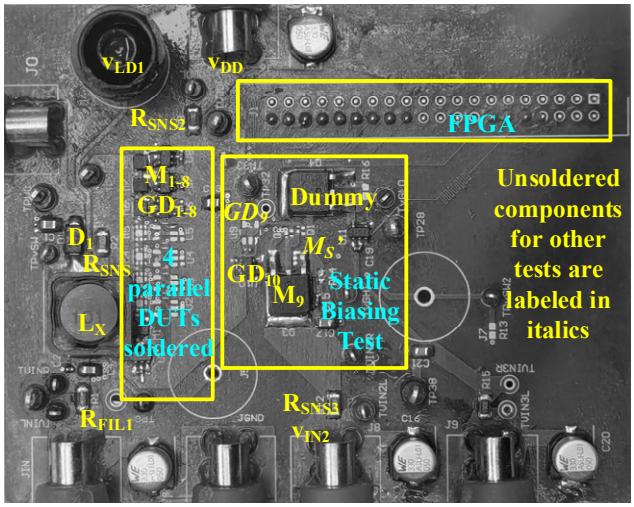

Fig. 17. PCB photograph.

Two gate-driving schemes are measured, the first one is the static biasing scheme shown in Fig. 18. v_{SS} of GD_9 needs to be ground since v_{SW} is pulled to ground, and DUT needs to stay off even when v_{SW} is ground. In this particular simplified circuit, v_{SS} can connect to v_{SW} without cross conduction. However, in an actual multiple-I/O system, v_{SS} cannot be connected to v_{SW} if v_{SW} can connect to another voltage higher than $v_{I/O}$. Consequentially, v_{SS} here is connected to ground

directly to simulate the usual implementation. This static biasing scheme is commonly used to block cross conduction.

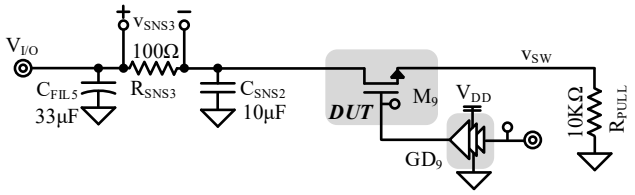

Fig. 18. PCB schematic for testing static biasing P_G.

Another circuit is the low-loss scheme shown in Fig. 19 where the gate driver supplies with 12 V as v_{DD} and selector output as v_{SS}. The selector constructed by M_{S1} and M_{S2} selects the lower voltage dynamically to supply the v_{SS} of GD_{10}.

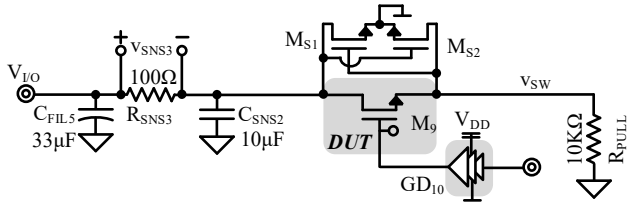

Fig. 19. PCB schematic for testing low-loss driver P_G.

TABLE II
DYNAMIC SELECTOR MEASUREMENTS COMPONENTS

Designator	M_9	GD_9	M_{S1}, M_{S2}
Device	IRFR120ZTRPBF	UCC27517	RUM001L02

In the static biasing case, the v_G of DUT swings from 12 V to ground, and the device turns on and shuts off normally. Since v_{SW} does not drop below ground, there's no risk of accidentally establishing a v_{GS} with a negative v_{SW}. However, P_G is high with this scheme, since v_G swings to ground even when it only needs to swing to $v_{I/O}$ to keep off. In the low-loss scheme, v_G instead only goes to v_{MIN}, which is $v_{I/O}$ when it's on and about to be shut off. And as v_{SW} is pulled below $v_{I/O}$, the selector selects v_{SW} instead to bias the gate. The operational waveforms are shown in Fig. 20.

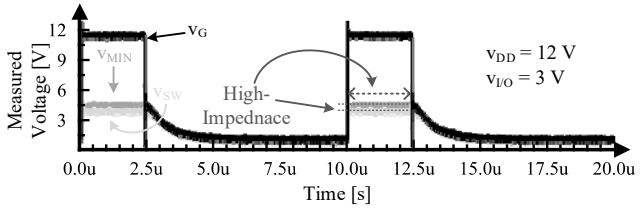

Fig. 20. Measured waveforms of v_{MIN} selector action.

Because the selector itself also has a non-negligible switching loss, it must be measured. However, it's not trivial to measure the power of this selector, since it conducts in quick transients. Therefore, the PCB circuit is designed such that when the loss of the entire system is measured, it primarily consists of the P_G of DUT and the loss of the selector (if present), with every other loss being negligible.

The loss of the entire circuit is measured by R_{SNS3} shown in Fig. 18 and Fig. 19 and R_{SNS2} shown in Fig. 10. Both RC_{SNS}'s filter the power drawn from $v_{I/O}$ and v_{DD} to DC currents that can be easily measured with v_{SNS}'s. The combined power draw from $v_{I/O}$ and v_{DD} is measured for both schemes across different $v_{I/O}$'s. It can be seen that the low-loss scheme can achieve significantly lower loss compared to static biasing.

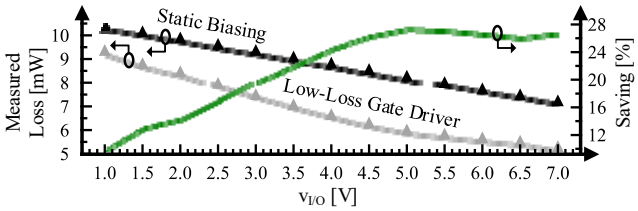

Fig. 21. Measured loss of static biasing versus selector across $v_{I/O}$.

In Fig. 21, the power draws of both static and low-loss gate driving schemes, as well as the P_G saving of low-loss scheme compared to the static scheme is plotted. One can derive from (21) that the P_G saving should increase with $v_{I/O}$, as $v_{SUP(L)}$ decreases with respect to $v_{SUP(F)}$. The effect is not precisely captured in measurements, where the maximum saving is measured to be around 5 V, due to the gate driver ICs' quiescent loss increasing from around half v_{DD}. (21) also approximates away the C_{GD} charging across $v_{SUP(F)}$, which will become dominant as $v_{SUP(L)}$ drops to extremely low levels.

Due to the limitation of discrete components, the power switch DUT does not have independent body access. The low-loss gate driving scheme proposed in this paper also connects the body to the selector, ensuring the gate to body capacitance is not charged when selector output moves. This power saving is therefore not captured in the measurements.

D. State of the Art

Although the dynamic selector has been used extensively in literature for biasing the body to prevent cross conduction through the body diodes [13], [14], [21], [28]–[30], its benefit when used to supply gates has not been explored. In the state of the art, even when they use the selector to bias the body, the gates are often biased by a generated high voltage [14], [21], [29], [30], which increases P_G significantly by moving v_{SUP} away from v_{SUP}'', like the static biasing scheme. This paper proposes to use the selector not only as a body bias circuit, but also simultaneously as the gate bias circuit, and theorized and validated the efficiency benefits.

V. SINGLE-INDUCTOR MULTIPLE-I/O EXAMPLE

To showcase the design guidelines proposed in the paper, a design flow of a simple SL–MI/O buck–boost will be presented in this section. The example system will have an input v_{I1} of 3.3 V, two outputs v_{O1} and v_{O2} of 5 V and 1.8 V with a combined maximum output power of 1 W. The inductor has ESR of 200 mΩ. The system will work in DCM, controlled with open-loop signals with peak modulation. First, we can implement the system in the simplest way, by driving the gates with the extreme voltages in the system, applying F_{NP} to select N/PMOS for M_{I1} and M_{O2}, and sizing them at W_M'.

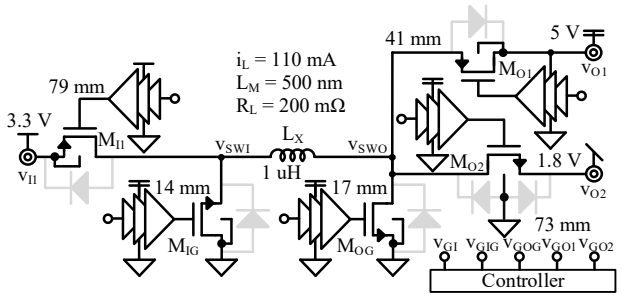

Fig. 22. Simple implementation of SIMO buck–boost.

The simple system in Fig. 22 works well, but according to the optimal supply theory, we should select $v_{DD/SS}$'s of switches such that v_{SUP} is close to $2v_T$, instead of the extreme voltages in the system (v_{O1} and ground). Therefore, we should redesign the system by reselecting the gate drivers' supplies and sizing them again at the new W_M''s, as shown in Fig. 23, with changes highlighted in red. NFETs' gates can be driven with v_{O2} instead of the higher v_{O1}, and the v_{SS} of PMOS' gate drivers can be an I/O voltage instead of ground. F_{NP} should be recalculated with properly selected v_{SUP}'s.

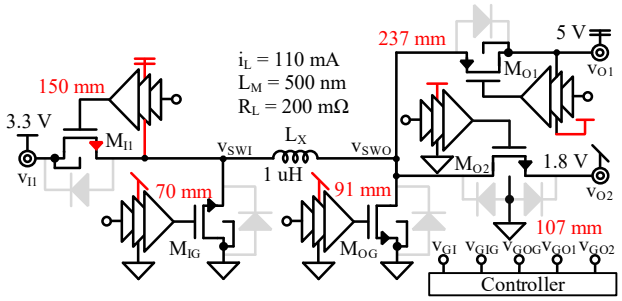

Fig. 23. Applying optimal v_{SUP} to switches.

However, this is still not the optimal design, as M_{O2} is using static biasing to prevent cross conduction, swinging its v_G from 0 to 5 V. If we introduce the selector and low-loss gate driving scheme, M_{O2} can be even more efficient.

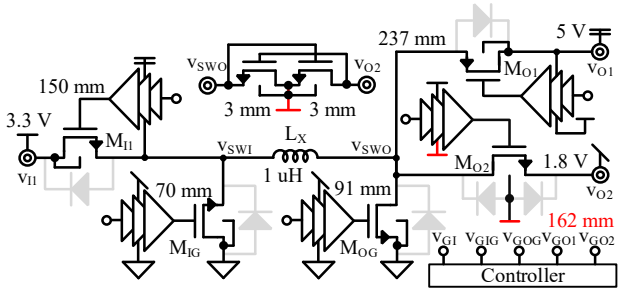

Fig. 24. Using selector to block cross conduction.

The conversion efficiency η_C of all three implementations are measured in simulation across combined output power and plotted below in Fig. 25. It can be seen that the simplest implementation is the least efficient, with the efficiency improving after applying optimal supply theory. And the highest efficiency is achieved after introducing low-loss gate driver and the dynamic selector, which allows even switches that experience cross conduction to reach v_{SUP}''.

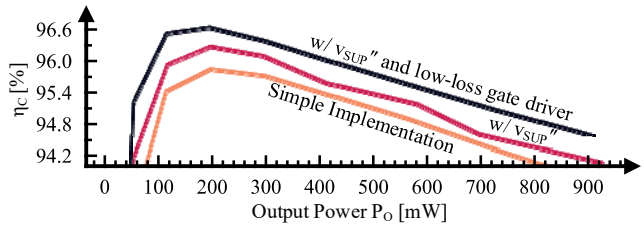

Fig. 25. Simulated conversion efficiency η_C across combined P_O.

Comparing the implementation with all guidelines from the paper applied in Fig. 24 and the simple implementation in Fig. 22, efficiency is improved by around 1%. A 1% improvement in the efficiency of a system that is already 96% efficient represents a 4x reduction in loss, which is a substantial reduction that can be achieved by following the relatively straightforward guidance developed in this paper.

The operational waveforms of the final system shown in Fig. 24 is shown below. v_{MIN} successfully tracks the lower voltage between v_{O2} and v_{SWO}. Cross conduction is prevented, as v_{SWO} is neither clamped to v_{O1} nor v_{O2}, and there's no shorting between ground, v_{O1}, and v_{O2} on the output side.

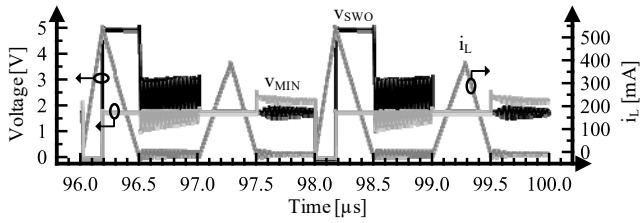

Fig. 26. Simulated operational waveforms showing no cross conduction.

VI. Conclusions

This paper presents design guidelines and insights concerning power switch design in SL–MI/Os. A brief analysis of power MOSFET losses leads to a derivation of the Favorability Index (F_{NP}). This provides designers with an intuitive metric for choosing between an NFET vs. a PFET for any power I/O switch. An optimal supply voltage for efficiency is theorized to be $2v_T$, which is also validated. In a multiple-I/O system, selecting the optimal supply is not always possible. But with this theory, selecting the supply that's the closest to the optimal is fairly straightforward. A low-loss gate driver solution is proposed and validated for efficient blockage of cross conduction while still allowing the supply voltage to be close to the optimal. Finally, an example implementation is provided to illustrate the design flow.

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References

[1] M. Forouzesh, Y.P. Siwakoti et al., "Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[2] A. Al-Fuqaha, M. Guizani et al., “Internet of Things: A Survey on Enabling Technologies, Protocols, and Applications,” IEEE Communications Surveys & Tutorials, vol. 17, no. 4, pp. 2347–2376, 2015.

[3] D. Kwon and G.A. Rincon-Mora, “Single-Inductor–Multiple-Output Switching DC–DC Converters,” IEEE Trans. Circuits Syst. II, vol. 56, no. 8, pp. 614–618, Aug. 2009.

[4] H.-P. Le, C.-S. Chae et al., “A Single-Inductor Switching DC–DC Converter With Five Outputs and Ordered Power-Distributive Control,” IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2706–2714, Dec. 2007.

[5] O. Ray, A.P. Josyula et al., “Integrated Dual-Output Converter,” IEEE Trans. Ind. Electron., vol. 62, no. 1, pp. 371–382, Jan. 2015.

[6] L. Solero, A. Lidozzi et al., “Design of Multiple-Input Power Converter for Hybrid Vehicles,” IEEE Trans. Power Electron., vol. 20, no. 5, pp. 1007–1016, Sep. 2005.

[7] B.G. Dobbs and P.L. Chapman, “A multiple-input DC-DC converter topology,” IEEE Power Electron. Lett., vol. 1, no. 1, pp. 6–9, Mar. 2003.

[8] Y. Li, X. Ruan et al., “Synthesis of Multiple-Input DC/DC Converters,” IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2372–2385, Sep. 2010.

[9] Z. Qian, O. Abdel-Rahman et al., “An Integrated Four-Port DC/DC Converter for Renewable Energy Applications,” IEEE Trans. Power Electron., vol. 25, no. 7, pp. 1877–1887, Jul. 2010.

[10] Z. Qian, O. Abdel-Rahman et al., “Modeling and Control of Three-Port DC/DC Converter Interface for Satellite Applications,” IEEE Trans. Power Electron., vol. 25, no. 3, pp. 637–649, Mar. 2010.

[11] A. Nahavandi, M.T. Hagh et al., “A Nonisolated Multiinput Multioutput DC–DC Boost Converter for Electric Vehicle Applications,” IEEE Trans. Power Electron., vol. 30, no. 4, pp. 1818–1835, Apr. 2015.

[12] G.A. Rincón-Mora, Switched inductor power IC design. Cham: Springer, 2023.

[13] Z. Chen, M.-K. Law et al., “Fully Integrated Inductor-Less Flipping-Capacitor Rectifier for Piezoelectric Energy Harvesting,” IEEE J. Solid-State Circuits, vol. 52, no. 12, pp. 3168–3180, Dec. 2017.

[14] D. Cho, H. Cho et al., “A High-Efficiency Single-Mode Dual-Path Buck-Boost Converter With Reduced Inductor Current,” IEEE Journal of Solid-State Circuits, vol. 58, no. 3, pp. 720–731, Mar. 2023.

[15] C. Hardy and H.-P. Le, “A Reconfigurable Single-Inductor Multi-Stage Hybrid Converter for 1-Cell Battery Chargers,” IEEE Journal of Solid-State Circuits, vol. 58, no. 12, pp. 3503–3518, Dec. 2023.

[16] T.-H. Yang, Y.-H. Wen et al., “A 94.3% Peak Efficiency Adaptive Switchable CCM and DCM Single-Inductor Multiple-Output Converter With 0.03 mV/mA Low Crosstalk and 185 nA Ultralow Quiescent,” IEEE Journal of Solid-State Circuits, vol. 57, no. 9, pp. 2731–2740, Sep. 2022.

[17] A.C.T. Aarts and W.J. Kloosterman, “Compact modeling of high-voltage LDMOS devices including quasi-saturation,” IEEE Trans. Electron Devices, vol. 53, no. 4, pp. 897–902, Apr. 2006.

[18] K. Takeuchi and M. Fukuma, “Effects of the velocity saturated region on MOSFET characteristics,” IEEE Transactions on Electron Devices, vol. 41, no. 9, pp. 1623–1627, Sep. 1994.

[19] G.W. Taylor, “Velocity-saturated characteristics of short-channel MOSFETs,” AT&T Bell Laboratories Technical Journal, vol. 63, no. 7, pp. 1325–1404, Sep. 1984.

[20] T. Xie, J. Zhu et al., “A Highly Integrated Hybrid DC–DC Converter With nH-Scale IPD Inductors,” IEEE Journal of Solid-State Circuits, vol. 58, no. 3, pp. 705–719, Mar. 2023.

[21] H.-J. Chen, Y.-H. Wang et al., “20.9 An energy-recycling three-switch single-inductor dual-input buck/boost DC-DC converter with 93% peak conversion efficiency and 0.5mm2 active area for light energy harvesting,” in 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, Feb. 2015, pp. 1–3.

[22] H.A. Zadeh, H.R. Kooshkaki et al., “An Adaptive Constant-on-Time-Controlled Hybrid Multilevel DC–DC Converter Operating From Li-Ion Battery Voltages With Low Spurious Output,” IEEE Trans. Power Electron., vol. 38, no. 5, pp. 5763–5776, May 2023.

[23] L. Zhao, J. Tang et al., “A 96.1% Efficiency Single-Inductor Multiple-Output (SIMO) Buck Converter With 2.1-A/ns Transient Speed and 2.2-A Maximum Current Capacity,” IEEE Journal of Solid-State Circuits, vol. 59, no. 8, pp. 2545–2556, Aug. 2024.

[24] L. Cui and G.A. Rincon-Mora, “Switched-Inductor Multiple-I/O Power Supplies: MOSFET Selection and Cross Conduction,” in 2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS), Aug. 2024, pp. 1357–1361. Accessed: Dec. 19, 2024. [Online]. Available: https://ieeexplore.ieee.org/document/10658661/?arnumber=10658661

[25] J. Ebrahimi, E. Babaei et al., “A New Multilevel Converter Topology With Reduced Number of Power Electronic Components,” IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 655–667, Feb. 2012.

[26] E. Babaei, “A Cascade Multilevel Converter Topology With Reduced Number of Switches,” IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2657–2664, Nov. 2008.

[27] S.S. Amin and P.P. Mercier, “MISIMO: A Multi-Input Single-Inductor Multi-Output Energy Harvesting Platform in 28-nm FDSOI for Powering Net-Zero-Energy Systems,” IEEE J. Solid-State Circuits, vol. 53, no. 12, pp. 3407–3419, Dec. 2018.

[28] T. Chang and G.A. Rincón-Mora, “Fast Energy-Harvesting TEG-Supplied Charging Regulator Microsystem,” IEEE Trans. Power Electron., vol. 38, no. 7, pp. 9116–9126, Jul. 2023.

[29] Z. Li, Z. Chen et al., “A Self-Bias-Flip With Charge Recycle Interface Circuit With No External Energy Reservoir for Piezoelectric Energy Harvesting Array,” IEEE Transactions on Power Electronics, vol. 38, no. 9, pp. 11630–11641, Sep. 2023.

[30] S. Zhao, C. Zhan et al., “A Battery-Input Three-Mode Buck–Boost Hybrid DC–DC Converter With 97.6% Peak Efficiency,” IEEE Journal of Solid-State Circuits, vol. 59, no. 5, pp. 1567–1577, May 2024.

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