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Compact Switched-Inductor Power Supplies: Design Optimization with Second-Order Core Loss Model

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Abstract: Expressing switched-inductor converter losses simply as a function of design variables is key for designers. Power losses in switched-inductor power supplies are varied in nature, and optimization schemes in the literature fail to account for all of them. Available core loss models are mostly empirical or rely on measurements or variables beyond the reach of power supply designers. Specifically, a simple core loss model is missing. This work offers complete design optimization of switched-inductor power supplies with a quadratic model of core loss that relies solely on design variables known to the designers—inductance and switching frequency (or inductor peak current). This model alleviates the burden of performing complex measurements to characterize the inductor—measurements that, moreover, require geometric data about the core, such as its size, which are often not disclosed by the manufacturer. Predicted minimum losses without approximation are within 3.2% of measured minimum losses, and predicted minimum losses with approximation are within 2.2% of measured minimum losses.

Keywords: core loss; design; second-order model; switched inductor; power supplies; optimization; minimum losses; inductor model; loss approximation

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1. Compact Switched-Inductor Power Supplies

In recent times, there has been a surge in the utilization of electronic devices annually, particularly for portable applications like those used to access the Internet of Things, compact consumer products, wearables, and biomedical devices [1–3]. Because these systems rely on batteries for power, there is a substantial requirement for power converters with heightened efficiency [4–6]. Figure 1 illustrates a typical electronic application with power supply, where a DC–DC voltage regulator, whether derived from an AC–DC converter or a battery, supplies various components like Digital-to-Analog Converters (DACs), Analog-to-Digital Converters (ADCs), Power Amplifiers (PAs), Digital Signal Processing (DSP) microcontrollers, voltage amplifiers, and sensors.

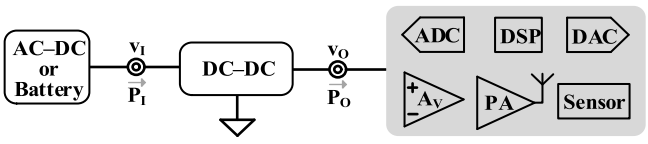

Figure 1. Electronic system with power supply and load.

Switched-inductor converters, renowned for their efficiency across a broad output power range, are popular among power supply solutions. Being a central part of switched inductors, inductors play a crucial role in the overall performance of the switched-inductor power supply. Namely, their volume, inductance, and parasitic elements are paramount [7].

Under heavy loads, the switched-inductor converter operates in continuous conduction, employing Pulse Width Modulation (PWM) [8–12]. The choice of inductance, L_X and

switching frequency, f_{SW}, lies within the designer's discretion. Optimizing f_{SW} and L_X in Continuous Conduction Mode (CCM) has been explored in state-of-the-art reports. However, the papers either lacked one parameter (only f_{SW} is optimized for instance) or omitted certain losses (like IV overlap loss or dead time loss), as detailed further. Notably, the core loss of the inductor is largely absent from the literature when it comes to optimizing a converter for low loss, taking into account core loss. Ref. [13] (also referenced in [12]) offers a simple model, but it excludes the influence of inductance on core loss for a fixed-volume inductor.

The challenges in designing a power supply stem from the absence of a simple core loss model in the optimization scheme. Without this model, designers must rely on trial and error supported by measurements and/or datasheet information at specific design points (inductance and switching frequency), which dampens the design process. The scope of this work includes offering a core loss model that can be directly included in the optimization scheme because it depends only on design variables known to the designers.

Refs. [14–17] discuss predicting core loss through measurements on a core with known geometric characteristics (such as core section), but they do not provide insight into how switching frequency, inductance, and ripple current collectively impact the overall design and efficiency of a complete switched-inductor power converter. For example, selecting L_X and f_{SW} solely to minimize core loss could be detrimental to the overall design, as tradeoffs with other losses must be considered.

Namely, they do not offer a design model that can be used for a general design optimization of a switched-inductor converter. Refs. [13,18,19] investigate inductor optimization to minimize associated losses. However, Refs. [18,19] do not account for all types of losses in their optimization efforts; IV overlap loss and dead time loss are missing. Additionally, Ref. [19] fails to consider core loss despite employing a magnetic core.

Regarding switching frequency optimization, it is explored in [20–26]. However, Refs. [23–25] do not account for IV overlap and dead time losses, and Refs. [20–26] do not report an optimization scheme for L_X.

Traditionally, a Pulse Frequency Modulation (PFM) control scheme is employed in Discontinuous Conduction Mode (DCM), where equally sized energy packets are dispatched to the output as long as it is power-hungry [27–29]. The size of these packets hinges on the inductor and the duration of conduction time t_C or, equivalently, to the inductor peak current $i_{L(PK)}$ [30–33]. Limited research in the literature is available concerning optimization in Discontinuous Conduction Mode (DCM). Ref. [31] investigates loss dominance without optimizing $i_{L(PK)}$ or L_X. Although Refs. [30,32] optimize L_X, they do not include, in their expression for input energy, the amount of energy supplied to the drivers. Ref. [33] also does not consider all losses. Furthermore, no state-of-the-art report includes experimental data presenting an optimization scheme that optimizes all design variables and accounts for all losses.

Incomplete optimization schemes result in sub-optimal designs, leading to more losses in power supplies. For example, in typical usage, where a 1200 mAh smartphone battery would last 21 h [34], a power supply that is 3% less efficient would shorten the battery life by 36 min. This reduction in battery life is significant and highlights the importance of efficient power supply design.

The contribution of this work is to systematically elucidate the impacts of L_X, $i_{L(PK)}$, and f_{SW} on power losses and on the efficiency of a switched inductor power converter. It provides valuable insights into the interdependence of power losses on design variables and guides designers in selecting them judiciously to achieve peak efficiency at the desired output power level. Namely, it offers a linearized quadratic design model for core loss. While certain parameters, such as the width of switches (pertinent to integrated power converters) [35–39] ([35] pp. 225–229), remain at the discretion of the designer, this work emphasizes inductance, switching frequency, and inductor peak current for converters using discrete components. Nevertheless, the theoretical framework derived in this work

remains applicable to integrated circuits and proves valuable in the design of integrated power converters.

Section 2 introduces the inductor design model and Section 3 outlines the optimization process for minimum loss in Discontinuous Conduction Mode and Continuous Conduction Mode, respectively. Section 4 presents the design error, which is used as a benchmark for the optimization process, and shows measurement results. Finally, Section 5 offers concluding remarks for this work.

2. Design Model for Volume-Constrained Inductor

It is always preferable for a system to have the smallest footprint possible. Since inductors typically constitute a substantial portion of the total volume of power supplies [40–43], their volume is crucial. The performance of inductors is directly tied to their volume, as a smaller inductor provides less space for windings and core, influencing their efficiency.

2.1. Ohmic-Loss Model

During the energy transfer process from the input to the output, the inductor incurs DC ohmic loss attributed to its internal coil resistance. Additionally, the inductor determines the ripple current, Δi_L:

$$\Delta i_L = \frac{v_E d_E}{L_X f_{SW}}, \tag{1}$$

which induces AC ohmic loss across all parasitic resistances within the circuit. v_E is the energizing voltage applied across the inductor during a duty cycle fraction, d_E, of the switching period. Equation (2) expresses the inductor DC and AC ohmic loss:

$$P_{R(L)} = R_{L(DC)} i^2_{L(DC)} + R_{L(AC)} \left(\frac{\Delta i_L}{2\sqrt{3}} \right)^2. \tag{2}$$

In most cases, within specified volume constraints, the parasitic resistance, R_L, of the inductor is typically proportional to its inductance, as Figure 2 illustrates and (3) describes based on manufacturers' datasheet:

$$R_L = k_{RL} L_X. \tag{3}$$

k_{RL} is a proportionality factor and is a function of the volume of the inductor. Figure 2 displays R_L as a function of L_X for four different volumes of inductors. Table 1 gives more details about the inductors in Figure 2.

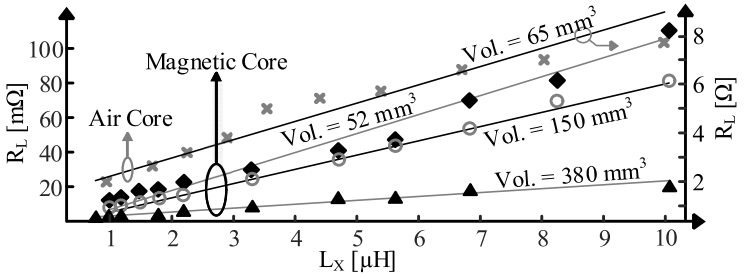

Figure 2. R_L as a function of inductance for four fixed volumes.

Frequency-related phenomena, specifically the skin effect and proximity effect, tend to elevate the effective resistance of a wire when subjected to high-frequency currents [44]. The skin effect arises from a counter electric field that shifts the current distribution toward the edges of the conductor. On the other hand, the proximity effect results from nearby conductors altering the current flow within a wire. The effective resistance is proportionate to the square root of the switching frequency, as [45–48] indicate.

Table 1. Inductors for Figure 2.

#	Serie	k_{RL} [mΩ/µH]	k_C [W/Hz/H/A^2]
○	XGL 5050	3.2	0.032
◆	WE-MAPI 4030	10.3	0.023
✖	1812CS (Air core)	756	N/A
▲	XAL 7070	1.9	0.032

In the context of designing switched inductor power supplies, it becomes crucial to estimate the extent to which these effects contribute to resistance at the switching frequency, as (4) demonstrates:

$$R_L = R_{L(DC)}\left(1 + k_{SW}\sqrt{f_{SW}}\right). \tag{4}$$

k_{SW} is a proportionality factor depending on geometric parameters [49]. The accurate measurement of AC resistance requires specific materials that may not be readily accessible for power supply designers. Instead, inductor manufacturers can provide customers with models, and it may be more convenient to rely on these models during the design process.

2.2. Core Loss Model

Magnetic core inductors provide the benefit of enhancing inductance within a given volume [50–53], making them appealing for space-constrained applications. However, this boost in effective inductance is accompanied by two drawbacks. Firstly, the core is saturable, meaning that when the current flowing through the inductor reaches a certain level, the inductance decreases. Secondly, magnetic cores are susceptible to a particular type of loss known as core loss.

To accurately anticipate the power efficiency of a switched inductor power converter, having an estimate of the core loss is crucial. Core loss, as described by the Steinmetz equation [54–57], Refs. [14–17], is predominantly empirical and relies on measuring or predicting the magnetic field in the core [58–61]. This task is intricate and demands information about the inductor's geometry [62,63]. When designing switched-inductor power supplies, designers typically select a commercially off-the-shelf inductor from a magnetic manufacturer. They need to understand how the chosen inductor will impact the design without depending on information that manufacturers are unwilling to disclose, such as core section area and core material. Additionally, taking measurements for single-winding cores that are not easily accessible is challenging.

Hence, there is a preference for predicting or at least approximating core loss based on known design variables, such as ripple current Δi_L, frequency, and inductance. Inductor manufacturers offer tools to forecast core loss as a function of ripple current Δi_L, frequency, and inductance. Figures 3–5 below illustrate, from manufacturer data, how core loss scales with f_{SW} (with a fixed Δi_L and L_X), with Δi_L (with a fixed f_{SW} and L_X), and with L_X (for a fixed Δi_L and f_{SW}), respectively, for the inductors presented in Table 1.

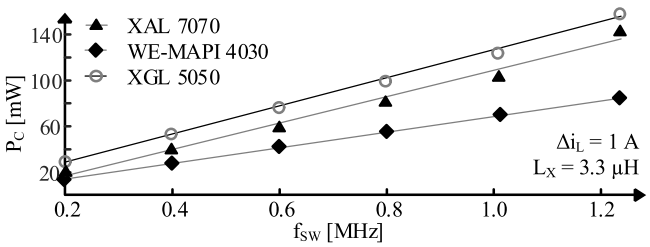

Figure 3. Core loss as a function of switching frequency, f_{SW}.

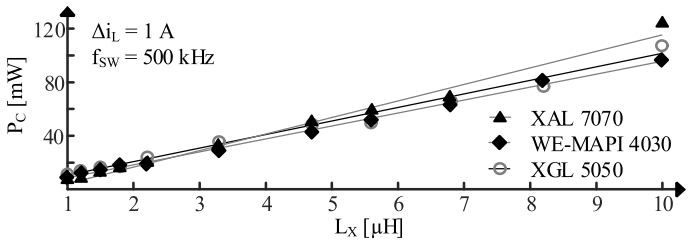

Figure 4. Core loss as a function of inductance, L_X.

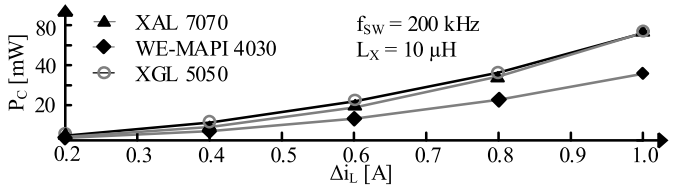

Figure 5. Core loss as a function of ripple current, Δi_L.

Equation (5) presents a design model expression for core loss:

$$P_C = k_C L_X f_{SW} \Delta i_L^2. \tag{5}$$

It has simple linear and quadratic terms (ultimately, all functions of inductance and switching frequency or peak current) and can be included in a broader design optimization scheme including all the loss expressions of a switched inductor. k_C is a constant whose value depends on the volume of the inductor. Δi_L, being proportional to ΔB in the core, (5) is similar to the Steinmetz equation with a frequency exponent of 1 and a flux exponent of 2.

Traditionally, these exponents are between 1 and 2 and 2 and 3, respectively [64]. The exponents in (5) are obtained from curve-fitting, and, as Figures 3–5 highlight, a value of 1 and 2 for the frequency exponent and the ripple current exponent, respectively, provide good results. The intended applicability of this model is for the design of switched-inductor power supplies. It is intended for designers who require a core loss model dependent solely on design variables, facilitating its inclusion in their optimization schemes without the necessity for complex core loss measurements or inductor characterization.

2.3. Design Tradeoffs for Saturable Inductors

A property of magnetic cores is their susceptibility to saturation when the current passing through the inductor becomes too high, leading to an excessive magnetic field. This saturation causes a drop in inductance [65]. From a design standpoint, it is preferable to operate at current levels below the saturation threshold of the inductor because saturation increases losses and creates an unpredictable ripple [66–69].

Magnetic core inductors are ideally characterized by three key attributes: low equivalent series resistance (R_L), low core loss, and a high saturation level. Designers aim to utilize an inductor at the highest possible current scale without reaching saturation. However, all these characteristics are constrained by the volume of the inductor. Given a specific volume, trade-offs must be made regarding which attributes to prioritize.

When selecting an appropriate inductor, designers typically begin by choosing the largest possible inductor within their volume constraints. Subsequently, they opt for the best available core, considering factors such as core material and geometry [70]. This selection involves trade-offs between core loss, R_L, and saturation level. If the initially chosen inductor saturates, designers may need to select another inductor with different characteristics.

3. Switched-Inductor Losses

3.1. Switched Inductor

The central component of a switched-inductor power supply is the inductor. It serves as a temporary energy reservoir for transferring energy from the input to the output, as depicted in Figure 6. Switches apply varying voltage, v_L, across the inductor, alternately energizing it (with an energizing voltage, v_E) and draining it (with a draining voltage, v_D). The draining current comes from the ground. Equations (6) and (7) explicitly define the energizing fraction, d_E, of the switching cycle during which the inductor is energized [35] (p. 111), as follows:

$$v_{SWI(AVG)} = d_E v_E = v_{SWO(AVG)} = d_D v_D, \tag{6}$$

$$d_E = d_D\left(\frac{v_D}{v_E}\right) = \frac{v_D}{v_E + v_D}. \tag{7}$$

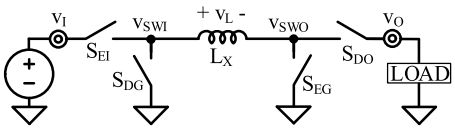

Figure 6. Switched-inductor Buck–Boost.

It is also important to define d_O, the output duty cycle, which corresponds the fraction of the switching period where the inductor is connected to the output. In Figure 6 below, d_O corresponds to d_D. Accordingly, d_I, the input duty cycle, is the fraction of the switching period where the inductor is connected to the input.

3.2. Discontinuous Conduction

In Discontinuous Conduction Mode (DCM), all loss expressions are contingent on the values of inductor peak current, $i_{L(PK)}$, and L_X. Equation (8) provides the expression for $i_{L(PK)}$, where v_E represents the energizing voltage across the inductor during a fraction of the conduction time, t_C, denoted as t_E (equivalent to $d_E t_C$):

$$i_{L(PK)} = \frac{v_E d_E t_C}{L_X}. \tag{8}$$

Figure 7 below illustrates the DCM waveforms, the switching node voltage v_{SW}, output voltage v_O, and inductor current, i_L, with the inductor WE-MAPI 4030 at 100 mA.

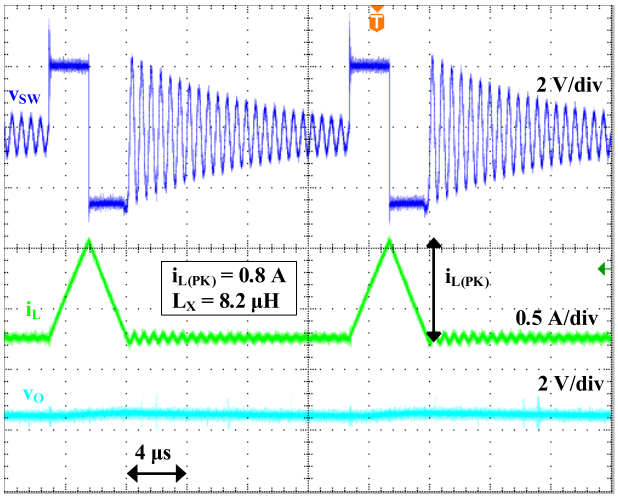

Figure 7. v_{SW}, v_O, and i_L waveforms in DCM for WE-MAPI 4030 at 100 mA.

Given that energy packets are periodically supplied to the load, optimal efficiency is attained when utilizing energy packets with minimal losses. Equation (9) expresses the frequency of pulses function of i_O:

$$i_O = \left(\frac{i_{L(PK)}}{2}\right) t_C f_{SW}. \tag{9}$$

Losses in switched inductor power converters emanate from various origins. Ohmic losses arise from parasitic resistances in components such as the inductor ($E_{R(L)}$), switches ($E_{R(MOS)}$), and output capacitor ($E_{R(C)}$), as (10)–(12) express:

$$E_{R(C)} = R_C t_C \left\{ i_O^2 \left[1 - \left(\frac{d_O t_C}{t_{SW}} \right) \right] + \left[\left(\frac{i_{L(PK)}}{2} - i_O \right)^2 + \left(\frac{0.5 i_{L(PK)}}{\sqrt{3}} \right)^2 \right] \left(\frac{d_O t_C}{t_{SW}} \right) \right\}$$

$$\propto \left(i_{L(PK)}^5 L_X^2 \right) \left\{ f_{SW}^2 - d_O f_{SW} \left(\frac{L_X i_{L(PK)}}{v_E d_E} \right) + \left(\frac{d_O v_E d_E}{f_{SW} L_X i_{L(PK)}} \right) \left[\left(1 - \frac{f_{SW} L_X i_{L(PK)}}{v_E d_E} \right)^2 + K \right] \right\}, \tag{10}$$

$$E_{R(MOS)} = d_{E/D} R_{E/D} \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 t_C \propto i_{L(PK)}^3 L_X, \tag{11}$$

$$E_{R(L)} = R_L \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 t_C \propto i_{L(PK)}^3 L_X^2, \tag{12}$$

where $R_{E/D}$ represents the total resistance of all switches in the energizing or draining path [35] (p. 189).

To prevent a short circuit between the supply and ground, a brief dead time is introduced at the end of the energizing period. Consequently, an inductor current flows through the body diode of the draining switch(es), dropping a voltage, v_{DG}, of approximately 0.7 V, resulting in a loss (E_{DT}) as (13) expresses:

$$E_{DT} = i_{L(PK)} v_{DG} t_{DT} \propto i_{L(PK)}. \tag{13}$$

Turning off the high-side switch creates an overlap loss (E_{IVV}) when both the current flowing through the switch and the voltage across it are high, as (14) expresses:

$$E_{IV} = v_{SW} i_{L(PK)} \left(\frac{t_I}{3} + \frac{t_V}{2} \right) \propto i_{L(PK)}. \tag{14}$$

Charging and discharging the gate capacitances of the switches when they transition from the on state to the off state generate a gate drive loss ($E_{G(MOS)}$), as (15) shows:

$$E_{G(MOS)} = C_{G(MOS)} v_{DD}^2 \propto i_{L(PK)}^0 L_X^0. \tag{15}$$

The stray capacitance (C_{SW}) at the switching nodes burns energy (E_{CSW}) each time the switching node transitions, as (16) shows:

$$E_{CSW} = C_{SW} \left(2 v_{DG}^2 + 0.25 v_{IN}^2 + v_{IN} v_{DG} \right) \propto i_{L(PK)}^0 L_X^0. \tag{16}$$

The controller requires quiescent energy (E_Q) to operate, as (17) expresses:

$$E_Q = P_Q t_{SW} \propto i_{L(PK)}^2 L_X, \tag{17}$$

where t_{SW} is the inverse of f_{SW} given in (9). Drivers consume gate drive energy (E_{GI}) per energy packet, as (18) expresses:

$$E_{GI} \propto i_{L(PK)}^0 L_X^0, \tag{18}$$

with E_{GI} extracted from the datasheet. Usually, switches are much larger than the driver, making E_{GI} negligible in front of $E_{G(MOS)}$. $E_{G(MOS)}$, E_{GI}, and E_{CSW} are constant and do not scale with $i_{L(PK)}$, not L_X (noted with the power exponent 0 in (15), (16), and (18)).

Finally, the magnetic core (when such a core is used) generates a core loss, E_C, as (19) expresses:

$$E_C = k_C L_X i_{L(PK)}^2 \propto i_{L(PK)}^2 L_X. \tag{19}$$

3.3. Continuous Conduction

Increased load compels the converter to transition into CCM. The inductor current ascends during the energizing phase of the switching period and subsequently descends during the draining phase. The distinction from DCM lies in the fact that i_L never attains 0. The average inductor current, $i_{L(avg)}$, is proportionate to the output current, i_O. Figure 8 below shows the CCM waveforms with the inductor XAL 7070 at 1 A.

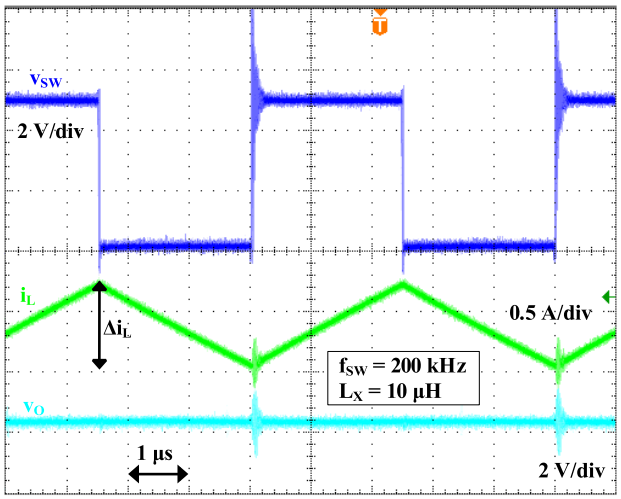

Figure 8. v_{SW}, v_O, and i_L waveforms in CCM for XAL 7070 at 1 A.

In CCM, power losses manifest in five categories. The identical loss mechanisms are applicable, with the distinction that in CCM, ohmic loss takes two forms: DC ohmic loss, which scales quadratically with the output current, and AC ohmic loss ([35], p. 182), which scales with Δi_L^2, as (20) and (21) show:

$$P_{R(AC)} = (d_{E/D} R_{E/D} + R_C + R_L)\left(\frac{0.5\Delta i_L}{\sqrt{3}}\right)^2 \propto \left(\frac{1}{L_X} + \frac{1}{L_X^2}\right), \tag{20}$$

$$P_{RL(DC)} = k_{RL} L_X i_O^2 \propto L_X. \tag{21}$$

Equations (22) and (23) express that P_{IV} and P_{DT} both scale with i_O and f_{SW}:

$$P_{IV} = v_{SW} i_O \left(\frac{t_I}{3} + \frac{t_V}{2}\right) f_{SW} \propto f_{SW}, \tag{22}$$

$$P_{DT} = 2 i_O t_{DT} f_{SW} \propto f_{SW}. \tag{23}$$

Equations (24)–(27) show the expressions of P_{CSW}, P_G, P_{GI} (which depend on f_{SW}), and P_Q:

$$P_{CSW} = C_{SW}\left(2v_{DG}^2 + 0.25 v_{IN}^2 + v_{IN} v_{DG}\right) \propto f_{SW}, \tag{24}$$

$$P_{G(MOS)} = C_{G(MOS)} v_{DD}^2 f_{SW} \propto f_{SW}, \tag{25}$$

$$P_{GI} = E_{GI} f_{SW} \propto f_{SW}, \tag{26}$$

$$P_Q \propto f_{SW}^0. \tag{27}$$

3.4. Switched Inductor Variants

Depending on the relationship between v_{IN} and v_O, switched-inductor power supplies can exhibit various configurations. The Buck and Boost configurations are variants of the Buck–Boost configuration where the output switches and input switches are eliminated, respectively. In the inverting Buck–Boost configuration, the inductor is grounded and v_O is negative, as illustrated in Figure 9. Table 2 below summarizes the expressions for v_E and v_D for the four configurations [35] (p. 111).

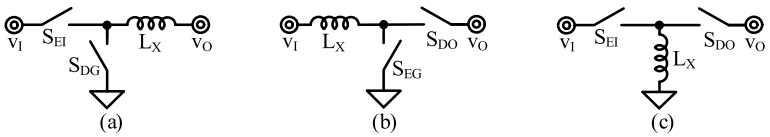

Figure 9. Other topologies: (**a**) Buck, (**b**) Boost, and (**c**) inverting Buck–Boost.

Table 2. v_E, v_D for switched-inductor configurations.

Topology	v_E	v_D
Non-inverting Buck–Boost	v_{IN}	v_O
Buck	$v_{IN} - v_O$	v_O
Boost	v_{IN}	$v_O - v_{IN}$
Inverting Buck–Boost	v_{IN}	$-v_O$

4. Switched-Inductor Design

4.1. Power Level

To optimize the converter in Continuous Conduction Mode (CCM), a DC output current needs to be selected. This current can either be set halfway on the power range or at a point where the converter is most likely to operate, especially if the load is known. Optimizing for a specific i_O ensures the highest efficiency (η_C) for that particular i_O, although it does not guarantee that η_C will peak at this i_O. In Discontinuous Conduction Mode, the optimization approach is independent of i_O. Figure 10 below shows power losses and efficiency as a function of i_O, for a switched inductor optimized for maximum efficiency at 1.5 A.

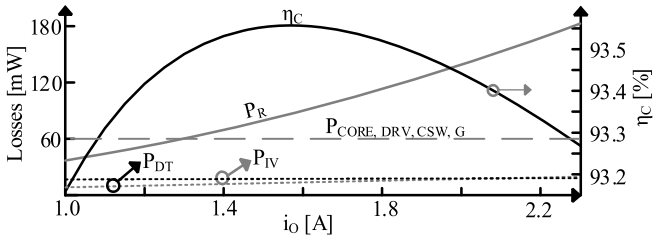

Figure 10. Losses and efficiency as a function of i_O (theoretical).

Since η_C can remain relatively flat in the middle of the i_O scale, it may be beneficial to optimize for a medium i_O and trade off a slightly higher η_C at large i_O, where η_C typically decreases due to ohmic losses dominating all other losses. This trade-off might result in a slightly lower η_C in the high i_O region but a higher η_C on the lower end of the current scale. As depicted in Figure 11, optimizing for 1.4 A yields a slightly lower η_C at high i_O but a higher η_C on the lower end of the current scale compared to optimizing for 1.8 A.

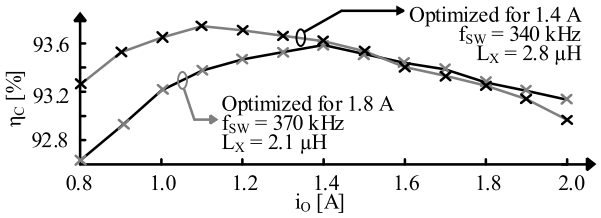

Figure 11. Power efficiency as a function of i_O for two different designs with inductor WE-MAPI 4030.

4.2. Discontinuous Conduction Optimization

Understanding how losses scale with $i_{L(PK)}$ and L_X is key to maximizing efficiency. In DCM, η_C is the ratio of the energy delivered to the output to the energy supplied by the input (E_{IN}), as (28) shows:

$$\eta_C = \frac{E_{IN} - \sum E_{LOSS}}{E_{IN}}. \tag{28}$$

Figure 12 below shows power efficiency in DCM as a function of $i_{L(PK)}$ and L_X.

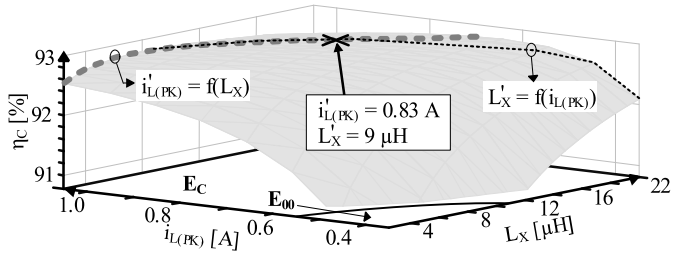

Figure 12. η_C as a function of $i_{L(PK)}$ and L_X in DCM at 100 mA for inductor XGL 5050 (theoretical).

Input energy, E_{IN}, rises with increasing $i_{L(PK)}$ and increasing L_X, but efficiency drops when sizing up the energy packet because it generates more ohmic loss in the switches than it increases E_{IN}. Therefore, optimal $i'_{L(PK)}$ as a function of L_X (grey dashed line in Figure 12) stagnates for large L_X. In other words, efficiency becomes insensitive to L_X when $i_{L(PK)}$ is large enough. When $i_{L(PK)}$ rises, optimal L_X, as a function of $i_{L(PK)}$ (black dotted trace in Figure 12), decreases to compensate for the increasing weight of core loss on efficiency. The bottom horizontal plane in Figure 12 shows which loss dominates. Core loss dominates most of the design space.

On the other hand, when sizing down the energy packet too much, constant losses (losses that are not a function of $i_{L(PK)}$ nor L_X, noted E_{00} in Figure 12) start to overwhelm all other losses because they do not scale down with the size of the energy packet. Therefore, efficiency in DCM peaks when all losses trickily balance.

4.3. Continuous Conduction Optimization

Optimal inductance (noted L'_X) minimizes the sum of $P_{R(AC)}$, P_C, and $P_{RL(DC)}$; that is to say, when the derivative with respect to L_X of the sum of these three losses is 0, as (29) shows:

$$\left.\frac{\partial\left(P_{R(AC)} + P_C + P_{RL(DC)}\right)}{\partial L_X}\right|_{L'_X} = 0 \ . \tag{29}$$

The AC loss, comprising core loss and AC ohmic loss, diminishes as L_X increases. However, due to volume constraints, the resistance of the inductor (R_L) elevates with inductance, leading to $P_{RL(DC)}$ being directly proportional to L_X. Consequently, the optimal L_X is achieved by balancing AC losses (AC ohmic loss $P_{R(AC)}$ and core loss P_C, the sum of those two being noted P_{AC}) with the DC ohmic loss of the inductor $P_{RL(DC)}$ for a specific

output current level, i_O, as Figure 13 shows. It is important to note that optimal inductance is contingent on the switching frequency. As $P_{RL(DC)}$ increases with i_O^2, targeting a higher i_O tends to reduce the optimal L_X.

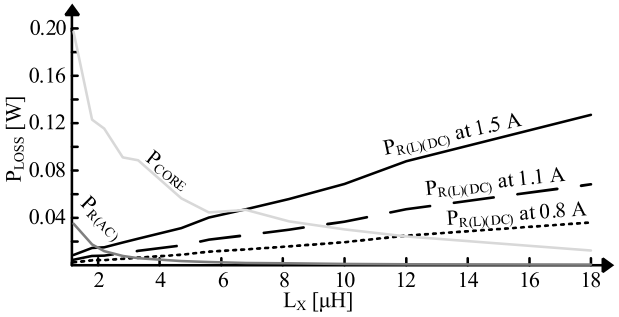

Figure 13. Inductor-related losses as a function of L_X at 250 kHz for inductor XGL 5050 (theoretical).

P_{GI}, P_G, P_{CSW}, P_{IV}, and P_{DT} exhibit proportionality to f_{SW}, whereas AC ohmic loss and core loss are inversely proportional to f_{SW}^2 and f_{SW}, respectively, as Figure 14 shows. P_Q remains constant and does not scale with f_{SW}. Consequently, the aggregate of these losses attains a minimum when switching losses (P_{GI}, P_G, P_{CSW}, P_{IV}, and P_{DT}, noted P_{SW}) balance with P_{AC}. Optimal switching frequency (noted f'_{SW}) is therefore obtained when the derivative with respect to f_{SW} of the sum of P_{GI}, P_G, P_{CSW}, P_{IV}, P_{DT}, and P_{AC} is 0, as (30) shows:

$$\left.\frac{\partial\left(P_G + P_{GI} + P_{C(SW)} + P_{IV} + P_{DT} + P_{AC}\right)}{\partial f_{SW}}\right|_{f'_{SW}} = 0 \ . \tag{30}$$

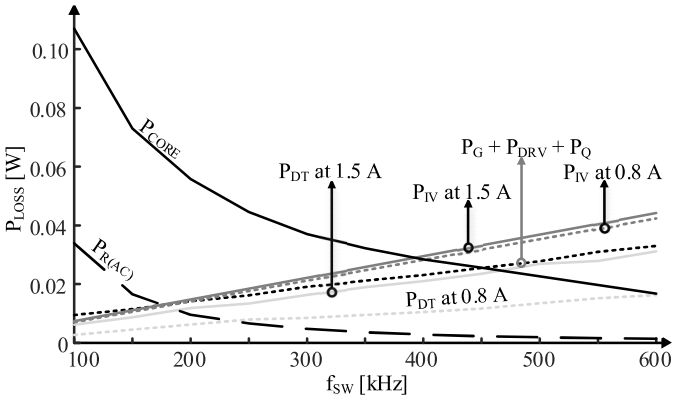

Figure 14. f_{SW}-dependent losses as a function of f_{SW} for a 5.6 µH XGL 5050 inductor (theoretical).

As P_{IV} and P_{DT} scale with i_O, striving for a higher i_O for a given inductance will marginally shift the optimal f_{SW} to a lower value. However, it is crucial to note that the optimal inductance is not constant; it relies on i_O. A higher i_O will counteract the optimal inductance to address the escalation of $P_{RL(DC)}$, significantly amplifying P_{AC}. Consequently, a higher f_{SW} is necessary to counterbalance the increase in P_{AC}.

Figure 15 below shows efficiency as a function of L_X and f_{SW} for 1.5 A. Regarding inductance optimization detailed above, $P_{RL(DC)}$ and P_{AC} shape efficiency along the L_X axis. A small inductance will greatly reduce DC ohmic loss in the coil, but the ripple will grow considerably high, leading to an overwhelming AC loss (namely core loss) and degraded efficiency. This is why optimal inductance, as a function of frequency (black line in Figure 15), shows a narrow range, from 3.5 µH at 600 kHz (bounded by $P_{R(AC)}$) to 9 µH, when f_{SW} is 100 kHz (bounded by $P_{RL(DC)}$).

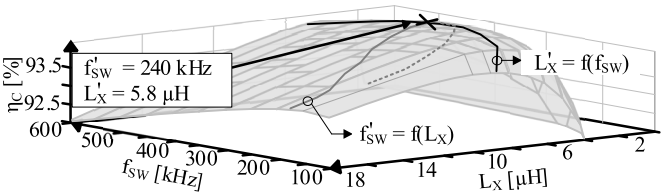

Figure 15. Power efficiency as a function of L_X and f_{SW} in CCM for inductor XGL 5050 (theoretical).

In the higher end of the L_X scale, larger inductances reduce the ripple to a more-than-acceptable level, but efficiency drops again due to DC ohmic loss in the coil. Rising f_{SW} too much will negatively impact η_C as P_{SW} will swamp P_{AC}; this will, however, allow for a very small optimal inductance, as the grey line in Figure 15 shows, to reduce $P_{RL(DC)}$, as the ripple is already low due to the high f_{SW}. On the other hand, pushing f_{SW} to the lower end of its scale will also degrade η_C as P_{AC} takes over; a large inductance is therefore required to attempt to reduce the ripple current.

It is important to note that core loss often overwhelms AC loss, so the optimal f'_{SW}, L'_X, and $i'_{L(PK)}$ are usually not very sensitive to d_E, especially when R_E and R_D are comparable (because $P_{R(AC)}$ depends on d_E, as (20) shows). In DCM, $E_{R(C)}$ is also sensitive to duty cycles, but because ESR_{C_O} is very low, it makes this sensitivity negligible. Moreover, since duty cycles are a function of v_{IN}, v_O, d_E, d_D, d_I, and d_O are usually static parameters, not dynamic variables.

4.4. Design Error

The objective of designers when developing a converter for high efficiency is to approach the minimum loss point as closely as possible. Losses can be quantified as a function of design parameters, and (31) introduces an error measure to quantify how far the predicted minimum deviates from the absolute measured minimum:

$$E_{PLOSS} \equiv \frac{P_{LOSS(MIN)(MEAS.)} - P_{LOSS(MIN)(PREDICTED)}}{P_{LOSS(MIN)(MEAS.)}}. \tag{31}$$

A prediction corresponds to an optimal set of design parameters, which represents a loss point on the measured loss plane.

It is crucial to recognize that inductance values provided by manufacturers are discrete. Therefore, if the predicted optimal inductance falls between two available inductance values, the nearest inductance should be selected. Figure 16 below illustrates which inductance should be chosen as a function of the theoretical optimal inductance, L'_X. This introduces a potential source of error when comparing predicted minimum losses to measured minimum losses.

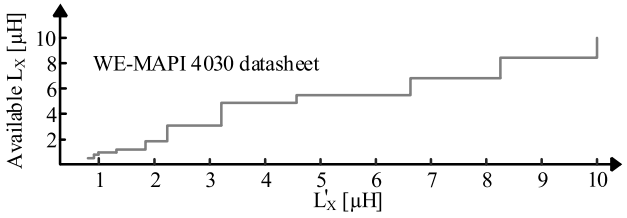

Figure 16. Discrete values of inductance available.

5. Validation

5.1. Buck Prototype

This work presents two optimization schemes: one that includes all the losses outlined in Section 3, and another one that neglects P_Q, P_{CSW}, and P_{GI}. In order to validate the proposed optimization schemes and compare them against the state of the art, a Buck converter is designed, and its total power loss is measured for three different output current

levels and three different inductors, varying inductance and switching frequency (CCM) or inductor peak current (DCM). An optimization scheme predicts an optimal design point (lowest loss), which is a set of optimal design variables, L_X and f_{SW} or $i_{L(PK)}$. The amount of losses induced by these particular sets of design variables is then compared to the lowest amount of loss measured, as (31) details.

It is reasonable to assume that incomplete optimization schemes offered by the state of the art will yield sub-optimal designs. The purpose of this work is not to compare the core loss model against measured core loss (this model being based on manufacturer data) but rather to consider the optimization as a whole. Specifically, it aims to avoid the burden of measuring core loss and/or characterizing inductors, relying instead on data from manufacturers to directly include core loss in the optimization process. This work seeks to quantify how much the optimization schemes from the state of the art are sub-optimal and to offer an optimization scheme that accurately predicts the optimal design point.

Figure 17 shows the schematic of the prototype Buck, and Figure 18 displays the PCB boards used for testing. The three inductors tested are XGL 5050, XAL 7070, and WE-MAPI 4030. An FPGA board was used to feed complementary non-overlapping active-high and active-low signals to the dual driver chip, which drives the NMOS and PMOS transistors, respectively. The method for measuring power losses relies on monitoring input voltage, input current (with sensing resistors R_S and R_{SD}), output voltage, and output current using an oscilloscope (TDS 6054) and multimeters (HP 34401A) to extract input and output powers. The difference between input power and output power represents the power losses.

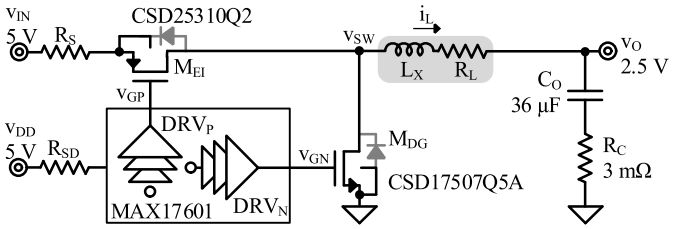

Figure 17. Prototype Buck: schematic.

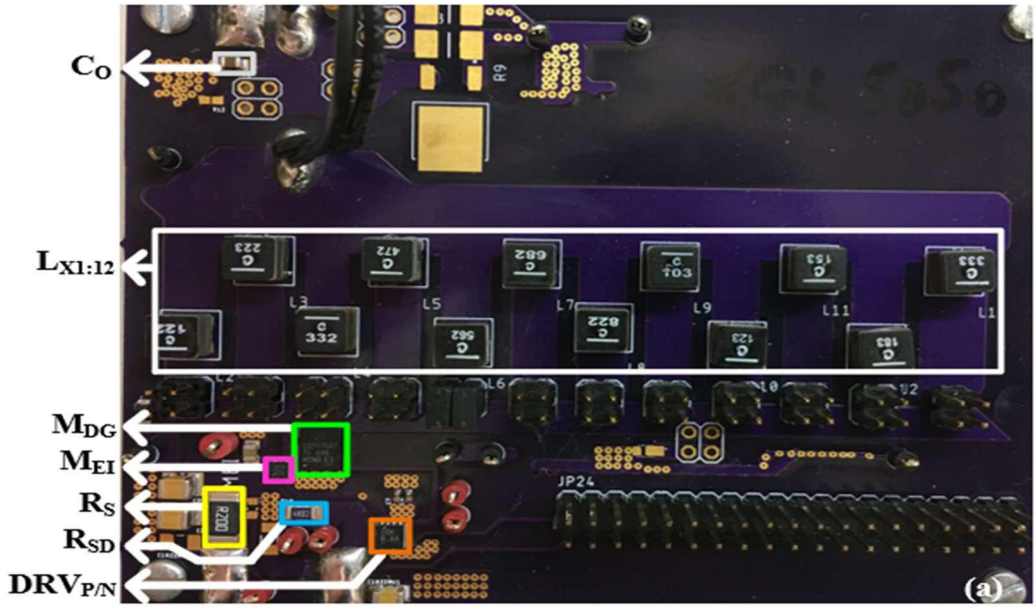

Figure 18. *Cont.*

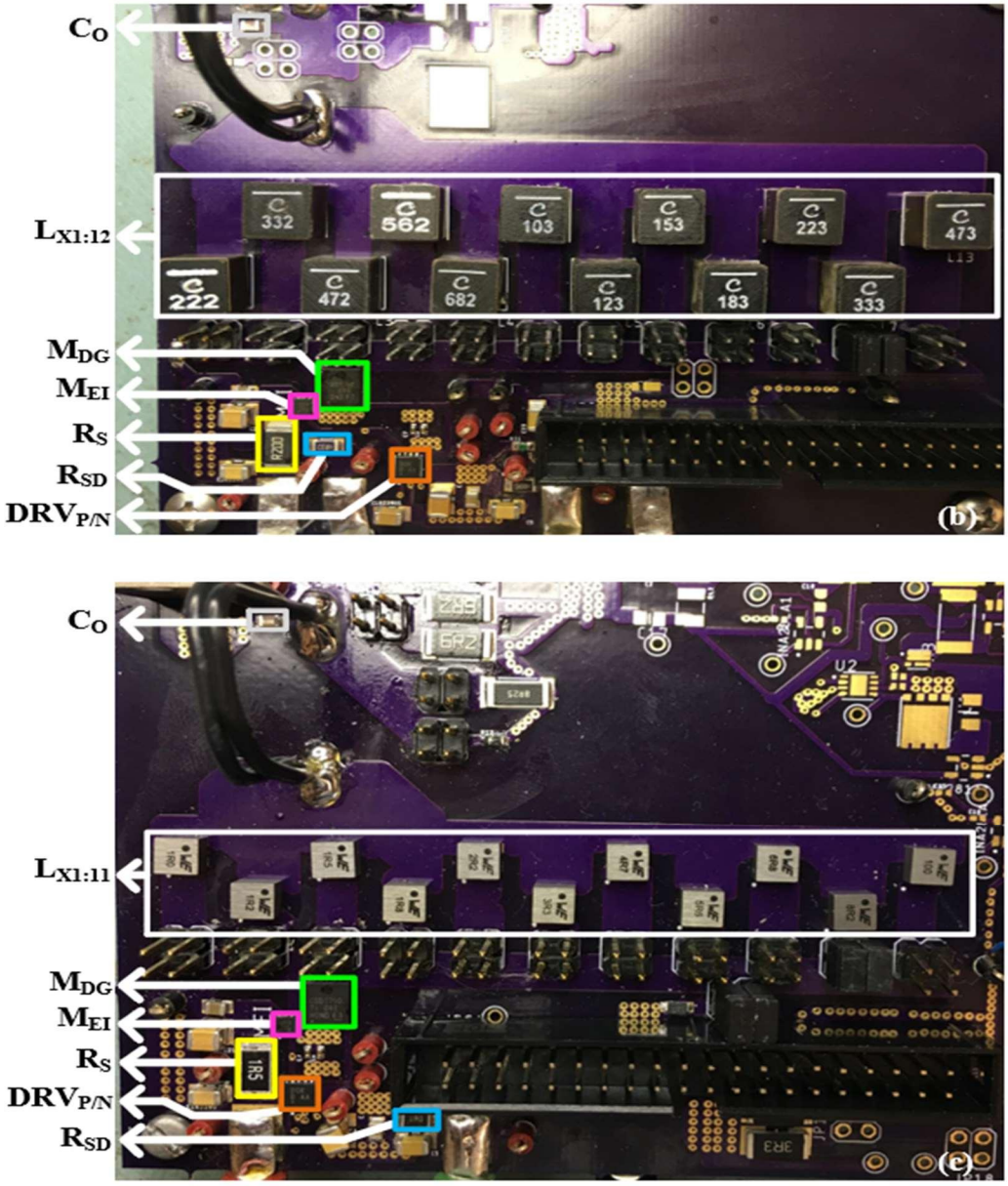

Figure 18. Prototype Buck PCB: XGL 5050 (**a**), XAL 7070 (**b**), and WE-MAPI 4030 (**c**).

5.2. Discontinuous-Conduction Error

In Discontinuous Conduction Mode (DCM), the schemes proposed in this work are compared against two optimization methods from the state of the art; the first neglects IV and dead-time loss, while the second ignores core loss [29,31,32].

The two design parameters in DCM are L_X and $i_{L(PK)}$. Figure 19 below shows measured P_{LOSS} as a function of L_X and $i_{L(PK)}$ at an output current of 100 mA for the inductor WE-MAPI 4030. Figure 7 above shows the DCM waveforms at the minimum loss design point at 100 mA for the inductor WE-MAPI 4030.

Table 3 summarizes the design error for the various optimization schemes. Each scheme provides an optimal (L'_X, $i'_{L(PK)}$) pair, and, from Figure 19, it can be determined how much power loss (P_{LOSS}) this design point yields and how far it deviates from the minimum. Schemes from the state of the art yield errors of 16.4% and 0%, while the schemes presented in this work converge to the optimal design point. It is worth noting that because E_C and output energy scale identically with L_X and $i_{L(PK)}$, omitting E_C in the design in DCM results in the same optimal pair (L'_X, $i'_{L(PK)}$).

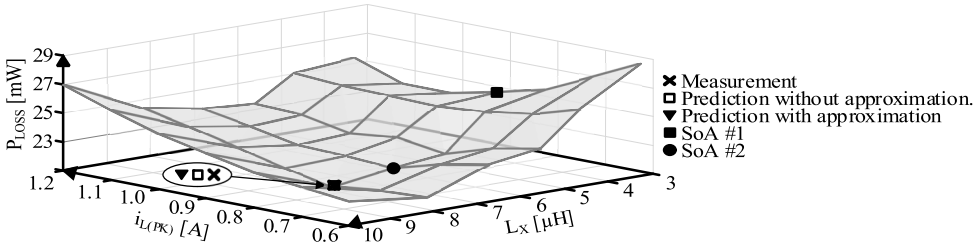

Figure 19. Measured P_{LOSS} in DCM at 100 mA for WE-MAPI 4030.

Table 3. WE-MAPI 4030 in DCM at 100 mA—summary of E_P measurements.

Optimization Scheme	$L_X^{'}$,$i_{L(PK)}^{'}$	P_{LOSS}	E_P
Minimum measured	0.8 A, 8.2 µH	21.3 mW	-
SoA #1 (missing IV, DT loss)	0.94 A, 4 µH	24.8 mW	16.4%
SoA #2 (missing core loss)	0.84 A, 7.6 µH	22.1 mW	0%
Prediction from this work without approximation	0.84 A, 7.6 µH	21.3 mW	0%
Prediction from this work with approximation	0.76 A, 7.7 µH	21.3 mW	0%

The same measurements are performed for the inductors XAL 7070 and XGL 5050. Tables 4 and 5 below summarize the design error for the different optimization schemes. For the XAL 7070 inductor, schemes from the state of the art result in errors of 4.7%, and 3.2%, while the scheme without approximation presented in this work yields an error of 3.2%, and the scheme with approximation yields an error of 2.2%. Interestingly, approximating losses yields a power loss closer to the minimum in this case. This is because the prediction with and without approximation results in an L_X' value roughly halfway between two available inductors (33 µH and 47 µH), creating an error, as Figure 16 highlights. For the XGL 5050 inductor, schemes from the state of the art yield errors of 3.1% and 0%, while schemes presented in this work converge to the optimal design point.

Table 4. XAL 7070 in DCM at 180 mA—summary of E_P measurements.

Optimization Scheme	$L_X^{'}$,$i_{L(PK)}^{'}$	P_{LOSS}	E_P
Minimum measured	400 mA, 47 µH	31.7 mW	-
SoA #1 (missing IV, DT loss)	530 mA, 23 µH	33.2 mW	4.7%
SoA #2 (missing core loss)	480 mA, 37 µH	32.7 mW	3.2%
Prediction from this work without approximation	480 mA, 37 µH	32.7 mW	3.2%
Prediction from this work with approximation	440 mA, 39 µH	32.4 mW	2.2%

Table 5. XGL 5050 in DCM at 100 mA—summary of E_P measurements.

Optimization Scheme	$L_X^{'}$,$i_{L(PK)}^{'}$	P_{LOSS}	E_P
Minimum measured	500 mA, 22 µH	22.8 mW	-
SoA #1 (missing IV, DT loss)	610 mA, 14.7 µH	23.5 mW	3.1%
SoA #2 (missing core loss)	540 mA, 23.5 µH	22.8 mW	0%
Prediction from this work without approximation	540 mA, 23.5 µH	22.8 mW	0%
Prediction from this work with approximation	500 mA, 24.3 µH	22.8 mW	0%

5.3. Continuous-Conduction Error

In CCM, the design variables are L_X and f_{SW}. In CCM, the state of the art has three optimization schemes; a few papers from the literature do not offer an optimization scheme for L_X [20,21], while some others ignore IV and dead-time loss [18,23–25]. The last one ignores core loss [18,23–25].

Figure 20 below shows P_{LOSS} for the XAL 7070 inductor at 1 A. Table 6 below summarizes the design error for the different optimization schemes. The error reported from the

first state of the art is the minimum loss of the worst-case inductor. Schemes from the state of the art yield errors of 12.6%, 8.7%, and 41.7%, while the scheme without approximation presented in this work yields an error of 0.9%, and the scheme with approximation yields an error of 0.9%. Figure 8 above shows the switching node voltage, v_{SW}; output voltage, v_O; and inductor current, i_L, at the minimum loss design point in CCM for the inductor XAL 7070 at 1 A.

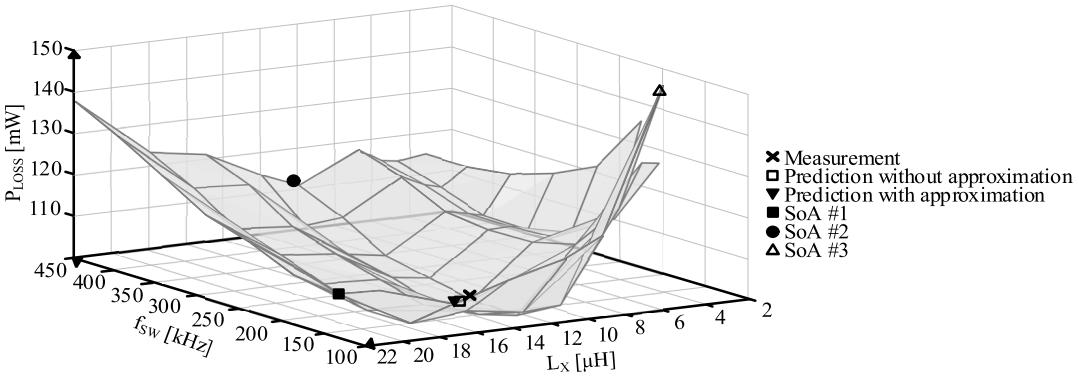

Figure 20. Measured P_{LOSS} in CCM at 1 A for XAL 7070.

Table 6. XAL 7070 in DCM at 1 A—summary of E_P measurements.

Optimization Scheme	$f_{SW}^{'}$,$L_X^{'}$	P_{LOSS}	E_P
Minimum measured	200 kHz, 10 µH	103 mW	-
SoA #1 (only f_{SW} is optimized)	150 kHz, 22 µH	116 mW	12.6%
SoA #2 (missing IV, DT loss)	420 kHz, 8.9 µH	112 mW	8.7%
SoA #3 (missing core loss)	120 kHz, 7.6 µH	146 mW	41.7%
Prediction from this work without approximation	190 kHz, 11.2 µH	104 mW	0.9%
Prediction from this work with approximation	180 kHz, 11.6 µH	104 mW	0.9%

The same measurements are performed for the inductors WE-MAPI 4030 and XGL 5050. Tables 7 and 8 below summarize the design error for the different optimization schemes. For the WE-MAPI inductor, schemes from the state of the art yield errors of 41.8%, 60.8%, and 28.2%, while the scheme without approximation presented in this work converges to the optimal design point, and the scheme with approximation yields an error of 1%. For the XGL 5050 inductor, schemes from the state of the art yield errors of 84.9%, 20.5%, and 16.2%, while schemes presented in this work converge to the optimal design point.

Table 7. WE-MAPI 4030 in CCM at 1 A—summary of EP measurements.

Optimization Scheme	$f_{SW}^{'}$,$L_X^{'}$	P_{LOSS}	E_P
Minimum measured	350 kHz, 3.3 µH	184 mW	-
SoA #1 (only f_{SW} is optimized)	550 kHz, 1.2 µH	261 mW	41.8%
SoA #2 (missing IV, DT loss)	630 kHz, 2.4 µH	296 mW	60.8%
SoA #3 (missing core loss)	370 kHz, 2.5 µH	236 mW	28.2%
Prediction from this work without approximation	330 kHz, 3.9 µH	184 mW	0%
Prediction from this work with approximation	320 kHz, 3.8 µH	186 mW	1%

Table 8. XGL 5050 in CCM at 1 A—summary of E_P measurements.

Optimization Scheme	$f_{SW}^{'}$,$L_X^{'}$	P_{LOSS}	E_P
Minimum measured	250 kHz, 8.2 µH	185 mW	-
SoA #1 (only f_{SW} is optimized)	500 kHz, 1.2 µH	342 mW	84.9%
SoA #2 (missing IV, DT loss)	550 kHz, 5.1 µH	223 mW	20.5%

Table 8. *Cont.*

Optimization Scheme	$f_{SW}^{'}$,$L_X^{'}$	P_{LOSS}	E_P
SoA #3 (missing core loss)	180 kHz, 5 µH	215 mW	16.2%
Prediction from this work without approximation	250 kHz, 8 µH	185 mW	0%
Prediction from this work with approximation	240 kHz, 7.6 µH	185 mW	0%

As the CCM current scale is usually longer than in DCM, another set of measurements is performed for the three inductors at 1.5 A. Figure 21 below shows P_{LOSS} for the XGL 5050 inductor at 1.5 A. Table 9 summarizes the design error for the different optimization schemes. Schemes from the state of the art yield errors of 76%, 46.4%, and 20.6%, while schemes presented in this work converge to the optimal design point. Figure 22 shows v_{SW}, v_O, and i_L at the minimum loss design point for the inductor XGL 5050 at 1.5 A.

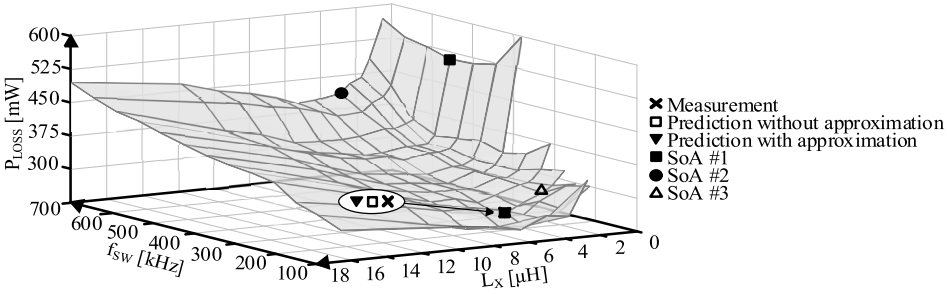

Figure 21. Measured P_{LOSS} in CCM at 1.5 A for XGL 5050.

Table 9. XGL 5050 in CCM at 1.5 A—summary of E_P measurements.

Optimization Scheme	$f_{SW}^{'}$,$L_X^{'}$	P_{LOSS}	E_P
Minimum measured	250 kHz, 5.8 µH	291 mW	-
SoA #1 (only f_{SW} is optimized)	550 kHz, 1.2 µH	512 mW	76%
SoA #2 (missing IV, DT loss)	680 kHz, 3.4 µH	426 mW	46.4%
SoA #3 (missing core loss)	200 kHz, 3.8 µH	351 mW	20.6%
Prediction from this work without approximation	260 kHz, 5.9 µH	291 mW	0%
Prediction from this work with approximation	250 kHz, 5.5 µH	291 mW	0%

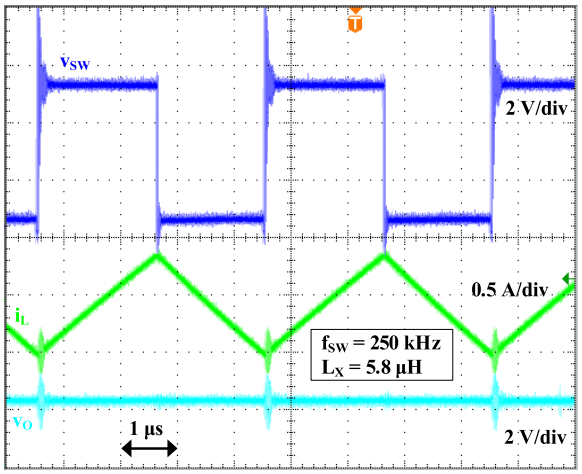

Figure 22. v_{SW}, v_O, and i_L waveforms in CCM for XGL 5050 at 1.5 A.

The same measurements are performed for the inductors WE-MAPI 4030 and XAL 7070. Tables 10 and 11 below summarize the design error for the different optimization schemes. For the WE-MAPI 4030 inductor, schemes from the state of the art yield errors of

40.5%, 50.2%, and 8.7%, while the scheme without approximation presented in this work yields an error of 0.6%, and the scheme with approximation yields an error of 0.6%. For the XAL 7070 inductor, schemes from the state of the art yield errors of 20.8%, 11.3%, and 11.3%, while schemes presented in this work converge to the optimal design point.

Table 10. WE-MAPI 4030 in CCM at 1.5 A—summary of E_P measurements.

Optimization Scheme	f'_{SW},L'_X	P_{LOSS}	E_P
Minimum measured	450 kHz, 2.2 µH	289 mW	-
SoA #1 (only f_{SW} is optimized)	200 kHz, 10 µH	406 mW	40.5%
SoA #2 (missing IV, DT loss)	720 kHz, 1.4 µH	434 mW	50.2%
SoA #3 (missing core loss)	405 kHz, 1.7 µH	324 mW	8.7%
Prediction from this work without approximation	410 kHz, 2.5 µH	300 mW	0.6%
Prediction from this work with approximation	370 kHz, 2.5 µH	300 mW	0.6%

Table 11. XAL 7070 in CCM at 1.5 A—summary of E_P measurements.

Optimization Scheme	f'_{SW},L'_X	P_{LOSS}	E_P
Minimum measured	250 kHz, 10 µH	168 mW	-
SoA #1 (only f_{SW} is optimized)	500 kHz, 2.2 µH	203 mW	20.8%
SoA #2 (missing IV, DT loss)	510 kHz, 4.9 µH	187 mW	11.3%
SoA #3 (missing core loss)	130 kHz, 5.6 µH	187 mW	11.3%
Prediction from this work without approximation	230 kHz, 8.5µH	168 mW	0%
Prediction from this work with approximation	210 kHz, 8.6 µH	168 mW	0%

It is important to note that the error in CCM is significantly more significant than in DCM. The reason is twofold. First, core loss in CCM no longer scales with output energy the same way it does in DCM, so ignoring core loss in CCM results in a significant error, which is invisible in DCM. Second, the fractional weight of IV and dead time loss is more important in CCM than in DCM, so neglecting them in DCM leads to fewer errors. Lastly, the optimization scheme neglecting P_Q, P_{CSW}, and P_{GI} results in a maximum error of 2.2%, highlighting the fact that those losses can be neglected.

5.4. Optimization Check

When selecting an i_O large enough to operate in CCM but close to the boundary with DCM, the optimization scheme in CCM should result in the same L'_X value and ripple current (indirectly obtained from f_{SW}) as the optimal L'_X and $i'_{L(PK)}$ obtained from optimizing in DCM. Figure 23 illustrates this principle with the inductor WE-MAPI 4030. The converter is optimized in CCM for 450 mA, and the two efficiency curves intersect at the boundary, indicating that the two optimization schemes in DCM and CCM proposed are correct.

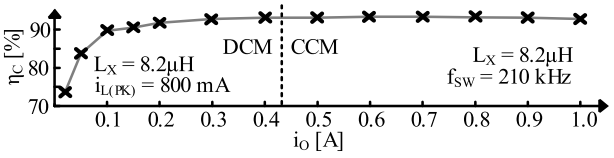

Figure 23. η_C as a function of i_O showing convergence of optimization scheme in DCM and CCM.

6. Conclusions

This work presents a core loss model that is a function of design variables only known to power supply designers. This way, it alleviates the burden of the designers to estimate core loss from measurements and geometric information that are usually unknown for commercially off-the-shelf inductors. With this model, core loss can be directly included in the optimization scheme. Furthermore, this work addresses all types of losses to be

accounted for in the optimization effort. This aspect has been largely absent from previous research efforts. Predicted minimum losses without approximation are within 3.2% of measured minimum losses, while predicted minimum losses with approximation are within 2.2% of measured minimum losses.

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