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Quantifying and Correcting Systemic Offset Errors in PWM and Peak–Valley DC–DC Converters

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Abstract

DC–DC converters are ubiquitous in consumer, industrial, commercial, and medical applications. In such voltage-, power-, and area-constrained systems, guaranteeing accurate output voltage remains a key challenge. Investigation of the fundamental cause of steady-state output errors in DC–DC converters, however, is largely absent in the literature. This work identifies systemic voltage offset error as one of the key contributors to steady-state output inaccuracy in PWM and peak–valley-controlled switched-inductor voltage regulators. It uses an insightful reverse-feedback translation framework to quantify the systemic offset as a function of the duty cycle, input voltage, sawtooth amplitude, propagation delays, load conditions, error amplifiers, and comparator. Furthermore, with the derived offset expressions, the paper develops accurate and low-overhead design guidelines to remove systemic errors by aligning the regulator's steady-state equilibrium with its operating conditions. With the proposed offset "centering" and "elimination" techniques, the systemic error (that accounts for up to 2.1% variation in the steady-state output) is reduced by over 70% when centered and to zero when eliminated at room temperature. Overall, this work provides an insightful and generalized quantification of systemic offsets and describes low-overhead strategies to restore steady-state accuracy in practical PWM, hysteretic and peak/valley-controlled voltage regulators.

Keywords: switched-inductor power supply; voltage regulator; DC–DC converter; negative feedback; gain error; offset; voltage loop; current-mode voltage loop; loading effect; PWM; hysteretic; peak; valley; offset correction; offset elimination

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1. Accurate DC–DC Converters

Accurate DC–DC voltage regulators are ubiquitous in applications like microprocessors, IoT devices, implantable biomedical devices and renewable energy harvesters [1–8]. A typical DC–DC power-supply system is illustrated in Figure 1. It consists of switch-mode and linear power supplies. Among switch-mode supplies, switched-inductor voltage regulators are widely preferred for their high conversion efficiencies [9–12]. Since their output voltage has ripples, switched-inductor voltage regulators are typically used to power digital loads. Noise-sensitive analog loads are powered by the less efficient but far steadier linear low-dropout (LDO) regulators [13–15].

The steady-state accuracy of a switched-inductor voltage regulator, defined as the difference between the output voltage, v_O, and the target output voltage, v_O', under steady-state conditions has been the focus of many works [16–24]. One of the key contributors to the regulator's steady-state error is the systemic error, v_{Err}, which is inherent to the

negative feedback mechanism that regulates v_O. Finite loop gain of practical negative feedback loops result in a systemic offset, v_{OS}, at the input of the loop. It is this v_{OS} that translates into v_{Err} at the output.

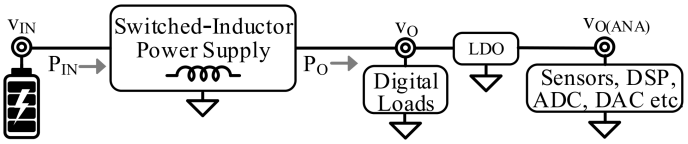

Figure 1. Typical power-supply system composition.

Various prior works have proposed modifications to the feedback loop gain to restore the accuracy of the regulator's output. Ref. [16] proposes the design of a high-gain error amplifier that suppresses the forward translation of v_{OS} to v_{Err}. However, this merely reduces v_{Err}, leaving behind a residual systemic error at the expense of the limited bandwidth of the regulator. Refs. [17,19] eliminate v_{Err} by altering the DC loop gain using digital algorithm implementations. However, their approach is iterative and requires additional FPGA or MCU blocks. Other works [20–24] have proposed the design of secondary feedback loops to suppress v_{OS} upon sensing v_{Err}. For example, refs. [20–22] dynamically trim the feedback factor (β_{FB}) and [23] dynamically adjusts the reference voltage (v_{REF}) to eliminate the offset when an output error is sensed. However, the limited response times from finite loop bandwidths, and the limited robustness of these solutions renders the system vulnerable to recurrence of v_{Err} at extreme operating conditions. Moreover, the additional area and power overhead from secondary loops add unwanted costs. Many of the presented solutions are also narrow in their scope, optimizing their analysis to specific control techniques [17–24]. Overall, a unified, insightful, control-agnostic formalism of systemic offsets is missing from the literature, rendering v_{OS} and v_{Err} unpredictable across regulator design parameters and operating conditions.

The present work fills this gap by deriving v_{OS} as a function of design parameters (propagation delay, component offsets, and sawtooth parameters) and regulator operating conditions (input voltage, load, and duty cycle) through an insightful, control-agnostic reverse-feedback translation framework. The paper demonstrates and validates this approach for the three most popularly used control techniques [25–27], namely, pulse-width modulation (PWM), hysteretic and peak/valley control. Furthermore, using the derived offset expressions, it develops a novel approach to accuracy. Unlike prior research, this work proposes design modifications of existing parameters that eliminate v_{OS} by aligning the regulator's steady-state equilibrium with its operating conditions. Thus, the presented solution allows designers to remove the systemic error at its source in an insightful, accurate and single-step way. Furthermore, it has a minimal impact on loop stability and circuit complexity.

The paper is organized as follows: Section 2 defines the fundamental systemic offset in switched-inductor voltage regulators and derives its relationship to v_{Err}. Section 3 provides a rigorous quantification of this offset within PWM control. It also presents the proposed strategies for systemic offset elimination to realize a highly accurate system. Section 4 extends this analysis to hysteretic and peak/valley control. Section 5 expands on other sources of steady-state error and discusses the practical considerations of the proposed strategies. Finally, key conclusions are drawn in Section 6.

2. Offset Errors in Switched-Inductor Voltage Regulators

2.1. Ideal Switched Inductors

Switched inductors lie at the heart of inductive voltage regulators, efficiently transferring energy from an input voltage source to the output. The switched inductor is shown

in Figure 2. It consists of an ideal inductor, L_X, between switching nodes v_{SWI} and v_{SWO} and ideal switches S_{EI}, S_{DI}, S_{EO} and S_{DO}. At first, switches S_{EI} and S_{EO} close, energizing L_X with an energizing voltage, v_E, for an energizing time, t_E. During t_E, inductor current i_L rises linearly at a slope proportional to v_E. Subsequently, S_{EI} and S_{EO} open and S_{DI} and S_{DO} close for a draining time, t_D. During t_D, L_X releases its energy into the output and i_L falls linearly at a slope proportional to v_D. The alternate conduction of switch pairs S_{EI}, S_{EO} and S_{DI}, S_{DO} repeats over multiple switching period t_{SW} and induces a voltage, v_O, at the output.

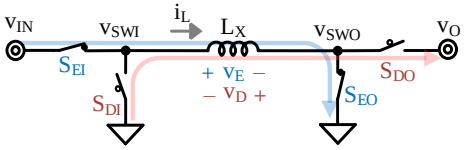

Figure 2. Ideal switched inductor with energizing and drain phases shown with blue and red markings respectively.

Since L_X is a DC short, the average inductor current, $i_{L(AVG)}$, remains constant in the steady state. Therefore, i_L rises with v_E during t_E as much as it falls with v_D during t_D, resulting in a volts–seconds balance [27]:

$$v_E t_E = v_D t_D = v_D(t_{SW} - t_E) = v_D t_E \left(\frac{1}{d_E} - 1\right). \quad (1)$$

In the above equation, the ratio of t_E to t_{SW} is defined as the energizing duty cycle, d_E. From (1), d_E can be expressed as:

$$d_E = \frac{v_D}{v_E + v_D}. \quad (2)$$

where v_E and v_D are linear functions of v_{IN} and v_O. In fact, in the switched inductor described above, v_E and v_D are equal to v_{IN} and v_O respectively. Therefore, v_O is related to v_{IN} via d_E. The target output voltage of the regulator, v_O', is set by its application. It is this v_O' that determines the input, d_E, of the switched-inductor stage.

2.2. Topologies

The switched inductor in Figure 2 can both buck and boost v_{IN} to v_O' depending on the input, d_E. It is therefore referred to as the buck–boost topology. In applications where v_O' is strictly lower than v_{IN}, L_X can be energized directly into v_O, circumventing the output switches. This gives rise to the buck topology, shown in Figure 3b. Conversely, when v_O' is strictly higher than v_{IN}, input switches can be circumvented to realize the boost topology (Figure 3c). Negative output voltages can be produced by draining the energized inductor into the ground, as in the inverting boost–boost topology (Figure 3d). Finally, in the flyback (Figure 3e), v_{IN} energizes an input inductor, L_{XI}, which is coupled to an output inductor, L_{XO}, in the opposite direction with a transformer ratio of 1:k_T. Energy is transferred to the output when the output voltage drains L_{XO}. This topology is useful when galvanic isolation is necessary between the input and output supplies [27]. In Table 1, v_E and v_D are expressed in terms of v_{IN} and v_O for each topology. The resulting d_E is derived from (2).

Table 1. Energizing/draining voltages in ideal switched-inductor topologies.

Topology	v_E	v_D	d_E
Buck–Boost	v_{IN}	v_O	$\frac{v_O}{v_{IN}+v_O}$
Buck	$v_{IN} - v_O$	v_O	$\frac{v_O}{v_{IN}}$

Table 1. *Cont.*

Topology	v_E	v_D	d_E
Boost	v_{IN}	$v_O - v_{IN}$	$\frac{v_O - v_{IN}}{v_O}$
Inverting	v_{IN}	$-v_O$	$\frac{-v_O}{v_{IN} - v_O}$
Flyback	v_{IN}	$\frac{v_O}{k_T}$	$\frac{v_O}{v_{IN} k_T + v_O}$

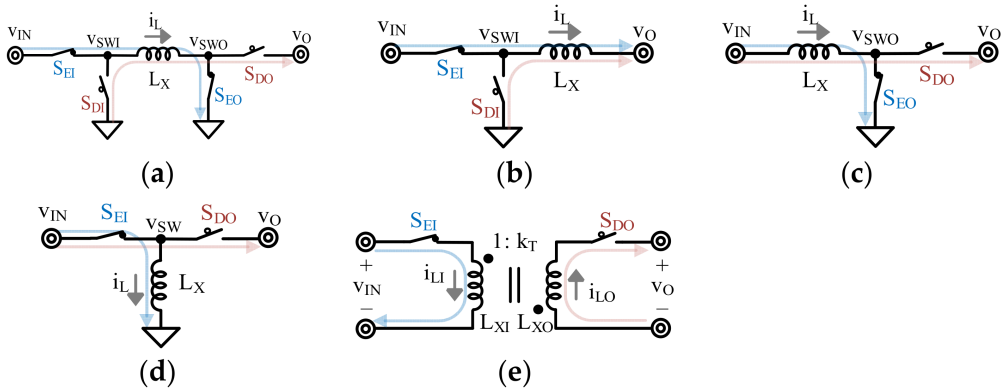

Figure 3. Switched-inductor topologies with energizing and drain phases shown with blue and red markings respectively. (**a**) Buck–Boost, (**b**) Buck, (**c**) Boost, (**d**) Inverting Buck–Boost, (**e**) Flyback.

2.3. Systemic Offset Error

Voltage regulators employ negative feedback loops around switched inductors to set and regulate v_O at v_O'. Figure 4 shows a basic negative feedback loop. The feedback factor, β_{FB}, senses and translates v_O into of the forward gain that amplifies the difference between the ideal control voltage, v_C, and v_{FB} to produce a feedback voltage, v_{FB}. A_{FW} is the part of the forward gain that amplifies the difference between the control voltage, v_C and v_{FB} to produce a duty cycling voltage, v_E'. v_E' controls the alternate conduction of the switch pairs in the following switched-inductor stage. Therefore, v_E' duty cycles at the d_E that the switched inductor needs to produce the target, v_O'.

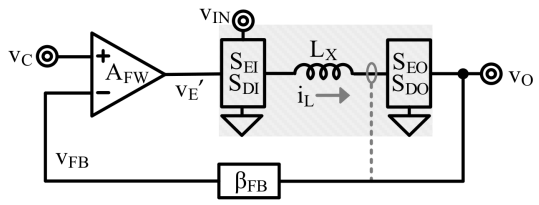

Figure 4. Basic negative feedback loop around a switched-inductor stage shown in the shaded area.

We define the systemic offset error, v_{OS} as the difference between v_C and v_{FB}. Since v_O is a β_{FB} fraction of v_{FB}, it can be expressed in terms of v_{OS}:

$$v_O = \frac{v_{FB}}{\beta_{FB}} = \frac{v_C - v_{OS}}{\beta_{FB}}. \tag{3}$$

The typical feedback loop design process begins with a key assumption that v_{OS} is negligibly small. Thus, either β_{FB} or v_C is fixed and the other is estimated according to the regulator's target, v_O', using the following approximation:

$$\beta_{FB} = \frac{v_C - v_{OS}}{v_O'}\bigg|_{v_{OS} \approx 0} \approx \frac{v_C}{v_O'} \tag{4}$$

When v_{OS} is not zero, however, the above approximation for β_{FB} (or v_C) is invalid. This results in a systemic output voltage error, $v_{Err.}$ We define v_{Err} as the difference between the steady-state output, v_O, and its target, v_O':

$$v_{Err} = v_O - v_O' = \frac{v_C - v_{OS} - v_O'\beta_{FB}}{\beta_{FB}} \quad (5)$$

Thus, the systemic offset error, referred to as the "offset" in the remainder of the paper, determines the steady-state output error. It is therefore crucial to quantify how offsets scale with circuit parameters and operating conditions. Offset expressions derived in the following sections provide crucial insight into the factors that affect the voltage regulator's DC accuracy.

3. Pulse-Width Modulation

3.1. Comparator

Figure 5a shows a comparator, CP, that compares inputs v_P and v_N to produce an output, v_O. v_O reaches output level high, V_{OH}, when v_P exceeds v_N, or when the difference between v_P and v_N, v_{ID}, exceeds zero. Conversely, when this differential input falls below zero, the output swings across $\Delta v_{O(MAX)}$ to reach output level low, V_{OL}. The transfer characteristics of the ideal CP are shown in Figure 5b.

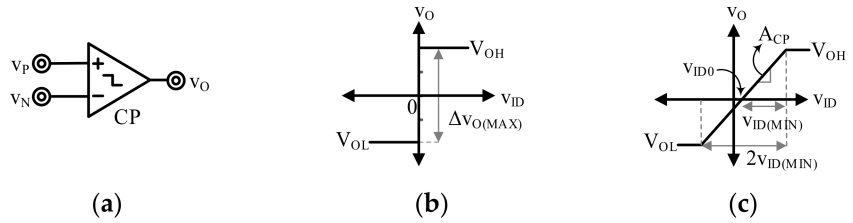

Figure 5. (**a**) Ideal comparator. (**b**) Ideal transfer characteristics. (**c**) Practical transfer characteristics.

In practice, however, comparators have finite gain, A_{CP}. As a result, v_P and v_N must differ by at least $\pm v_{ID(MIN)}$ for v_O to attain either V_{OH} or V_{OL}. Moreover, typically, CP has an input referred offset of v_{ID0}, such that the output swing is centered around v_{ID0} instead of zero. The transfer characteristics of a practical CP are shown in Figure 5c.

In the practical CP above, v_{ID} must traverse at least $2v_{ID(MIN)}$ for the output to swing across $\Delta v_{O(MAX)}$. The ratio of $\Delta v_{O(MAX)}$ to $2v_{ID(MIN)}$ is the gain, A_{CP}, of the comparator. The overdrive factor, K_O, is the factor by which the actual applied input swing, Δv_{ID}, is greater than the minimum swing, v_{ID}. Therefore, K_O should at least be unity for the comparator to assert a clear digital state at the output.

$$K_O = \frac{\Delta v_{ID}}{\Delta v_{ID(MIN)}} = \frac{\Delta v_{ID}}{2v_{ID(MIN)}} \quad (6)$$

Furthermore, the response of the comparator to an input swing is not instantaneous. The propagation delay, t_P, is defined as the time difference between the halfway point of the instantaneous step differential input and that of the resulting output transition. This is illustrated in Figure 6.

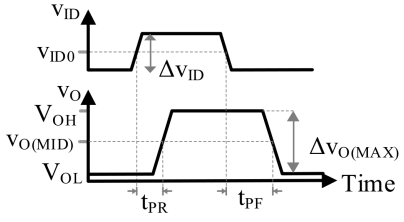

Figure 6. Propagation delays in a comparator.

Since the response of CP is limited by its bandwidth-setting pole, it behaves like an RC stage with a time constant, τ_{BW}. If $t_{P(BW)}$ is the time that an RC stage takes to swing v_O halfway across $\Delta v_{O(MAX)}$, then

$$\begin{aligned} 0.5\Delta v_{O(MAX)} &= \Delta v_{ID} A_{CP} \left(1 - e^{-\frac{t_{P(BW)}}{\tau_{BW}}}\right) \\ &= K_o \Delta v_{ID(MIN)} A_{CP} \left(1 - e^{-\frac{t_{P(BW)}}{\tau_{BW}}}\right) \end{aligned} \tag{7}$$

so that

$$t_{P(BW)} = \tau_{BW} \ln\left(1 - \frac{1}{2K_O}\right)^{-1}. \tag{8}$$

Moreover, the comparator also needs time $t_{P(SR)}$ to slew its effective load capacitance, C_O, up to $0.5\Delta v_{O(MAX)}$ with an output current, i_O. As a result, the overall propagation delay, t_P, is the sum of $t_{P(BW)}$ and $t_{P(SR)}$:

$$t_P = t_{P(BW)} + t_{P(SR)} = t_{P(BW)} + C_O\left(\frac{0.5\Delta v_{O(MAX)}}{i_O}\right). \tag{9}$$

In practice, signals do not step instantaneously but rather ramp up or down in finite time. Therefore, the overdrive factor, K_O, varies with the comparator's differential input ramp. A fast ramp transition asserts a higher effective overdrive than a slow ramp transition. As a result, comparators respond faster when v_{ID} swings across a large Δv_{ID} in a short time.

3.2. Pulse-Width Modulator

The simplest way to generate a duty cycled voltage is with a pulse-width modulator. As shown in Figure 7, the pulse-width modulator is a comparator, CP_{PWM}, that compares an input, v_I, with a sawtooth voltage, v_S, of period t_{SW}. The range of the sawtooth, Δv_S, spans from $v_{S(LO)}$ to $v_{S(HI)}$ and is equal to CP_{PWM}'s differential input swing. As the sawtooth crosses over v_I once every t_{SW}, a duty cycling voltage, v_E', is generated at the output.

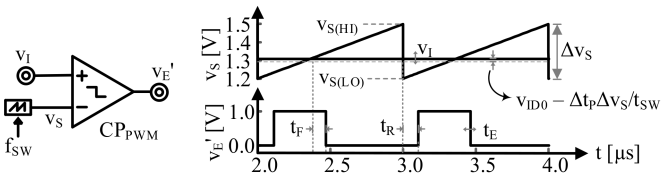

Figure 7. Duty cycle generation using pulse-width modulator.

For a duty cycle of d_E, v_I should be $d_E\Delta v_S$ above $v_{S(LO)}$ (or below $v_{S(HI)}$) when v_S is a rising (or a falling) sawtooth. Moreover, v_I should be raised (or lowered) by CP_{PWM}'s input referred offset, v_{ID0}. When a rising sawtooth is used, Δv_{ID} at the sawtooth's falling edge is fast and large. As a result, the falling delay of the output, t_{PF}, is usually longer than its rising delay, t_{PR}, by Δt_P (if a falling sawtooth is used, it is t_{PR} that would typically be longer). Therefore, v_I should be lowered (or raised) to account for Δt_P. Finally, v_I can be expressed as a function of d_E:

$$v_I = v_{S(LO/HI)} \pm d_E\Delta v_S \pm v_{ID0} \mp \Delta t_P\left(\frac{\Delta v_S}{t_{SW}}\right). \tag{10}$$

Note that CP_{PWM} rails when the input v_I goes up to or above $v_{S(HI)}$ or below $v_{S(LO)}$. The range of v_I is therefore Δv_S. Moreover, the output duty cycle ranges between d_E = 0% and d_E = 100%. As a result, the pulse-width modulation gain from v_I to d_E is expressed as

$$A_{PWM} = \frac{\Delta d_E}{\Delta v_I} = \frac{1 - 0}{v_{S(HI)} - v_{S(LO)}} = \frac{1}{\Delta v_S}. \tag{11}$$

3.3. Basic Voltage Loop

Figure 8 shows the PWM basic voltage loop. CP_{PWM} produces the d_E that controls the switches in the following ideal switched-inductor stage. β_{FB} senses and translates v_O to v_{FB}. We define the difference between the control voltage, v_C, and v_{FB} as the voltage loop offset, v_{VOS}. The error amplifier, A_{VE}, amplifies v_{VOS} to produce the amplified error voltage, v_{EO}. This v_{EO} results in a d_E according to (10). The output capacitor, C_O, is used to supply a continuous load current, i_{LD}, when S_{DO} opens.

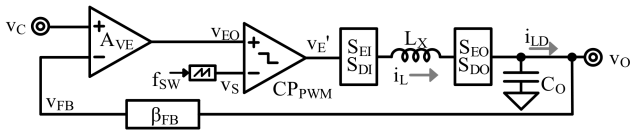

Figure 8. PWM basic voltage loop.

In practice, A_{VE} produces an output voltage, v_{EO0}, even when its differential input is zero. This is the output offset of A_{VE}. v_{VOS} is therefore expressed as

$$v_{VOS} = v_C - v_{FB} = \frac{v_{EO} - v_{EO0}}{A_{VE}} = \frac{v_{S(LO/HI)} \pm d_E \Delta v_S \pm v_{ID0} \mp \Delta t_P \left(\frac{\Delta v_S}{t_{SW}}\right) - v_{EO0}}{A_{VE}}. \quad (12)$$

Consider a buck regulator as an example of the basic voltage loop. For simplicity, consider ideal switches, a 1 MHz rising sawtooth with $v_{S(LO)}$ = 1.2 V and Δv_S = 300 mV, v_{IN} = 5 V and i_L = 2 A. The target voltage for this buck ranges from 1.2 V to 4.5 V, depending on the application. The corresponding d_E is calculated from (2) and ranges from 24% to 90%. β_{FB} is fixed at 0.48 V, and v_C is scaled to produce the target v_O' according to (4).

The solid grey trace in Figure 9 shows v_{VOS} as a linear function of d_E. As expected from (12), the slope of its rise is the reverse translation of the gain across A_{VE} and CP_{PWM}. As described in Section 2, this v_{VOS} results in a steady-state output error, v_{Err}, given by (5). As shown in the grey trace in Figure 10, v_{Err} worsens as v_{VOS} rises with d_E.

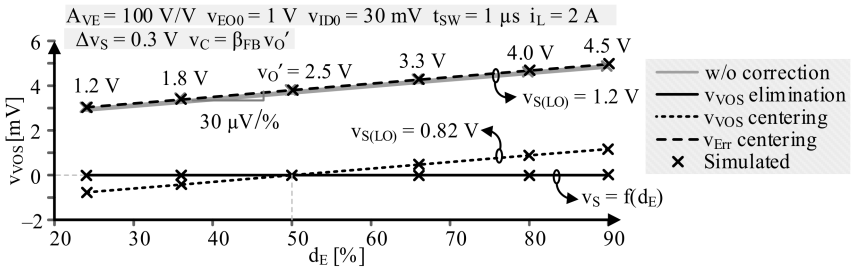

Figure 9. v_{VOS} vs. d_E.

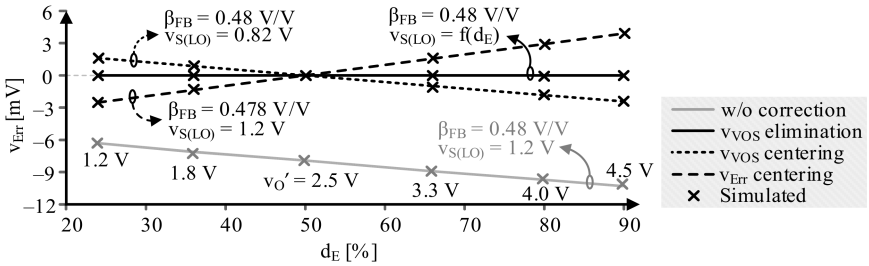

Figure 10. Corresponding v_{Err} vs. d_E.

3.3.1. Offset Elimination

Equation (12) hints at a way of eliminating v_{VOS} to restore output accuracy. v_{VOS} vanishes when v_{EO} matches v_{EO0}. v_{EO}, however, is constituted by the comparator's v_{ID0}

and $t_{PR/F}$; the sawtooth's $v_{S(LO/HI)}$, Δv_S and t_{SW}; and the regulator's d_E. The latter is fixed by the application. Moreover, v_{ID0} and $t_{PR/F}$ as well as v_{EO0} are unintended byproducts of the design and fabrication, while Δv_S affects the loop gain [27]. $v_{S(LO/HI)}$, however, is a flexible design variable that does not affect loop gain and stability. Therefore, we shift the sawtooth limits without affecting its range, such that

$$\begin{aligned} v_{S(LO/HI)} &= v_{EO0} \mp d_E \Delta v_S \mp v_{ID0} \pm \tfrac{\Delta t_P \Delta v_S}{t_{SW}}, \\ v_{S(HI/LO)} &= v_{S(LO/HI)} \pm \Delta v_S. \end{aligned} \tag{13}$$

In Figure 9, the solid black trace shows offset elimination when the sawtooth is designed according to (13) for each target, d_E, of the buck regulator. With v_{VOS} eliminated, the approximation in (4) is valid and v_{Err} is consistently zero, as shown by the solid black trace in Figure 10.

3.3.2. Centering Across v_{IN}:v_O Ratios

The input voltage in practical switching regulators suffers from line variations. Moreover, as seen above, v_O' may change with application. These variations in v_{IN} and v_O are encapsulated within d_E and manifest as changes in v_{VOS} according to (12). v_{VOS} therefore determines the steady-state line regulation accuracy of the regulator.

It may not always be feasible to shift the sawtooth for every possible combination of v_{IN} and v_O. It is useful, however, to eliminate v_{VOS} and/or v_{Err} at the center of the range of possible variations. Therefore, eliminating v_{VOS} and/or v_{Err} at the average d_E lowers the steady-state output error across the range of d_E. This is referred to as "centering".

Centering v_{VOS}: In Figure 9, the dotted black trace plots v_{VOS} after it has been centered at d_E = 50% by using a sawtooth that satisfies (13) at d_E = 50%. When d_E varies from this center, v_{VOS} re-emerges but remains consistently lower than the previous case. Even in the worst case (lowest d_E), v_{VOS} centering reduces v_{VOS} by 74.6% w.r.t. the default. The corresponding v_{Err} is shown by the dotted black trace in Figure 10. The worst case of v_{Err} is when v_{Err} is largest relative to the target output voltage. With v_{VOS} centering, v_{Err} also undergoes a reduction of at least 74.6% in the worst case.

Centering v_{Err}: Alternatively, when v_{VOS} is known, the regulator's control voltage and β_{FB} can be calculated accurately without the approximation in (4). The current example uses a fixed β_{FB} and a variable v_C. Therefore, by accounting for v_{VOS} at d_E = 50% in β_{FB}, v_{Err} is eliminated at the center of the d_E range. The dashed black trace in Figure 10 shows v_{Err} when β_{FB} is lowered to 478 mV/V. With v_{Err} centering, the absolute v_{Err} undergoes a reduction of at least 60.3% (at the lowest d_E).

3.4. Current-Mode Voltage Loop

Current-mode voltage loops employ a current-regulating negative feedback loop inside the outer voltage loop. Figure 11 illustrates a PWM current-mode voltage loop. A_{VE} inputs v_{EO} as the control voltage for the inner loop. The current feedback factor, β_{IFB}, senses i_L and translates it into v_{IFB}, the current feedback voltage. The difference between v_{EO} and v_{IFB} is the current loop offset, v_{IOS}.

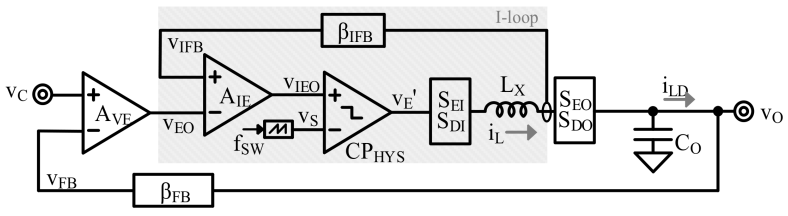

Figure 11. PWM current-mode voltage loop.

Like A_{VE}, A_{IE} also produces an output, v_{IEO0}, when its differential input is zero. Therefore, v_{IOS} is expressed as

$$v_{IOS} = v_{EO} - v_{IFB} = \frac{v_{IEO} - v_{IEO0}}{A_{IE}} = \frac{v_{S(LO/HI)} \pm d_E \Delta v_S \pm v_{ID0} \mp \Delta t_P \left(\frac{\Delta v_S}{t_{SW}}\right) - v_{IEO0}}{A_{IE}}. \quad (14)$$

Like v_{VOS} in the basic voltage loop, v_{IOS} is the reverse gain translation of d_E across A_{IE} and CP_{PWM}. Moreover, the current-mode voltage loop also suffers from a voltage loop offset given as

$$v_{VOS} = \frac{v_{EO} - v_{EO0}}{A_{VE}} = \frac{(v_{IOS} + i_L \beta_{IFB}) - v_{EO0}}{A_{VE}}. \quad (15)$$

Thus, v_{VOS} is the reverse gain translation of d_E across CP_{PWM}, A_{IE} and A_{VE}.

Consider the PWM current-mode voltage loop implementation of the previous buck example. Once again, $v_{S(LO)}$ = 1.2 V, Δv_S = 300 mV, v_{IN} = 5 V, i_L = 2 A and v_O' ranges from 1.2 V to 4.5 V. Additionally, β_{IFB} = 1 V/A. This time, v_C is fixed at 1.2 V and the required output voltage is realized by scaling β_{FB}. The grey trace in Figure 12 shows the variation in v_{IOS} with a rising d_E. It rises with d_E at a slope given by (14).

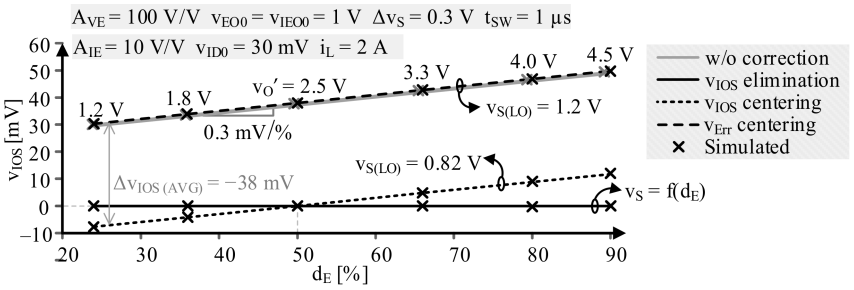

Figure 12. v_{IOS} vs. duty cycle.

The voltage loop offset also rises with d_E according to (15) and is plotted as the grey trace in Figure 13. The rise in v_{VOS} is attenuated with the combined high gain of A_{VE} and A_{IE}. The steady-state output error in this buck is shown with the grey trace in Figure 14. Because of v_{Err}, neither v_O nor d_E match their respective targets.

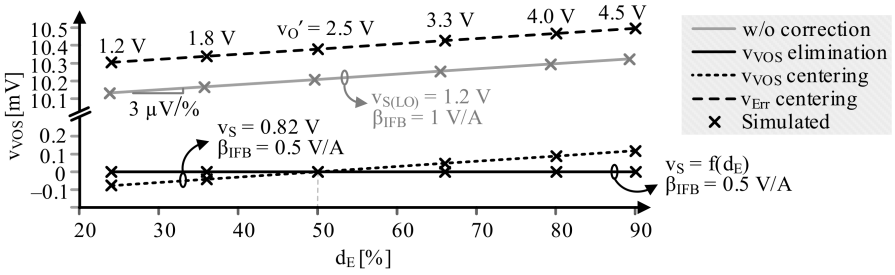

Figure 13. v_{VOS} vs. duty cycle.

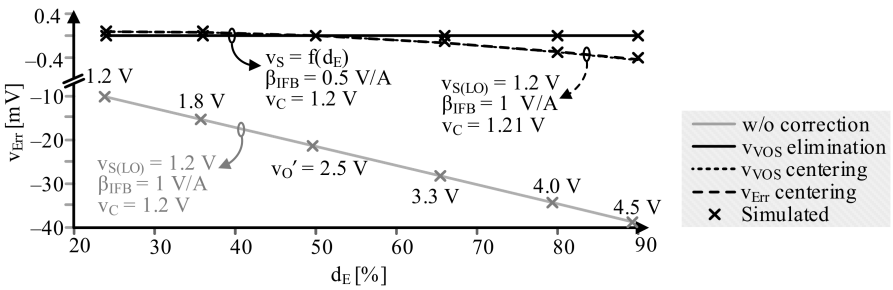

Figure 14. v_{Err} vs. duty cycle.

3.4.1. Offset Elimination

Since v_{IOS} is of the same form as v_{VOS} in the basic voltage loop, it can be eliminated by shifting the sawtooth according to the regulator's target, d_E, as shown in (13). This is shown by the solid black trace in Figure 12. Furthermore, v_{VOS} vanishes when the numerator in (14) becomes zero. For this, the current feedback factor, β_{IFB}, can be adjusted as follows:

$$\beta_{IFB} = \frac{v_{EO0} - v_{IOS}}{i_L}. \quad (16)$$

The solid black trace in Figure 13 shows v_{VOS} when β_{IFB} is adjusted for each d_E. With both v_{IOS} and v_{VOS} eliminated, the output error is consistently zero, as shown by the solid black trace in Figure 14.

3.4.2. Centering Across the v_{IN}:v_O Ratio

Like before, eliminating offsets and/or v_{Err} at d_E = 50% lowers the output error across the range of d_E. The dotted black traces in Figures 12 and 13 show v_{IOS} and v_{VOS} centered by shifting v_S and β_{IFB} according to (13) and (16). Thus, the v_{IOS} reduces by at least 76%. Since v_{VOS} variation is already limited by the combined gain of A_{VE} and A_{IE}, centering only at one d_E setting reduces v_{VOS} by at least 98.8% across d_E. With such a drastic reduction in v_{VOS}, the loop has almost no v_{Err}, as shown by the dotted black trace in Figure 14.

We note that since β_{IFB} is a current sensor, it is not always straightforward to adjust it precisely to eliminate or center v_{VOS}. In such cases, it is useful to accommodate v_{VOS} at d_E = 50% in the design of the voltage feedback factor, β_{FB}, or in the choice of the control voltage, v_C, in the first place. This centers v_{Err} without requiring any correction in offsets. In the present example, β_{FB} is fixed and v_C is raised to 1.21 V to account for the center v_{Err}. This is shown by the dashed black trace in Figure 14. With v_{Err} centering, v_{Err} reduces by at least 98.9% in the worst case across d_E.

3.5. Loading Effect

Consider the steady state after a sudden rise in the load current, i_{LD}, and hence in i_L in the current-mode voltage loop buck. To supply an increased i_L, the v_{VOS} must rise, according to (15). To accommodate this increased v_{VOS}, v_{FB} and v_O settle at values lower than their targets, since β_{FB} is fixed. With a lower v_O, the corresponding d_E and v_{IOS} are lower. Thus, while the voltage loop offset rises with i_{LD}, the current loop offset falls. Thus, the v_{IOS}, v_{VOS}, d_E and v_O suffer from an inherent loading effect in current-mode voltage loops.

Consider, for example, the current-mode voltage loop implementation of a buck voltage regulator. d_E in (13) is rewritten as the ratio of v_O to v_{IN} in bucks, so that

$$v_{IOS} = \frac{\left[v_{S(LO)} + \frac{(v_C - v_{VOS})}{v_{IN}\beta_{FB}}\Delta v_S + v_{ID0} - \Delta t_P\left(\frac{\Delta v_S}{t_{SW}}\right)\right] - v_{IEO0}}{A_{IE}}. \quad (17)$$

Solving (17) and (15) simultaneously reveals the dependence of v_{IOS} on i_L, which is the same as the load current, i_{LD}, in bucks:

$$v_{IOS} \propto -i_L\left(\frac{\beta_{IFB}}{1 + \frac{A_{VE}A_{IE}v_{IN}\beta_{FB}}{\Delta v_S}}\right). \quad (18)$$

The grey trace in Figure 15 shows the variation in the current loop offset when the previous buck example is used to supply a load current ranging from 0.5 A to 3.5 A at the

output target of 2.5 V. The slope of v_{IOS} is limited by the denominator term in (18), which denotes the loop gain of the buck regulator.

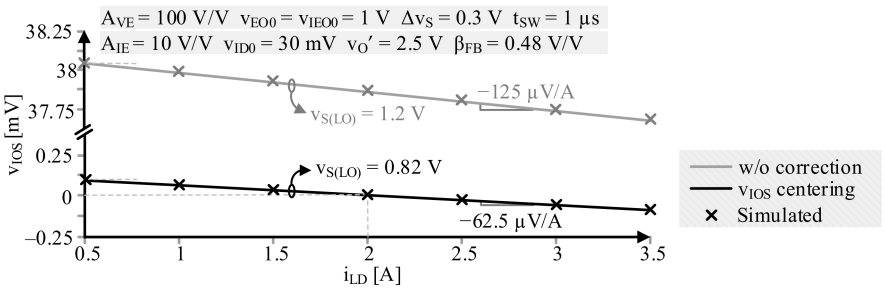

Figure 15. v_{IOS} vs. i_{LD}.

Since v_{IOS} varies very little with i_{LD}, v_{VOS} is largely a function of the load according to (15). The grey trace in Figure 16 shows the wide variation in v_{VOS} across different loading conditions. This resulting v_{Err} is shown by the grey trace in Figure 17. The output voltage is up to 2% below its target in the worst case, as denoted by the absolute percentage steady-state error, $|v_{Err\%}|$, in Figure 17.

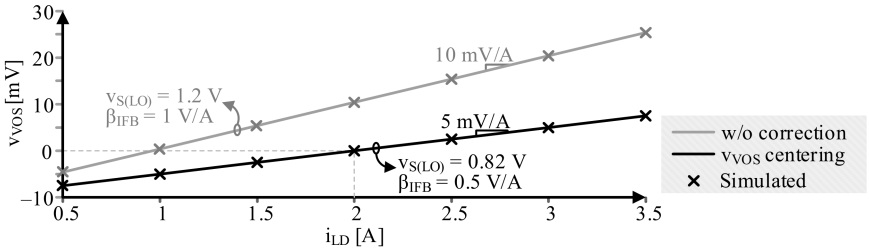

Figure 16. v_{VOS} vs. i_{LD}.

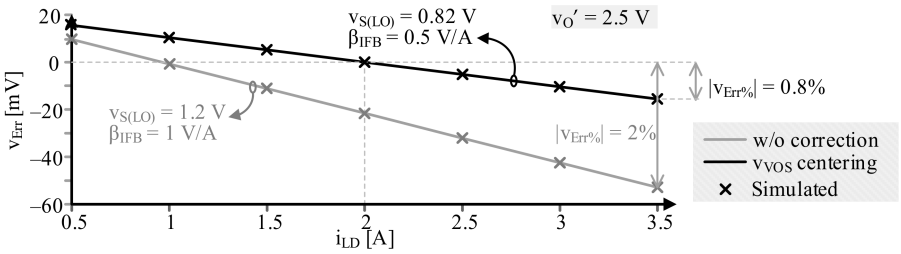

Figure 17. v_{Err} vs. i_{LD}.

Centering Across Load

If the range of the load current is known, it is useful to center v_{Err} or v_{VOS} at the most probable value of the load current, typically the average, $i_{LD(AVG)}$. Offsets in the above example are eliminated at $i_{LD(AVG)}$ = 2 A by lowering $v_{S(LO)}$ and β_{IFB} according to (13) and (16). This is shown by the solid black traces in Figures 15 and 16. Centering balances v_{Err} around zero, making the output voltage variation symmetric, and limited to only 0.8% around its target. This is shown by the solid black trace in Figure 17.

4. Peak–Valley Control

4.1. Hysteretic Comparator

Hysteretic comparators add hysteresis at the crossover point of a comparator. Hysteretic comparator CP_{HYS} in Figure 18a compares the difference, v_{ID}, between inputs v_P and v_N with an upper threshold, $v_{T(HI)}$, when v_{ID} is rising and with a lower threshold, $v_{T(LO)}$, when v_{ID} is falling. Therefore, the output, v_O, reaches V_{OH} when v_{ID} exceeds $v_{T(HI)}$, and V_{OL} when v_{ID} falls below $v_{T(LO)}$. The difference between the two thresholds is the

hysteretic window or Δv_T. When v_{ID} is within the hysteresis window, v_O does not change states. The transfer characteristics are shown in Figure 18b.

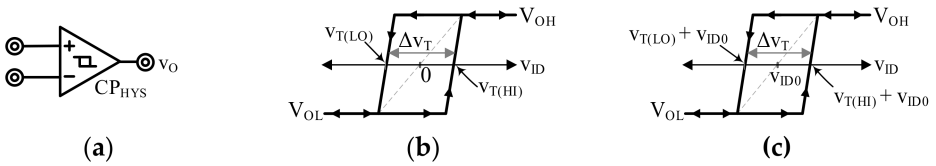

Figure 18. (**a**) Hysteretic comparator. (**b**) Ideal. (**c**) Practical transfer characteristics.

In practice, CP_{HYS}'s input referred offset of v_{ID0} raises both $v_{T(HI)}$ and $v_{T(LO)}$ by v_{ID0}. This is shown in Figure 18c. Moreover, like comparators, hysteretic comparators also suffer from rising and falling propagation delays.

4.2. Hysteretic (Peak Valley)

4.2.1. Duty Cycler

The duty cycling voltage, v_E', in the peak valley control is generated using the current loop illustrated in Figure 19. This control is more popularly known as hysteretic control [27]. β_{IFB} is typically unity. Therefore, v_{IFB} is a replica of i_L, falling and rising at slopes proportional to energizing and drain voltages, v_E and v_D.

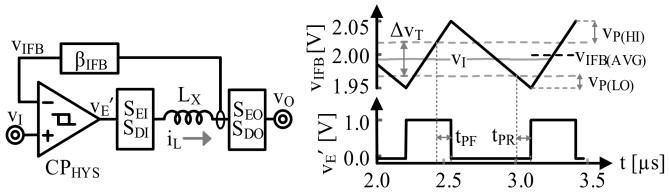

Figure 19. Duty cycle generation in hysteretic control.

The input, v_I, establishes a symmetric hysteresis window of Δv_T about itself. During energizing time t_E, i_L and v_{IFB} rise until v_{IFB} reaches $0.5\Delta v_T$ above v_I. When this happens, v_E' resets, beginning t_D for the following switched-inductor stage. As a result, i_L and v_{IFB} fall until v_{IFB} reaches $0.5\Delta v_T$ below v_I. When this happens, v_E' sets, initiating t_E again. Thus, by determining t_E and t_D, the hysteretic current loop effectively establishes the required d_E.

In actuality, due to rising and falling propagation delays, t_{PR} and t_{PF}, CP_{HYS} cannot set and reset v_E' instantaneously. Therefore, until CP_{HYS} responds, v_{IFB} continues to rise or fall beyond the threshold limits. The extent by which v_{IFB} projects beyond $v_{T(HI/LO)}$ is referred to as its projection, $v_{P(HI/LO)}$, and is given by

$$v_{P(HI/LO)} = t_{PF/PR}\frac{v_{E/D}}{L_X}\beta_{IFB}. \quad (19)$$

4.2.2. Current-Mode Voltage Loop

Figure 20 shows the hysteretic current-mode voltage loop. A_{VE} feeds the amplified error voltage, v_{EO}, as an input to the inner hysteretic current loop. v_{EO} therefore sets the limits, $v_{T(HI/LO)}$, by establishing a hysteretic window of Δv_T around itself.

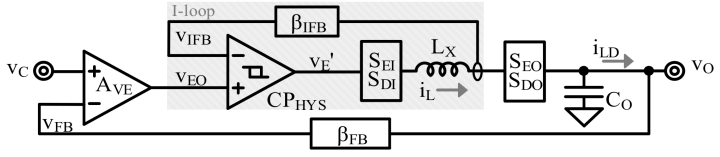

Figure 20. Hysteretic current-mode voltage loop.

The current loop offset in this loop is the difference between v_{EO} and v_{IFB} in the steady state. Ideally, v_{IFB} swings within a symmetric hysteretic window around v_{EO}. Therefore, its average, $v_{IFB(AVG)}$, is equal to v_{EO}. However, with projections $v_{P(HI)}$ and $v_{P(LO)}$, $v_{IFB(AVG)}$ shifts away from v_{EO}, giving rise to a non-zero v_{IOS}. Moreover, CP_{HYS}'s input referred offset adds to v_{IOS}, such that

$$v_{IOS} = v_{EO} - v_{IFB(AVG)} = -\frac{v_{P(HI)} - v_{P(LO)}}{2} + v_{ID0} = \frac{t_{PR}v_D - t_{PF}v_E}{2L_X}\beta_{IFB} + v_{ID0}. \quad (20)$$

From (2), d_E is directly proportional to v_D and inversely proportional to v_E. Therefore, v_{IOS} in (20) is ultimately directly proportional to the effective d_E that the hysteretic current loop sets.

Consider a hysteretic current-mode voltage loop buck with similar specifications to the previous example. The control voltage is held constant at 1.2 V, while β_{IFB} is scaled to produce a range of output voltages. As d_E rises, the current loop offset grows according to (20). The grey trace in Figure 21 shows the variation in the resulting v_{IOS} as d_E varies.

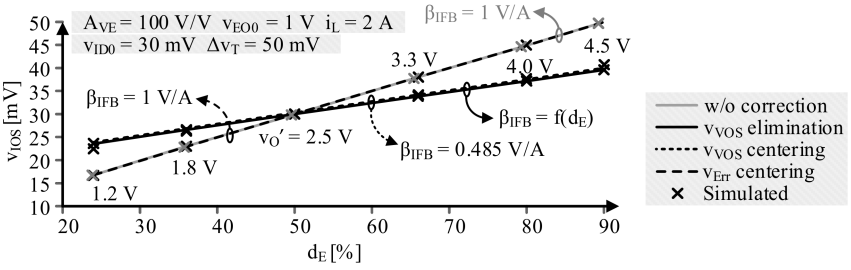

Figure 21. v_{IOS} vs. duty cycle.

The outer voltage loop in this case is the same as that in the PWM current-mode voltage loop presented in the previous section. Therefore, v_{VOS} follows the expression given by (15). The grey trace in Figure 22 shows the variation in v_{VOS} with d_E. As expected, v_{VOS} rises with d_E in the same way v_{IOS} does. The resulting v_{Err} is plotted as the grey trace in Figure 23.

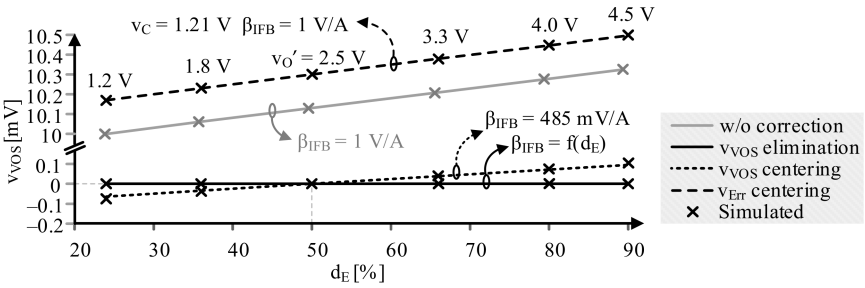

Figure 22. v_{VOS} vs. duty cycle.

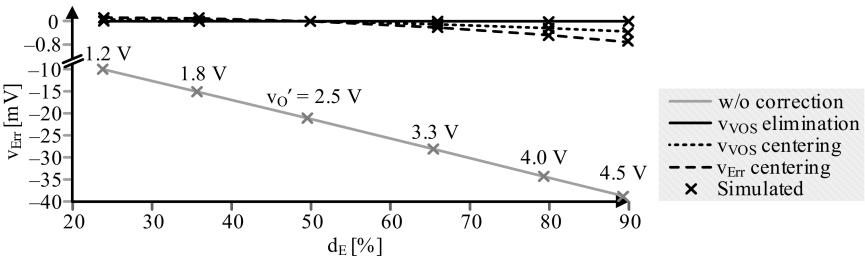

Figure 23. Corresponding steady-state output error vs. duty cycle.

Offset Elimination: In hysteretic control, v_{IOS} is the result of the offset and propagation delays of CP_{HYS}, which are always non-zero in practice. However, since v_{VOS} lends itself to

the same expression as in the PWM current-mode voltage loop (15), we use β_{IFB} adjustment, as described in Section 3, to eliminate v_{VOS}. The solid black trace in Figure 22 shows v_{VOS} when the loop uses β_{IFB} calculated using (16). Lowering β_{IFB} this way also reduces the slope of v_{IOS} with respect to d_E. The solid black traces in Figures 21 and 23 show the corresponding v_{IOS} and v_{Err} when v_{VOS} is eliminated. With zero v_{VOS}, the regulator's output voltage always matches its target, resulting in zero v_{Err}.

Centering across the v_{IN}:v_O Ratio: The dotted black traces in Figures 21–23 show offsets and v_{Err} when v_{VOS} is centered at d_E = 50% by adjusting β_{IFB}. The reduction in β_{IFB} decreases the slope of v_{IOS} and reduces the worst-case v_{VOS} and v_{Err} by 98.9% across d_E.

Alternatively, choosing an accurate v_C in the first place is another way of eliminating v_{Err}. We do so by accounting for v_{VOS} at d_E = 50% in (3). The dashed black traces in Figures 21–23 show offsets and v_{Err} when v_C is 1.22 V instead of 1.2 V. While offsets remain, v_{Err} is significantly lower than in the default case. In this example, the worst-case absolute v_{Err} reduces by 98.9% w.r.t. the default case (grey trace).

4.2.3. Loading Effect

As before, the voltage loop needs a higher v_{VOS} to supply an increased steady-state load current. To account for the rising v_{VOS}, v_O and therefore v_D settle below their targets, resulting in a lower v_{IOS}. In effect, v_{IOS}, the hysteretic current-mode voltage loop, suffers from a similar loading effect to the PWM current-mode voltage loop. Figure 24 shows v_{IOS} varying under the effect of a rising i_{LD} when the buck targets an output voltage of 2.5 V.

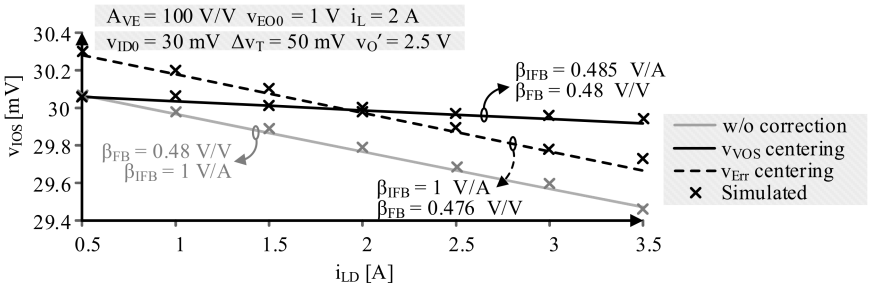

Figure 24. v_{IOS} versus load current.

Like v_{VOS} in the PWM current-mode voltage loop, the voltage loop offset here also follows (15) and rises with the load current. v_{VOS} and the resulting steady-state error are plotted in the grey trace in Figures 25 and 26.

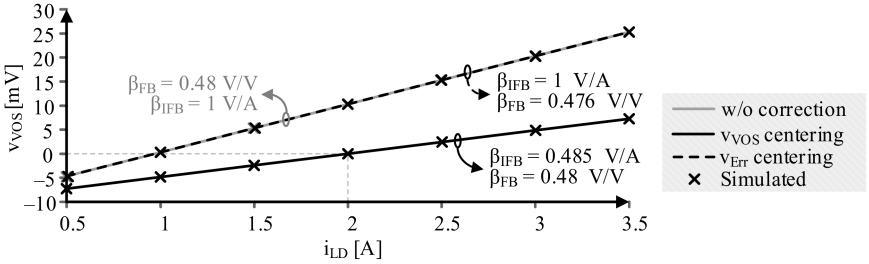

Figure 25. v_{VOS} versus load current.

Centering Load: Once again, we eliminate v_{VOS} at the average load current of 2 A by reducing β_{IFB} from 1 V/A to 485 mV/A according to (16). The solid black traces in Figures 24–26 show how offsets and v_{Err} improve with v_{VOS} centering. The output voltage deviates by only 0.6% about its target, which is over three times better than the default worst-case deviation of 2%. v_{Err} is also balanced about zero so that v_O varies equally during equally high or low load demands.

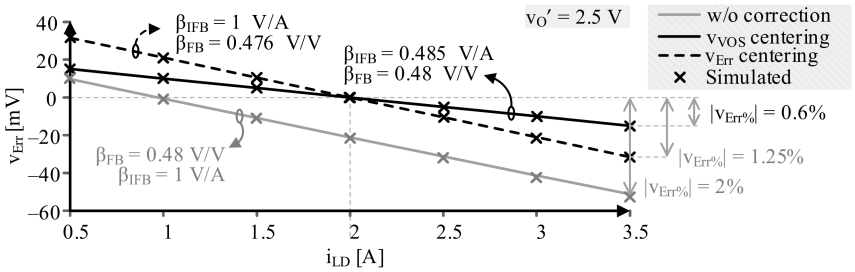

Figure 26. Corresponding steady-state error versus load current.

Alternatively, the v_{VOS}, calculated using (15), can be used in (3) to arrive at the precise β_{FB} that eliminates v_{Err} at $i_{L(AVG)}$. This v_{Err} centering is shown by the dashed black trace in Figures 24–26. As with v_{VOS} centering, the output voltage is balanced around its target and deviates by about 1.25% across the load current range in this example.

4.3. Peak

4.3.1. Duty Cycler

The duty cycler in peak control is shown in Figure 27. It consists of the comparator, CP_{PV}, that trips its output, v_{IO}, high when v_{IFB} rises to the level of the input voltage v_I. When this happens, the set-dominant reset-enabled flip flop, SR_{OFF}, pulses v_E' low, thus initiating the drain time, t_D. v_{IFB} then falls from v_I across Δv_{IFB}. Thus, CP_{PV} and SR_{OFF} detect and limit the peak of v_{IFB}. v_{IFB} continues to fall until the delayed complement of v_E', v_{DX}' sets SR_{OFF} and ends t_D. This fixed delay, t_X, therefore determines the off time of v_E' and the drain time for the switched inductor. For this reason, peak control is also known as constant off-time control. The time that v_{IFB} takes to rise to v_I at the rate that v_E allows sets the energizing time. This way, peak control realizes the target d_E.

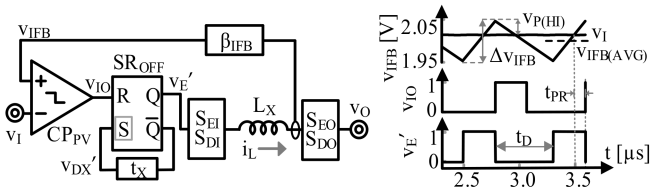

Figure 27. Duty cycle generation in peak control.

4.3.2. Current-Mode Voltage Loop

Figure 28 shows the peak-controlled current-mode voltage loop. Like before, the A_{VE} of the outer loop feeds the input to the inner current loop. The difference between the steady-state v_{EO} and $v_{IFB(AVG)}$ is v_{IOS}. Since v_{EO} is the peak of v_{IFB}, $v_{IFB(AVG)}$ is already half Δv_{IFB} away from v_{EO}. Moreover, CP_{PV}'s rising propagation delay allows v_{IFB} to rise above v_{EO} by a projection, $v_{P(HI)}$. Also, the input referred offset of CP_{PV} lowers v_{IOS}, such that

$$v_{IOS} = v_{EO} - v_{IFB(AVG)} = \frac{\Delta v_{IFB}}{2} - v_{P(HI)} - v_{ID0} = \frac{\Delta v_{IFB}}{2} - \left(\frac{t_{PR} v_E}{L_X}\right)\beta_{IFB} - v_{ID0}. \quad (21)$$

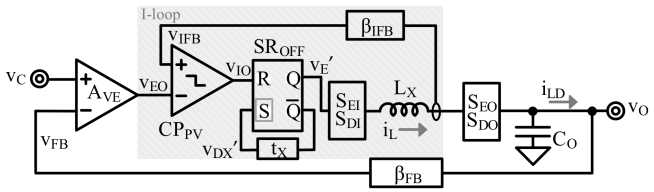

Figure 28. Peak-controlled current-mode voltage loop.

Since d_E increases as v_E rises, the current loop offset in peak control is ultimately directly proportional to d_E. We continue with the example of a buck regulator with similar operating conditions as before, now implemented using peak control with a constant off time of 515 ns. The grey trace in Figure 29 shows v_{IOS} rising with the effective d_E that the peak control loop sets. The voltage loop offset is given by (15) and rises with d_E like v_{IOS}. The grey trace in Figure 30 shows v_{VOS} in the case of this example.

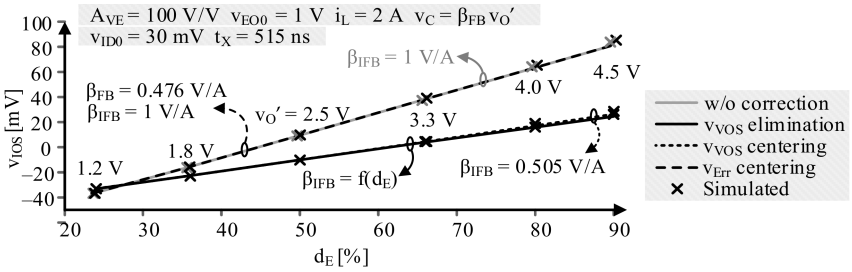

Figure 29. v_{IOS} versus energizing duty cycle.

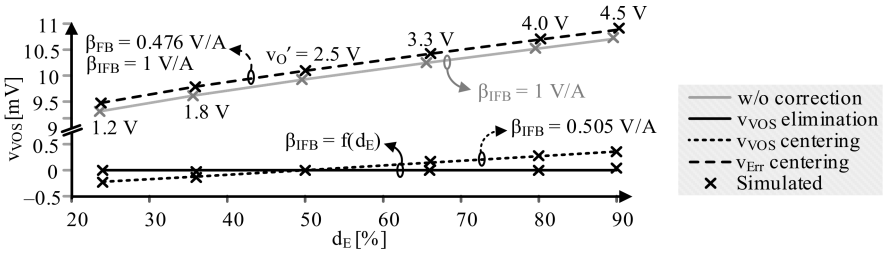

Figure 30. v_{VOS} versus energizing duty cycle.

As expected, the rising v_{Err} worsens as v_{VOS} grows according to (6). The resulting v_{Err}, shown as the grey trace in Figure 31, causes v_O to be below its target by up to 22 mV (2% in the worst case).

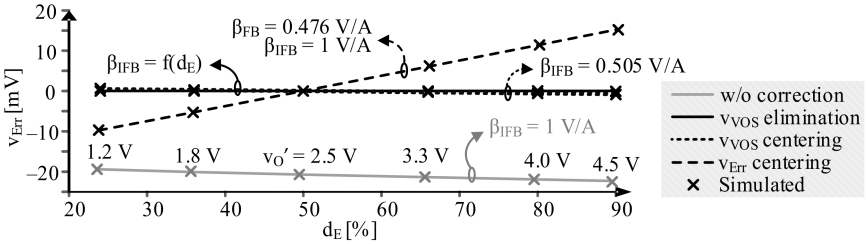

Figure 31. Corresponding steady-state output error versus energizing duty cycle.

Offset Elimination: v_{IOS} in peak control is the consequence of an inevitable ripple in v_{IFB} and comparator propagation delays and is therefore non-zero. v_{VOS}, however, still follows (15) and therefore can be eliminated by adjusting β_{IFB}, as in all the previous examples. The black trace in Figure 30 shows v_{VOS} elimination when β_{IFB} has been adjusted throughout the d_E range according to (15). Lowering β_{IFB} this way also attenuates the slope of v_{IOS} according to (21). This is evident from the solid black trace in Figure 29. With v_{VOS} elimination, the output voltage always matches its target, so that v_{Err} is consistently zero, as shown by the solid black trace in Figure 31.

Centering across the v_{IN}:v_O Ratio: We lower and fix β_{IFB} at about 505 mV/A to center v_{VOS} at d_E = 50%. This reduces the swing of v_{IOS}, lowers v_{VOS} by at least 96.7% across d_E and reduces the worst v_{Err} by 84.3%. This is shown by the dotted black traces in Figures 29–31. Alternatively, v_{VOS}, calculated using (15), can be used to calculate the precise β_{FB} that removes v_{Err} at d_E = 50%, thereby centering v_{Err} instead of v_{VOS}. Thus,

while v_{VOS} remains, the absolute v_{Err} reduces to 15 mV from 22 mV (by over 32%) in the worst case.

4.3.3. Loading Effect

As discussed, the voltage loop offset in peak control follows (15) and is proportional to i_L. Therefore, a rising load dump causes v_{VOS} to rise and v_O (and d_E to fall), as discussed in previous sub-sections. v_{IOS}, being proportional to d_E, therefore falls with a rising load current. As a result, offsets in peak control suffer from a similar loading effect to those in PWM and hysteretic control. Figures 32–34 show the trend of v_{IOS}, v_{VOS} and the resulting v_{Err} with respect to load current using grey traces.

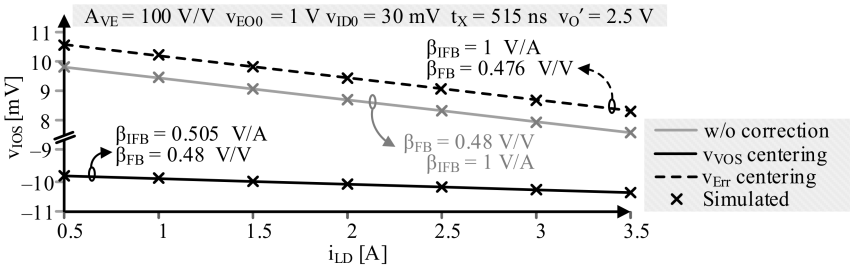

Figure 32. v_{IOS} versus load current.

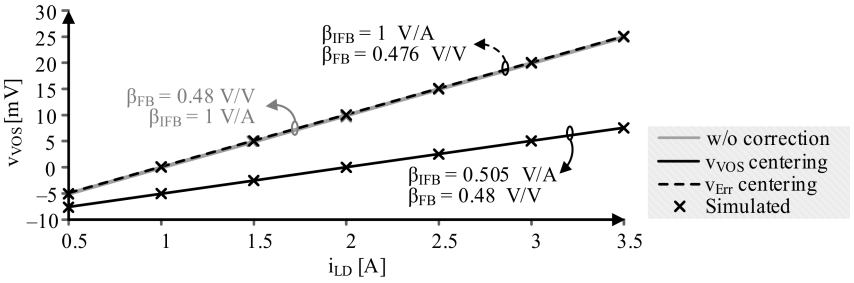

Figure 33. v_{VOS} versus load current.

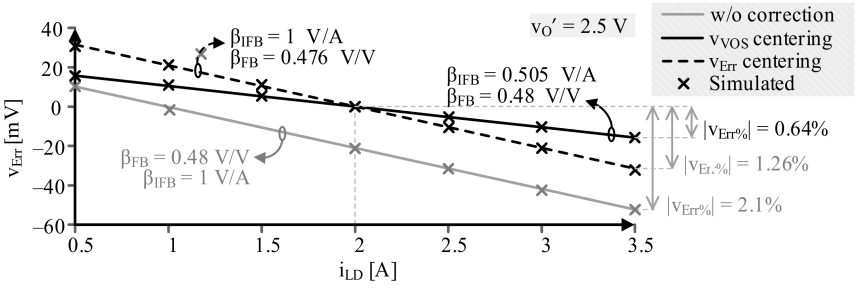

Figure 34. Corresponding steady-state output error versus load current.

Centering Load: The black trace in Figure 33 shows v_{VOS} centered at the average load current of 2 A by lowering and fixing β_{IFB} at 505 mV/A. This decreases the slope of v_{IOS} w.r.t. i_{LD}, shown by the black trace in Figure 32. With v_{VOS} centering, the output voltage deviates by only 0.64% about its target, which is over three times, or 70% lower than the default worst case of +2.1%. v_{Err} is also balanced about zero, so that v_O varies equally when the load current is equally higher or lower than its average.

Alternatively, the v_{VOS}, calculated using (15), can be used in (3) to arrive at the precise β_{FB} that eliminates v_{Err} at i_L = 2 A. The dashed black traces in Figures 32–34 show the v_{IOS}, v_{VOS}, and v_{Err} that result from this β_{FB}. The output voltage is balanced around its target and deviates by about 1.26% across the range of the load current. This represents a 40% reduction in v_{Err} w.r.t. the default case.

4.4. Valley

As its name implies, valley control works as the complement of peak control. Figure 35 illustrates the valley-controlled current-mode voltage loop. CP_{PV} detects the valley of the triangular v_{IFB} when it falls to the v_{EO} that the outer voltage loop sets. At this instant, the reset dominant set-enabled flip flop, SR_{ON}, initiates the energizing time, t_E, by pulsing v_E' high. v_E' remains high until its delayed version, v_{EX}', resets the flip flop after a fixed delay t_X. Thus, t_X sets the energizing time of the switched inductor. Therefore, valley control is also known as constant on-time control.

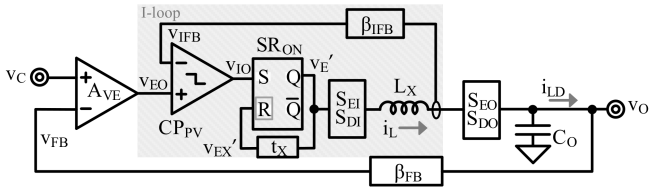

Figure 35. Valley-controlled current-mode voltage loop.

Once again, the current loop offset is the difference between v_{EO} and the steady state of the triangular v_{IFB}, given by $v_{IFB(AVG)}$. Since v_{EO} sets the valley of $v_{IFB(AVG)}$, the current loop offset is always at least equal to the negative of half the v_{IFB} ripple. In practice, the falling propagation delay of the comparator allows v_{IFB} to continue falling below v_{EO} by $v_{P(LO)}$. This adds to v_{IOS}. Moreover, the input referred offset of the comparator is adjusted to v_{IOS}, such that

$$v_{IOS} = v_{EO} - v_{IFB(AVG)} = v_{P(LO)} - \frac{\Delta v_{IFB}}{2} - v_{ID0} = \left(\frac{t_{PF} v_D}{L_X}\right)\beta_{IFB} - \frac{\Delta v_{IFB}}{2} - v_{ID0}. \quad (22)$$

Equation (22) shows that v_{IOS} in valley control is directly proportional to v_D and therefore d_E. As a result, it grows as the target voltage of the regulator rises in the same way as in previous examples. Moreover, as in all the current-mode voltage loops discussed thus far, v_{VOS} is the reverse gain translation of v_{IOS} and i_L across the amplifier, A_{VE}. It therefore follows (15) and rises with d_E. Additionally, v_{VOS} rises with i_L, such that offsets in this control suffer from a loading effect similar to that described in the previous sub-sections.

As in peak control, v_{IOS} in valley control is a consequence of the inevitable v_{IFB} ripple and comparator non-idealities. It is, however, possible to eliminate or center v_{VOS} by getting v_{IFB} to match v_{EO0} by redesigning β_{IFB} according to (16). Finally, with the v_{VOS} known from (15), β_{FB} can be designed precisely to center or eliminate v_{Err}.

5. Overall Accuracy

5.1. Voltage Reference

The baseline accuracy of a voltage regulator is set by the accuracy of the band-gap reference circuit that supplies v_{REF}. The reference circuit suffers from its own intial accuracy, temperature coefficient, temperature drift, long-term drift, line regulation and noise [27–30]. Initial accuracy (which accounts for process variation, mismatch, and random and manufacturing tolerances) is typically reported in the range of 0.02% to 1% [31,32]. Typical temperature coefficients range between 1 ppm/°C and 100 ppm/°C across a 120 °C temperature range [33]. Long-term drift can reach up to 100 ppm/1000 h [29], temperature drift can be between 1 ppm/°C and 10 ppm/°C [34], line regulation can reach up to 25 ppm/V [35], and noise can be between 0.2 ppm and 20 ppm [32]. With these errors, v_{REF} varies by up to ±1% around its nominal value, limiting the absolute accuracy of the voltage regulator to this extent.

5.2. Line Regulation

Line regulation refers to the ability of the voltage regulator to maintain v_O at its target v_O' under varying v_{IN}. Poor line regulation adds to the overall steady-state inaccuracy. In the present work, line variations translate into the energizing duty cycle via (2) in Section 2. For instance, in a 5 V to 2.5 V non-inverting buck–boost regulator with a nominal d_E of 50%, a ±10% line variation causes a ±0.11% variation in d_E according to (2). This is plotted in Figure 36. Sections 3 and 4 discuss how variations in d_E translate to v_{VOS} and v_{Err}. Thus, v_{Err} already accounts for the steady-state error contribution of line variation.

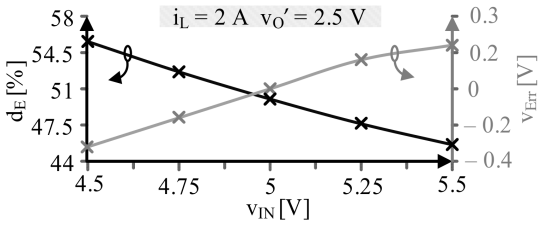

Figure 36. Effect of line variation on d_E and v_{Err}.

5.3. Load Regulation

Load regulation is the ability of the voltage regulator to maintain v_O at the target v_O' under varying load current demand. As discussed previously, in current-mode voltage loops, i_{LD} variations contribute to v_{Err} via the loading effect on d_E. For example, a ±1.5 A variation around a nominal i_{LD} of 2 A causes a 0.62% loading effect on d_E in PWM and 1.25% in hysteretic and peak current-mode voltage loops. The translation of this d_E variation to v_{VOS} and v_{Err} has been discussed in Sections 3 and 4.

In a practical switched-inductor stage, line variations also contribute to v_{Err} via ohmic losses. Figure 37 shows a non-ideal switched-inductor stage with L_X's equivalent series resistance (ESR), R_L; the total on-resistance of energizing switches, R_E; and the total on-resistance of drain switches, R_D.

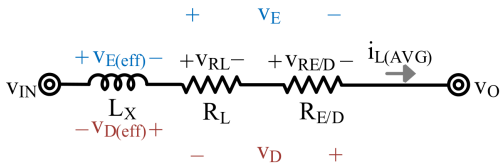

Figure 37. Switched-inductor model with ohmic losses.

R_L and R_E drop voltages v_{RL} and v_{RE} during t_E, lowering the ideal v_E to an effective $v_{E(eff)}$. Similarly, during t_D, R_L and R_D raise the ideal v_D to $v_{D(eff)}$ by adding voltages v_{RL} and v_{RD} in the opposite direction. This results in an energizing duty cycle, $d_{E(eff)}$, that varies with i_L:

$$\begin{aligned} d_{E(eff)} &= \frac{v_{D(eff)}}{v_{E(eff)}+v_{D(eff)}} \\ &= \frac{v_D+i_{L(AVG)}(R_L+R_D)}{v_E-i_{L(AVG)}(R_L+R_E)+v_D+i_{L(AVG)}(R_L+R_D)} \\ &= \frac{v_D+v_{RL}+v_{RD}}{(v_E-v_{RL}-v_{RE})+(v_D+v_{RL}+v_{RD})}. \end{aligned} \tag{23}$$

Since i_L scales with i_{LD}, the above $d_{E(eff)}$ encapsulates the loading effect of i_{LD} on d_E. Typical inductor ESRs can vary within ranges of up to a few tens of mΩ [36]. The $R_{E/D}$ of switches, when implanted using MOSFETs, range between 20 mΩ and 100 mΩ. For instance, consider a 5 V to 2.5 V non-inverting buck–boost regulator with an R_L = 30 mΩ and an $R_{E/D}$ = 50 mΩ. According to (23), the nominal $d_{E(eff)}$ is 53.2% and it varies by

±4.5% when i_{LD} varies by ±1.5 A around 2 A. Figure 38 plots this variation in $d_{E(eff)}$. The translation of $d_{E(eff)}$ into v_{Err} is already comprehended in the discussions in Sections 3 and 4 and is plotted on the secondary axis in Figure 38.

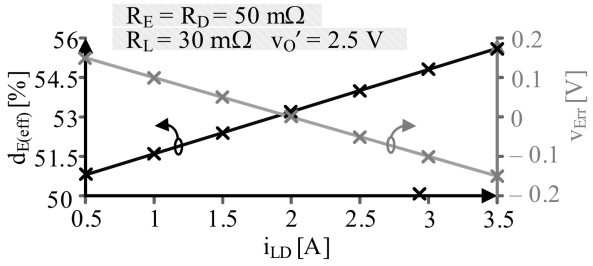

Figure 38. Effect of ohmic losses under load variation on $d_{E(eff)}$ and v_{Err}.

5.4. Process Variation and Random Tolerance

Design parameters that determine offsets suffer from statistical process variations and random tolerances, further worsening the overal steady-state accuracy. In modern CMOS processes, transistor threshold voltages vary by up to ±50–100 mV and the transcondutance parameter varies by up to ±20% across the process. On-chip resistors and capacitors show a poorer tolerance of around ±20%.

As a result, v_{IEO0}, v_{EO0}, and v_{ID0} (offsets in CP_{PWM}, CP_{HYS}, A_{IE} and A_E) vary by up to ±15 mV around the nominal value. Propagation delays ($t_{P(HI/LO)}$) and projections ($v_{P(LO/HI)}$) vary by ±30%. The sawooth generator frequency (t_{SW}), amplitude (Δv_S) and limits ($v_{S(LO/HI)}$) vary by 5%, 5% and ±5–10 mV respectively.

5.5. Temperature Drift

MOSFET threshold voltages vary by about –2 to –3 mV/°C [37], while channel resistance varies between 0.35%/°C and 0.5%/°C. Resistors show higher robustness to temperature, varying by 10 to 500 ppm/°C [38], while capacitors drift by 10 to 1000 ppm/°C depending on the implementation technology. With typical error amplifier gains between 60 and 80 dB, process variations and temperature drifts together contribute between ±1% and ±2% steady-state error in voltage regulators [38–41].

5.6. On-Chip vs. Off-Chip Feedback Implementation

The voltage feedback factor, β_{FB}, is usually a resistor divider network. On-chip implementations of the resistor divider benefit from superior resistor matching, higher thermal coupling and temperature drift, shorter test times, lower cost in terms of area, and shorter test times. However, as mentioned before, integrated resistors have loose tolerances of up to ±20%. On the other hand, off-chip implementations of resistor dividers offer the advantages of greater programmability and tighter resistor tolerances (±0.1% to ±1%). It is important to note that despite their lower contribution to overall error, off-chip implementations are less desirable because they require calibration. Calibration cycles increase test time and complexity, area, and overall cost.

5.7. Systemic Offsets

Systemic offsets discussed in this work add to the existing steady-state output error set by process variation, temperature drift, random tolerances and reference voltage stability. In the examples presented in this work, v_{OS} contributes up to an additional 2.1% variation in the steady-state output at room temperature. This v_{Err} can be lowered to 1.26% (over 40% improvement) with offset centering, to 0.63% (70% improvement) with v_{Err} centering, and to zero with offset elimination at room temperature.

It is noteworthy, however, that other sources of steady-state error remain unaffected by offset correction or elimination methods. The overall accuracy of the regulator is then limited by the ±1% to ±2% error contributed by the sources listed above. For the highest accuracy, these residual errors can be captured on-chip by designing a calibration cycle at the expense of cost and complexity. Alternatively, they can be measured and trimmed post-fabrication. Typically, trimmed voltage references exhibit errors below 0.05%. Temperature coefficients and process variations can be trimmed out up to 0.5% [42].

Table 2, below, summarizes the implementation, advantages, limitations and reduction in systemic steady-state error achieved by the offset elimination and centering techniques at room temperature and across i_L = 0.5 to 3.5 A and v_O = 1.2 V to 4.5 V.

Table 2. Summary of offset elimination and error centering strategies.

	v_{OS} Elimination	v_{OS} Centering	v_{Err} Centering
Implementation	Adjust $v_{S(LO/HI)}/\beta_{IFB}$ for each (d_E, i_L) combination	Adjust $v_{S(LO/HI)}/\beta_{IFB}$ at ($d_{E(AVG)}$, $i_{L(AVG)}$)	Adjust β_{FB} at ($d_{E(AVG)}$, $i_{L(AVG)}$)
% reduction in systemic error at room temperature	100%	PWM: 74.6% Hysteretic: 71.2% Peak/valley: 70%	PWM (basic): 60.3% PWM (current mode): 98.9% Hysteretic: 40.2% Peak/valley: 40%
Advantages	Highest achievable accuracy across (d_E, i_L) Higher ease of programming $v_O = v_C/\beta_{FB}$	Constant $v_{S(LO/HI)}/\beta_{IFB}$ Low residual v_{Err} across (d_E, i_L) Minimal impact on stability	Constant $v_{S(LO/HI)}/\beta_{IFB}$ Minimal impact on stability
Challenges	$v_{S(LO/HI)}$, $\beta_{IFB} = f(d_E, i_L)$ Requires precise and programmable sawtooth/current sensor design	Requires prior information on load conditions	Requires prior information of load conditions

Finally, Table 3 compares the present work with prior works on the steady-state accuracy of voltage regulators. This work outperforms the others owing to it having the widest scope, lowest overhead, and highest robustness. The residual post-trim accuracy can be ±0.5% when systemic offsets are completely removed at room temperature by offset elimination techniques.

Table 3. Comparison with prior works.

Metric	[23]	[17]	[24]	[20]	[This Work]
v_{IN}	4.2 V–5.5 V	NA	8 V–24 V	2.4 V–4.8 V	5 V ± 10%
v_O	3.52 V	2.5 V	5 V	−0.9 V to −5.3 V	1.2 V–4.5 V
Error Correction Strategy	Additional offset sensing control loop	Iterative error shifting using digital control	High precision current operational technique	Dynamic loop gain trimming	Aligning steady-state equilibrium with operating conditions
Scope	Constant on time	Digital Proportional–Derivative	Constant on time	Inverting buck–boost	PWM, hysteretic, peak–valley

Table 3. *Cont.*

Metric	[23]	[17]	[24]	[20]	[This Work]
Robustness	Focuses mainly on error due to i_{LD} variation (0 A–3 A)	Focuses mainly on error due to i_{LD} variation (1.25 A–3.25 A)	Quantifies offset error under both i_{LD} (0 A–2 A) & line variation	Focuses mainly on line regulation	Quantifies v_{OS} as a function of v_{IN}, v_O, i_{LD} & component parameters
Overhead	Additional VCO, OTA, 8-bit counter & CDAC	Additional MCU	Active current-mode logic	Trim bit storage registers & DAC	No additional blocks; up to 1% impact on stability
Post-Trim Residual Error	0.545 mV (0.02%)	NA	6 mV (0.12%)	0.17–0.3% (post-trimming)	±0.5% *

* Projected post-trim error stemming from v_{REF}, process and temperature variation after systemic error is completely eliminated at room temperature.

6. Conclusions

This work presents a unified and control-agnostic framework that analyzes systemic offset errors in PWM, hysteretic and peak/valley-controlled DC-DC voltage regulators. The presented framework explicitly relates current and voltage loop offsets to the regulator's duty cycle, load and line conditions, loop gain, internal propagation delays, and non-idealities in the error amplifier and comparator, providing a clear insight into the systemic mechanisms that govern the steady-state (systemic) output error, v_{Err}. SPICE simulations validate the presented expressions across various topologies.

Using the proposed framework, this work develops two low-overhead accuracy enhancement strategies, namely, offset elimination, offset centering and v_{Err} centering. Offset elimination aligns the regulator's steady-state equilibrium with its operating condition through direct adjustment of sawtooth limits (in PWM) or the current feedback factor (in current-mode voltage loops). Thus, this method completely removes the error contribution of systemic offsets to the overall accuracy at room temperature without requiring any auxiliary circuitry. Offset and v_{Err} centering reduce this contribution by up to 70% and 40% respectively. As a result, the variation in v_O due to systemic offsets can be as low as 0.63% (v_{VOS} centering) to 1.26% (v_{Err} centering), in addition to a baseline accuracy set by process, temperature, random tolerances and other factors. The proposed strategies are implemented by simple design-level modifications of existing circuit parameters that do not require additional sensing circuits, auxiliary feedback loops or calibration. Thus, there is no additional area or power overhead. Offset centering and elimination techniques do not affect the stability of the voltage loop, while the v_{Err} elimination method has little impact on the stability of the regulator. In the worst case among the presented examples, the voltage feedback factor, β_{FB}, is lowered by <1% in the implementation of v_{Err} centering, such that the DC loop gain and the unity gain bandwidth suffer a minimal reduction of <1%.

Finally, this work discusses multiple other sources of steady-state errors. With all sources included and systemic error removed using the presented techniques, the post-trim accuracy of voltage regulators across wide operating conditions is projected to be within ±0.5%. Overall, relative to the state-of-the-art, which often relies on bandwidth-limited high-gain designs or complex empirical or dynamic gain trimming to achieve highly accurate converter designs, the systematic strategies presented in this work ensure high accuracy while preserving cost, stability and performance.

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Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

A_{CP}	Comparator gain
A_{FW}	Forward gain
A_{IE}	Voltage error amplifier gain in the current loop
A_{PWM}	Input voltage to duty cycle gain in PWM control
A_{VE}	Voltage error amplifier gain in the voltage loop
β_{FB}	Feedback translation in the voltage loop
β_{IFB}	Feedback translation in the current loop
C_O	Power stage output capacitor
CP	Comparator
d_E	Energizing duty cycle ratio
Δt_P	Difference between falling and rising propagation delays
Δv_{ID}	Actual applied differential input swing
Δv_{IFB}	Ripple in the current feedback voltage
$\Delta v_{O(MAX)}$	Maximum output swing of the comparator
Δv_S	Range or amplitude of sawtooth voltage
Δv_T	Hysteresis window of the hysteretic comparator
f_{SW}	Switching frequency
i_L	Inductor current
$i_{L(AVG)}$	Average inductor current
i_{LD}	Load current
$i_{LD(AVG)}$	Average load current
i_{LI}	Flyback primary (input) side current
i_{LO}	Flyback secondary (output) side current
i_O	Output current of comparator
k_T	Transformer voltage ratio in flyback
K_O	Overdrive factor of the comparator input
L_X	Inductance
L_{XI}	Flyback primary coil inductance
L_{XO}	Flyback secondary coil inductance
P_{IN}	Input power
P_O	Output power
R_L	ESR of inductor L_X
R_E	Equivalent on-resistance of energizing switches
R_D	Equivalent on-resistance of drain switches
S_{DI}	Input drain switch
S_{DO}	Output drain switch
S_{EI}	Input energizing switch
S_{EO}	Output energizing switch
SR_{OFF}	Reset-enabled SR flip flop
SR_{ON}	Set-enabled SR flip flop
τ_{BW}	RC time constant of the bandwidth setting pole

t_D	Draining portion of the switching period
t_E	Energizing portion of the switching period
t_P	Propagation delay
$t_{P(BW)}$	Bandwidth-limited propagation delay
t_{PF}	Falling propagation delay
t_{PR}	Rising propagation delay
$t_{P(SR)}$	Slew rate-limited propagation delay
t_{SW}	Switching period
t_X	Fixed time delay in peak or valley control
v_C	Loop control voltage
v_D	Draining voltage across the inductor
$v_{DX}{}'$	Delayed component of duty cycle voltage in peak control
v_E	Energizing voltage across the inductor
$v_E{}'$	Voltage with duty cycle d_E
v_{EO}	Amplified error voltage in the voltage loop
v_{EO0}	Output offset of error amplifier in the voltage loop
v_{Err}	Steady-state output voltage error
$v_{EX}{}'$	Delayed version of duty cycle voltage in valley control
v_{FB}	Feedback voltage
v_I	Input voltage
v_{ID}	Differential input voltage
$v_{ID(MIN)}$	Minimum differential input voltage needed to swing comparator output
v_{ID0}	Input referred offset
v_{IEO}	Amplified error voltage in the current loop
v_{IEO0}	Output offset of error amplifier in the current loop
v_{IFB}	Current feedback voltage
$v_{IFB(AVG)}$	Average of current feedback voltage
v_{IN}	Input source voltage
v_{IOS}	Current loop systemic offset
v_N	Input voltage at the negative terminal
v_O	Steady-state output voltage
$v_O{}'$	Target output voltage
V_{OH}	Comparator output level high
V_{OL}	Comparator output level low
v_{OS}	General systemic offset
v_P	Input voltage at the positive terminal
$v_{P(HI)}$	Upper projection of v_{IFB}
$v_{P(LO)}$	Lower projection of v_{IFB}
v_S	Sawtooth voltage
$v_{S(LO)}$	Minimum sawtooth voltage
$v_{S(HI)}$	Maximum sawtooth voltage
v_{SWI}	Input switching node voltage
v_{SWO}	Output switching node voltage
$v_{T(HI)}$	Upper hysteretic threshold voltage
$v_{T(LO)}$	Lower hysteretic threshold voltage
v_{VOS}	Voltage loop systemic offset

Abbreviations

The following abbreviations are used in this manuscript:

LDO	Low dropout (regulator)
PWM	Pulse-width modulation
ESR	Equivalent series resistance
MCU	Micro-controller unit

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