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Sub-Harmonic Stability and Slope Compensation Boundary in Peak/Valley DC–DC Converters

Aaryan Tiwary * and Gabriel A. Rincón-Mora

School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250, USA; rincon-mora@gatech.edu

* Correspondence: atiwary30@gatech.edu

Abstract

Sub-harmonic oscillations are a key stability concern in fast-switched inductor power supplies using clocked constant-period peak/valley-current loops. Using generalized models, IC designers can predict and suppress sub-harmonic oscillations with minimal overhead. This work presents an insightful, generalized, and comprehensive time-domain analysis of sub-harmonic oscillation propagation and suppression via slope compensation in constant-period peak/valley-current control. Since it is unstated and unvalidated in the literature, an exact, easy-to-apply expression for the slope compensation boundary is derived in terms of basic circuit operating parameters, showing that it is half of the difference in the drain and energize slopes in peak mode, and half of the difference in the energize and drain slopes in valley mode, lying beyond the conventionally accepted half drain (peak) and energize (valley) slope criteria. The prior literature also does not account for the impact of parasitic resistances on the duty-cycle-based stability boundary beyond which sub-harmonic oscillations begin. We address these gaps and establish a theoretical basis for the absence of sub-harmonic oscillations in DCM. Additionally, existing approaches to slope selection ensure stability but do not target the rate of suppression. We address this by proposing a compensation slope that achieves 90% suppression of the initial imbalance within three switching periods.

Keywords: DC–DC converters; duty cycle; current loop; constant-period; constant-frequency; sub-harmonic oscillations; slope compensation; energize slope; drain slope; stability; compensation boundary; peak-current mode; valley-current mode; parasitics

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1. Fast and Accurate Power Supply Systems

Switched inductors are fundamental building blocks in modern power electronics, with applications ranging from high-gain DC–DC converters for photovoltaic applications [1] to bidirectional power converters for fuel cell-based electric vehicles [2]. Fast-switched inductor power supplies that use constant-period (constant-frequency) peak/valley control are crucial because they enable efficient regulation over a wide range of load conditions at a constant frequency. This makes them ideal for various applications such as LED drivers [3], mobile applications [4], and Power Factor Correction converters [5]. A general switched inductor power supply is depicted in Figure 1 to illustrate the overall structure and establish common terminology. These power supplies using constant-period peak/valley control are also referred to as clocked because an external clock (f_{CLK} in Figures 8, 16 and 17) determines the switching period.

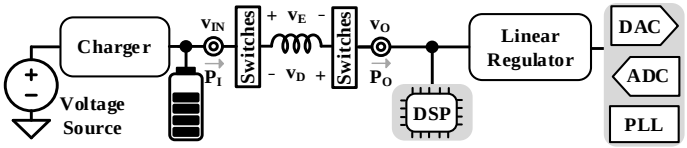

Figure 1. General switched inductor power supply.

Sub-harmonic oscillations are a critical stability concern in these systems, manifesting as cycle-to-cycle oscillations in inductor current at half the switching frequency [6] due to the propagation of small perturbations between successive switching cycles. This makes it essential to develop generalized, comprehensive, and intuitive frameworks to predict and suppress them reliably.

Past analyses have often relied on frequency-domain modeling [7–9]. Harmonic-balance-based analyses, as in [7], derive closed-form stability conditions by representing the converter as a square-wave generator with linear feedback and evaluating its behavior, but they require approximations like square-wave modeling of switching waveforms that obscure time-domain behavior and make interpretation and design application unintuitive. Sampled data analysis, as presented in [8], models converter dynamics through discrete-time transfer functions and identifies poles and zeros to assess stability. The continuous-time model in [9] incorporates sampled-data effects into a pole-zero representation that predicts sub-harmonic oscillations while accounting for the influence of the compensating ramp. These mathematical approaches abstract away waveform-level behavior, making it harder to understand oscillation propagation and intuit design guidelines for suppression.

While time-domain analyses exist [10,11], they do not offer a simple, generalized model for prediction and suppression, instead relying on rigorous approaches limited to specific topologies and control modes. The work in [10] derives relationships between control voltage, duty cycle, and inductor current through highly involved, multi-step mathematical formulations involving coupled equations, multiple variables, and geometrical and small-signal analysis, resulting in a level of analytical complexity that obscures physical insight. Though [11] is mathematically simpler, it does not generalize its results across a broader range of variants and does not clearly capture the origin of the initial deviation from the ideal inductor current waveform. Its emphasis on transistor-level design further detracts from developing broader theoretical insight.

Some popular power IC design textbooks [12–15] and research publications [11,16–21] state that the slope compensation boundary beyond which the applied slope will suppress oscillations is half of the drain slope of the inductor current in peak mode, while several other works [22–24] do not derive or explicitly state a minimum slope boundary at all despite demonstrating a reasonable understanding of sub-harmonic gain and oscillation propagation. Some other works [25,26] derive the critical condition for the compensating slope analytically to be half of the difference in the drain and energize slopes in peak mode, but then proceed to interpret the stability boundary as being half of the drain slope! No body of work in the literature states or validates the correct compensation slope boundary. This ambiguity in the exact location of the stability boundary reflects an incomplete understanding of the exact boundary location and surrounding stability region in the existing literature.

Existing works [27–29] largely neglect the impact of parasitic resistances, including inductor series resistance and/or switch on-resistances, on sub-harmonic oscillations and the associated stability boundary. This limits the applicability of existing results and design guidelines to practical converter implementations, where such parasitics are always present and can alter observed behavior.

Despite Continuous-Conduction Mode (CCM) and Discontinuous-Conduction Mode (DCM) being well-established concepts, existing works [30,31] show a notable lack of exploration of sub-harmonic oscillations in DCM, leaving an unresolved gap and little analytical rationale to either support or rule out their existence in this mode.

Constant-period valley mode control remains substantially underexplored in the existing literature compared to peak mode control, with no clear extension of established peak-mode sub-harmonic gain and stability results, slope relationships, or compensation guidelines to valley mode, leading to ambiguity in its analysis and design.

Lastly, a very commonly recommended compensating slope in the literature is half the drain slope. While this choice guarantees suppression, it does not provide a targeted measure of how much of the initial imbalance is reduced or how quickly this occurs, making it inadequate for designing rapid and controlled imbalance suppression.

To address these issues, this work develops an insightful generalized time-domain framework and determines the exact compensation boundary in terms of basic operating parameters: input/output voltages and inductance, revealing that the true limit lies beyond the traditionally accepted half-drain slope in peak mode (and half-energize slope in valley mode). The framework is further extended to account for parasitic resistances, capturing their impact on the energize duty cycle and stability boundary, and to examine the possibility of sub-harmonic oscillations in the Discontinuous-Conduction Mode. In addition, it enables a structured and predictive approach to compensation slope selection by linking slope choice to transient imbalance suppression. The validity and utility of these results are demonstrated through SPICE simulations, which illustrate both the accuracy of the derived boundary and its effectiveness as a practical design reference.

Section 2 reviews switched inductor operation in both CCM and DCM, covering ideal behavior, parasitic effects, and the fundamentals of peak-current loops. Section 3 examines sub-harmonic oscillation propagation, sub-harmonic gain, and stability conditions in the Continuous-Conduction Mode, and rigorously addresses the absence of sub-harmonic oscillations in the Discontinuous-Conduction Mode. Section 4 introduces slope compensation, derives the compensation boundary, and proposes a new structured design guideline for compensation slope selection. Section 5 extends the results to valley mode, graphically illustrates the stability boundaries, including the impact of parasitics, and validates both the derived boundary and the proposed slope compensation design guideline while demonstrating transient suppression behavior through peak-current reference step simulations. Section 6 concludes the paper.

2. Switched Inductors

2.1. General Operation in Continuous-Conduction Mode

As shown in Figure 1, inductors magnetize/demagnetize when an energize/drain voltage $v_E/-v_D$ is applied across them for time t_E/t_D, thereby storing and releasing energy. In the absence of parasitics, v_E and v_D equal the externally applied energize and drain voltages v_E' and v_D', respectively. Given an ideal inductor L_X, the magnitude of energize slope [32] s_E and drain slope s_D of the inductor current during energize/drain time $t_{E/D}$ is given by:

$$s_{E/D} = \frac{di_L}{dt_{E/D}} = \frac{v_{E/D}}{L_X}. \quad (1)$$

Energizing and draining L_X in the Continuous-Conduction Mode (CCM) across the switching period t_{SW} produces the triangular current ripple shown in Figure 2.

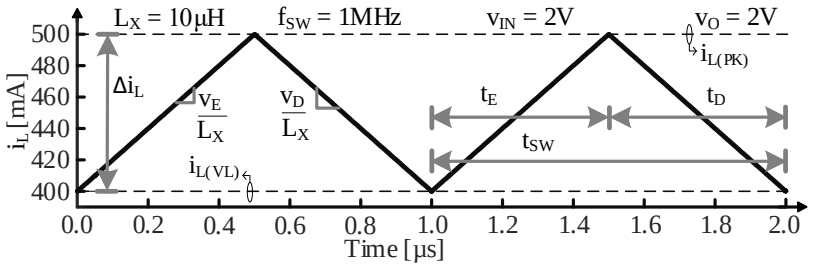

Figure 2. Simulated constant-period peak/valley control buck–boost inductor current in CCM.

The energize (d_E) and drain (d_D) duty cycles are the switching period fractions in which the inductor is energized and drained, respectively. For an ideal inductor draining and energizing through ideal switches, they are expressed as:

$$d_{E/D} = \frac{t_{E/D}}{t_{SW}} = \frac{v_{D/E}}{v_E + v_D}. \quad (2)$$

As t_E and t_D add up to t_{SW}, the sum of d_E and d_D is 1.

2.2. General Operation in Discontinuous-Conduction Mode

Our discussion so far has focused on the Continuous-Conduction Mode of operation. In the Discontinuous-Conduction Mode (DCM), L_X energizes and depletes before t_{SW} ends. As shown in Figure 3, i_L climbs across t_E to peak inductor current, falls across t_D to zero, and remains at zero until another cycle begins. The duration of time comprising t_E and t_D, during which inductor current is non-zero, is referred to as the conduction time t_C. The interval of zero inductor current t_{DCM} between consecutive t_Cs is the discontinuity in conduction that characterizes DCM. Because discontinuous conduction by definition requires an interval of zero current before the next switching cycle begins, the inductor current at the end of a switching cycle in DCM is zero, given by:

$$i_L|_{t=t_{SW}} = 0 \quad (3)$$

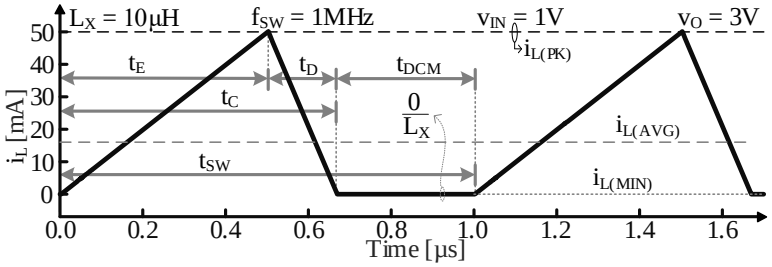

Figure 3. Simulated constant-period peak control buck–boost inductor current in DCM.

2.3. Variants

Switched-inductor variants include buck–boost, buck, boost, inverting, and flyback, as shown in Figure 4. The input v_{IN} is usually a voltage source. S_{EI}, S_{DG}, S_{EG}, and S_{DO} are the input energize switch, ground drain switch, ground energize switch, and output drain switch, respectively. The buck–boost alternates the inductor between input-ground and output-ground to energize/drain. In the buck, one end is always connected to the output while the other end toggles between the supply voltage while energizing and ground while draining.

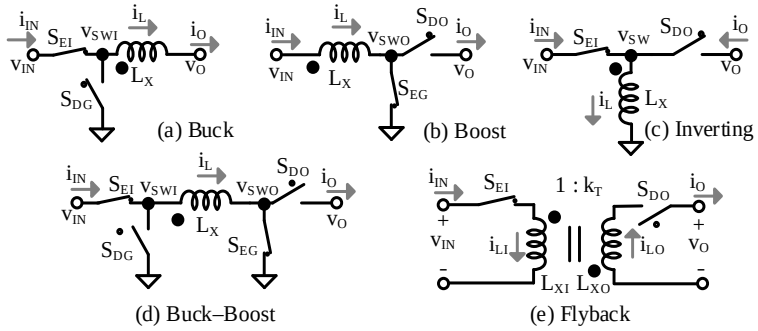

Figure 4. Converter topologies.

The inverting buck–boost is unique in having a negative output voltage wherein one terminal is always grounded and the other switches between input while energizing and output when draining. In the flyback, v_{IN} magnetizes the core of an inductor L_{XI} when energizing, while v_O demagnetizes the core of a coupled inductor L_{XO} while draining. k_T is defined as the ratio of the voltage induced across L_{XO} to the voltage applied across L_{XI}. The energize and drain voltages of these topologies, assuming ideal switches and inductors, are listed in Table 1. All results derived in subsequent sections can be applied to any of these topologies.

Table 1. Energize/drain voltages of ideal variants.

Variant	$v_E{}'$	$v_D{}'$	d_E
Buck	$v_{IN} - v_O$	v_O	$\frac{v_O}{v_{IN}}$
Boost	v_{IN}	$v_O - v_{IN}$	$\frac{v_O - v_{IN}}{v_O}$
Inverting	v_{IN}	$-v_O$	$\frac{-v_O}{v_{IN} - v_O}$
Buck–Boost	v_{IN}	v_O	$\frac{v_O}{v_{IN} + v_O}$
Flyback	v_{IN}	v_O/k_T	$\frac{v_O}{v_{IN}k_T + v_O}$

2.4. Effects of Parasitic Resistances

Our analysis thus far has focused on ideal converters, assuming zero parasitic resistance in the inductor and ideal switches with no conduction resistance. This raises the question of how the presence of these resistances in a practical circuit impacts $v_{E/D}$ and $d_{E/D}$. To investigate this, we assign resistances of R_L, R_{EI}, R_{DG}, R_{EG}, and R_{DO} to the inductor's series parasitic resistance and the input energize, ground drain, ground energize, and output drain switches, respectively. To simplify the analysis, the switch resistances of the energizing (R_E) and draining paths (R_D) are grouped together, as they collectively constitute the total switch resistance in series with the inductor during the energizing and draining phases. Therefore, we have the following:

$$R_{E/D} = R_{EI/DO} + R_{EG/DG}. \tag{4}$$

R_L and energize resistances R_E drop voltages v_{RL} and v_{RE} that decrease v_E below its ideal level $v_E{}'$, as shown in Figure 5. Similarly, since i_L flows to v_O when L_X drains, R_L and drain resistances R_D drop voltages v_{RL} and v_{RD} that increase v_D over its ideal level $v_D{}'$. The average ohmic drop across these resistances depends on the average inductor current $i_{L(AVG)}$. The energize and drain voltages are now given by:

$$v_E = v_E{}' - v_{RL} - v_{RE} = v_E{}' - i_{L(AVG)}(R_L + R_E) \tag{5}$$

$$v_D = v_D{}' + v_{RL} + v_{RD} = v_D{}' + i_{L(AVG)}(R_L + R_D). \quad (6)$$

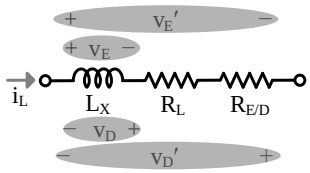

Figure 5. Energize and drain voltages modified due to parasitic resistances.

Reducing v_E extends the t_E that L_X needs to energize across Δi_L in Figure 2, and raising v_D reduces the t_D that L_X needs to drain. This rise in t_E and fall in t_D increases d_E above its ideal value $d_E{}'$ to the extent that i_L, R_L, R_E, and R_D dictate, given by:

$$d_E = \frac{v_D}{v_E + v_D} = \frac{v_D{}' + i_{L(AVG)}(R_L + R_D)}{\left(v_E{}' - i_{L(AVG)}(R_L + R_E)\right) + \left(v_D{}' + i_{L(AVG)}(R_L + R_D)\right)} = \frac{v_D{}' + i_{L(AVG)}(R_L + R_D)}{\left(v_E{}' - i_{L(AVG)}R_E\right) + \left(v_D{}' + i_{L(AVG)}R_D\right)}$$

$$\approx \frac{v_D{}' + i_{L(AVG)}(R_L + R_D)}{v_E{}' + v_D{}'}. \quad (7)$$

On average, R_L subtracts from $v_E{}'$ the same v_{RL} that R_L adds to $v_D{}'$. Similarly, R_E and R_D subtract from $v_E{}'$ and add to $v_D{}'$ similar voltages when R_E and R_D are similar, which is not unlikely (hence the approximation in (7)). But since d_E is a v_D fraction of v_E and v_D, v_{RL} and v_{RD} in v_D invariably raise d_E over its ideal counterpart $d_E{}'$. Figure 6 illustrates the increase in d_E in the presence of parasitics relative to the ideal case $d_E{}'$, where R_L, R_{EI}, R_{EG}, R_{DG}, and R_{DO} in a buck–boost are each set to 200 mΩ and $i_{L(AVG)}$ is approximately 450 mA, representing a typical operating point in many practical converters.

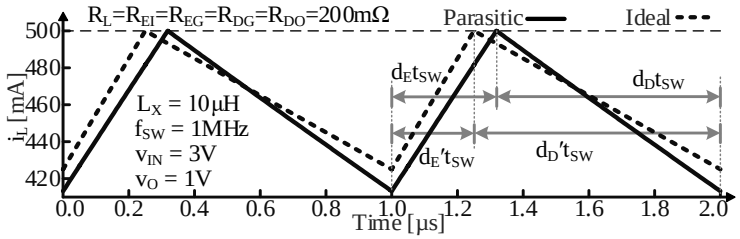

Figure 6. Simulated constant-period peak mode buck–boost inductor current with and without parasitics.

To assess the broader impact, simulations are also performed over parasitic resistances (R_L, R_{EI}, R_{EG}, R_{DG}, and R_{DO}), each ranging from 100 mΩ to 500 mΩ, and $i_{L(AVG)}$ from 400 mA to 1 A, which span typical variations in device on-resistance and load current across practical designs. Since the deviation of d_E from $d_E{}'$ increases monotonically with both resistance and current, evaluating the four corner cases (100 mΩ with 400 mA, 100 mΩ with 1 A, 500 mΩ with 400 mA, and 500 mΩ with 1 A) effectively bounds the full range of behavior, with intermediate values falling within these limits. The simulation results closely match the theoretical predictions from (6). Specifically, d_E increases from 0.25 in the ideal case ($d_E{}'$) to 0.28 (theoretical) and 0.281 (simulated), corresponding to a 12% increase, for the 100 mΩ and 400 mA case; to 0.325 (theoretical) and 0.323 (simulated), corresponding to a 30% increase, for the 100 mΩ and 1 A case; to 0.4 (theoretical) and 0.385 (simulated), corresponding to a 60% increase, for the 500 mΩ and 400 mA case; and to 0.625 (theoretical) and 0.624 (simulated), corresponding to a 150% increase, for the 500 mΩ and 1 A case.

Practical parasitic resistances, such as those used in the simulation in Figure 6, are typically small and do not produce visually significant changes in the energize and drain slopes of the inductor current. To illustrate this effect, the simulation is repeated with

uncharacteristically large parasitic resistances of 1 Ω each, resulting in a waveform with clearly visually discernible changes in the energize and drain slopes, as shown in Figure 7.

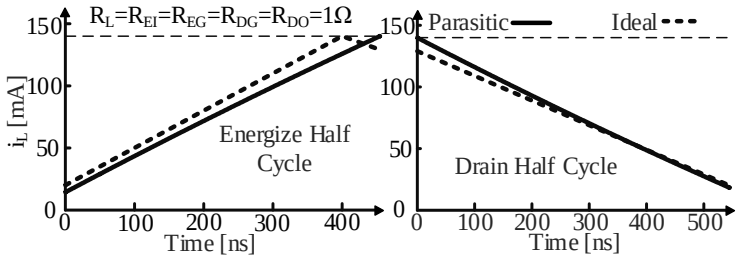

Figure 7. Simulated constant-period peak mode buck–boost inductor current with impractically high parasitic resistances, showing pronounced differences in energize and drain slopes.

2.5. Peak-Current Control

Switched inductor power supplies normally close feedback loops that sense the output, amplify the error, and adjust inductor current to minimize error. This enables them to supply any current the load requires. In clocked constant-period peak-current loops, switching events occur at fixed clock intervals, and inductor current regulation is achieved by comparing it to a reference that acts as its peak. For a current reference voltage v_C (set by an external circuit/outer loop), forward gain $A_{FW(PK)}$ and feedback gain $\beta_{FB(PK)}$, the peak reference $i_{L(PK)}$ is given by:

$$i_{L(PK)} = v_C \left(\frac{A_{FW(PK)}}{1 + A_{FW(PK)} \beta_{F\beta(PK)}} \right) \approx \frac{v_C}{\beta_{F\beta(PK)}}. \quad (8)$$

The fixed switching period t_{SW}/t_{CLK} is dictated by an external clock f_{CLK}. Constant-period loops are especially important for their fast response. The peak-current loop in Figure 8 works as follows: CP_{PK} starts t_D (and ends t_E) when v_{IFB} overcomes v_C (v_{IFB} rises in t_E), after which v_{IFB} falls until f_{CLK} ends t_D and starts another t_E. It uses a reset dominant SR latch. Figure 2 shows the inductor current in a constant-period peak-current loop across two switching cycles, where the feedback loop regulates $i_{L(PK)}$. While the exact value of the peak-current reference $i_{L(PK)}$ depends on the application, a value of 500 mA is chosen for the simulation in Figure 2, enabling a typical average inductor current of about 450 mA, representative of many practical applications. The $i_{L(VL)}$ reference is for valley control, which will be discussed later. Inductor current waveforms match in the two control schemes.

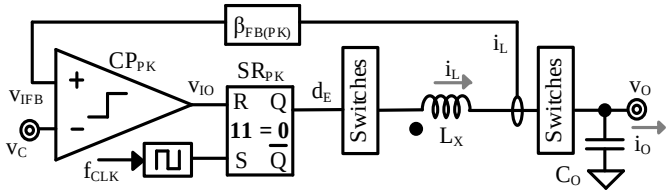

Figure 8. Constant-period peak-current loop.

3. Sub-Harmonic Oscillations

3.1. Sub-Harmonic Instability in CCM

Noise in v_{IN} or v_O can change the energize/drain slope of inductor current, thus altering $t_{E/D}$. A temporary rise in v_{IN}, for example, raises the energize slope in Figure 9. So i_L peaks sooner, falls for a longer t_D, and ends the cycle below its normal minimum.

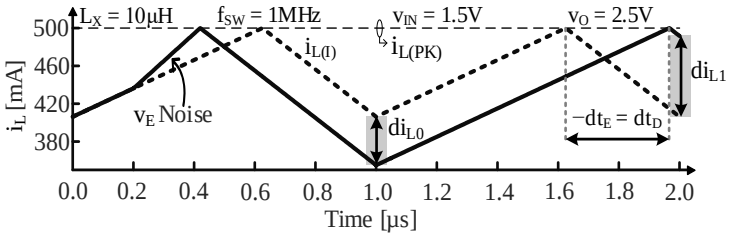

Figure 9. Simulated sub-harmonic oscillation propagation in a buck–boost.

The initial deviation di_{L0} from the ideal unperturbed inductor current $i_{L(I)}$ causes a dt_E increase in t_E in the next cycle because the increase in current needed to get to the peak is higher. This decreases t_D by dt_D because t_{SW} is constant. So i_L is above its normal value at the end of this cycle. This imbalance inverts every cycle, so the frequency of these oscillations is $f_{sw}/2$.

3.2. Sub-Harmonic Gain in CCM

The new imbalance di_{L1} is a drain slope projection of dt_D, which is the inverse (negative) of di_{L0}'s reverse energize slope projection dt_E, and therefore, we have:

$$di_{L1} = dt_D\left(\frac{di_L}{dt_D}\right) = di_{L0}\left(\frac{dt_E}{di_L}\right)\left(\frac{dt_D}{dt_E}\right)\left(\frac{di_L}{dt_D}\right) = di_{L0}\left(\frac{L_X}{v_E}\right)(-1)\left(\frac{v_D}{L_X}\right) = -di_{L0}\left(\frac{d_E}{1-d_E}\right). \quad (9)$$

The ratio of the final to the initial imbalance is the sub-harmonic gain A_{SH}. It is expressed as:

$$A_{SH} \equiv \frac{di_{L1}}{di_{L0}} = -\left(\frac{d_E}{1-d_E}\right). \quad (10)$$

3.3. Stability States in CCM

As shown in Figure 10, oscillations shrink, repeat, and grow when the magnitude of A_{SH} is less than, equal to, and greater than 1, respectively. The system is stable when oscillations shrink and is unstable otherwise. So, peak loops are unstable when d_E is 0.5 or greater. For the simulations in Figure 10, the input and output voltages are selected to yield duty cycles below, equal to, and above 0.5.

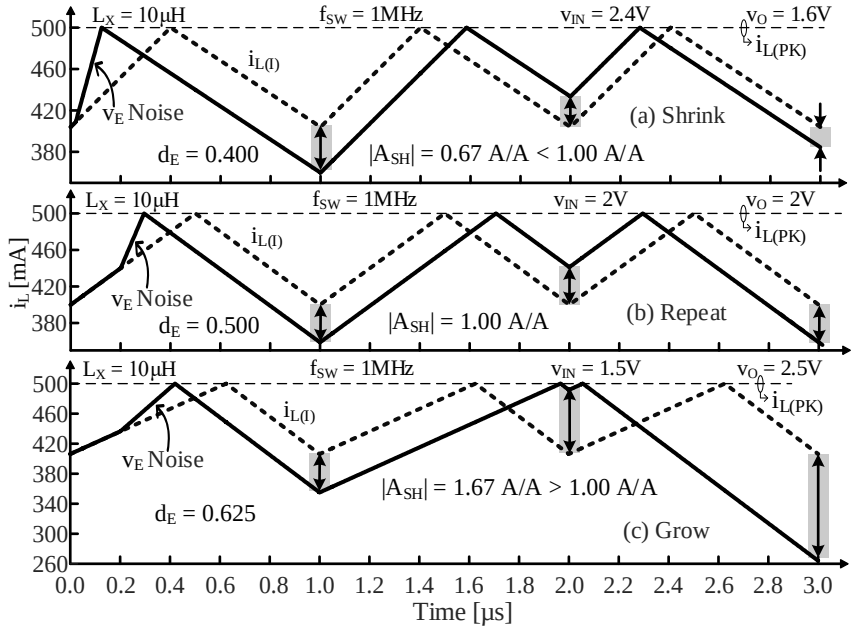

Figure 10. Oscillations shrink, repeat, and grow in a buck–boost.

3.4. Sub-Harmonic Instability in DCM

Sub-harmonic oscillations in CCM arise from cycle-to-cycle imbalances between the ideal (noiseless) inductor current trajectory $i_{L(I)}$ and perturbations induced by v_{IN}/v_O noise. These imbalances persist at the end of each switching cycle except in the special case where sub-harmonic gain is zero. They can either grow, shrink, or remain constant depending on the energize and drain slopes.

This behavior contrasts sharply with DCM. In DCM, the inductor current is forced to return to zero every cycle, effectively resetting the system and eliminating any residual 'memory' of prior perturbations. Because DCM forces both the perturbed and ideal unperturbed current to return to zero at the end of each switching cycle (from (3)), the imbalance di_{L1} between the perturbed inductor current and the ideal unperturbed current at the end of the switching cycle after the initial perturbation di_{L0} is zero. Mathematically, for a perturbation during the energize phase of the inductor, the sub-harmonic gain A_{SH} in DCM is given by:

$$A_{SH} \equiv \frac{di_{L1}}{di_{L0}} = \left(\frac{dt_E}{di_L}\right)\left(\frac{dt_C}{dt_E}\right)\left(\frac{dt_{DCM}}{dt_C}\right)\left(\frac{di_L}{dt_{DCM}}\right) = \left(\frac{L_X}{v_E}\right)(1)(-1)(0) = 0. \quad (11)$$

This can easily be extended to a perturbation in the drain phase. This implies that the imbalance between the perturbed and ideal unperturbed currents at the end the switching cycle in DCM is zero. As the sub-harmonic gain A_{SH} is zero, sub-harmonic oscillations do not occur in DCM. Figure 11 illustrates how a current perturbation in one switching cycle has no influence on the subsequent switching cycle. In Figure 11, time intervals corresponding to the ideal case are denoted with a prime (e.g., t_E'), whereas those under perturbed current conditions are represented without the prime (e.g., t_E). Unlike in CCM, the value of the peak-current reference $i_{L(PK)}$ needs to be much lower in DCM in order to be able to force the inductor current to zero every cycle. For our simulation, we choose 50 mA as $i_{L(PK)}$ because the current ripple Δi_L is typically bigger than that.

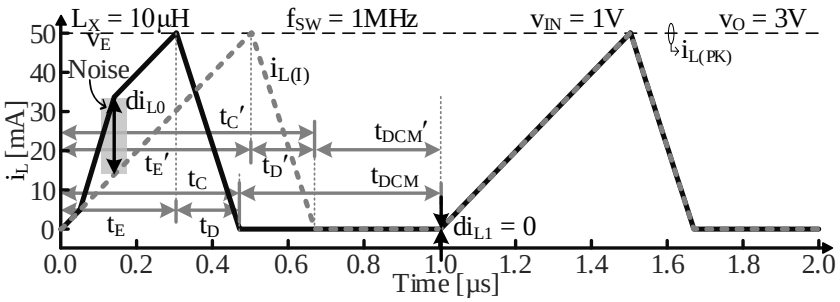

Figure 11. Simulated constant-period peak-current buck–boost in DCM; perturbation does not cause oscillations.

4. Slope Compensation

4.1. Full Slope

In peak mode, sloping the peak reference so that it falls at the same rate as the drain slope suppresses oscillations. Noise in v_E projects i_L to a v_C'/β_{FB} that aligns and redirects it back to its normal falling trajectory, as shown in Figure 12. Noise across t_D projects an imbalance di_{L0} that is rectified similarly.

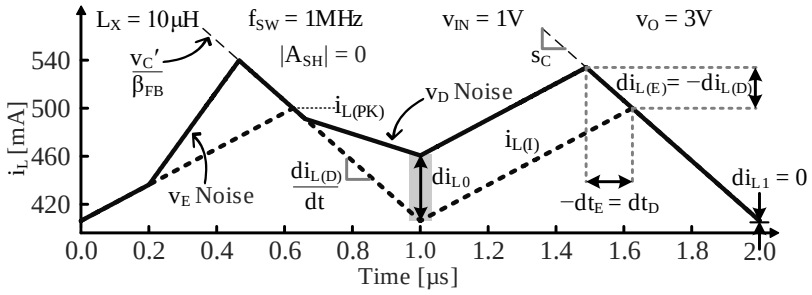

Figure 12. Simulated full-slope compensation in a buck–boost.

This use of a slope with magnitude s_C to suppress sub-harmonic oscillations is called slope compensation. Here, we use a slope equal to the drain slope, given by:

$$s_C = \frac{di_L}{dt_D} = \frac{v_D}{L_X} = s_D. \tag{12}$$

s_C set to drain slope is also called full slope because it corrects i_L within one cycle, representing the fastest possible correction.

4.2. Partial Slope

Lesser slopes may be used for more relaxed suppression requirements. The mechanism remains the same, except that i_L is steered closer, but not fully back to its normal falling path. The simulation in Figure 13 uses a compensation slope arbitrarily set to 40% of the drain slope to illustrate this relaxed suppression behavior. Because t_{SW} is constant, the dt_E increase caused by the noise is equal to $-dt_D$. As shown in Figure 13, s_C generates an imbalance $di_{L(E)}$ in time dt_E. Another imbalance arises from the change in drain time $-dt_D$ of the noisy current relative to the noiseless case. These two opposing imbalances add up to give the total deviation di_{L1} at the end of the cycle, expressed as:

$$di_{L1} = di_{L(E)} + di_{L(D)} = dt_E s_C + dt_D\left(\frac{di_L}{dt_D}\right) = dt_E\left(s_C - \frac{di_L}{dt_D}\right). \tag{13}$$

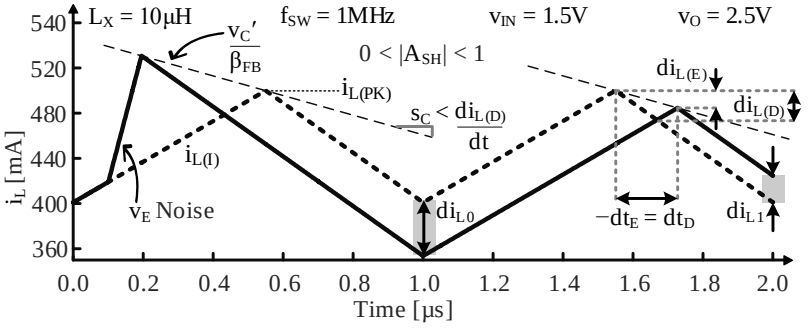

Figure 13. Simulated partial-slope compensation in a buck–boost.

dt_E is the difference in energize times for the perturbed and unperturbed currents and the inverse (negative) of the difference dt_D in their drain times because t_{SW} is constant. The rate at which the inductor current converges with the sloped reference is the sum of the energize (s_E) and compensation slopes (s_C), and therefore, it is:

$$dt_E = \frac{di_{L0}}{s_C + \frac{v_E}{L_X}}. \tag{14}$$

From (13) and (14), we get:

$$A_{SH} = \frac{s_C - \frac{di_L}{dt_D}}{s_C + \frac{v_E}{L_X}} = \frac{s_C - \frac{v_D}{L_X}}{s_C + \frac{v_E}{L_X}}. \tag{15}$$

To suppress sub-harmonic oscillations, we have:

$$|A_{SH}| < 1. \tag{16}$$

Simplifying further, we get:

$$s_C > s_{C(O)} = \frac{1}{2}\left(\frac{di_L}{dt_D} - \frac{di_L}{dt_E}\right) = \frac{1}{2}\left(\frac{v_D - v_E}{L_X}\right). \tag{17}$$

Thus, the compensation slope boundary in peak control is given by half of the difference between the drain and energize slopes. As shown in Figure 14, $|A_{SH}|$ is 1 when the compensation slope is set to this value. So, we call it the oscillating slope $s_{C(O)}$.

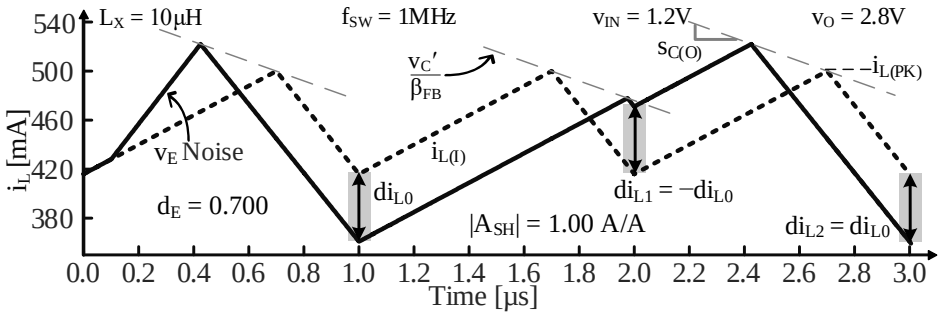

Figure 14. Simulated oscillating slope compensation in a buck–boost: repeating oscillations.

A commonly recommended compensating slope in the literature is half the drain slope [11,21,32]. This choice is always greater than the compensation slope boundary derived in (17) and therefore guarantees suppression. However, it does not provide a targeted measure of how much of the initial imbalance is suppressed and at what rate. This motivates the need for a more predictive and structured design approach.

In a power converter circuit, the objective is to suppress most of the imbalance within a short duration, ideally almost instantaneously, while avoiding unnecessarily aggressive correction. Here, 'most' and 'short duration' may be reasonably approximated as 90% suppression of the initial imbalance within three switching cycles, as this captures a rapid and practical settling behavior without imposing overly aggressive correction.

This requires a compensation slope s_{C3} that yields a sub-harmonic gain such that the imbalance reduces to one-tenth of its initial value within three switching cycles. The total sub-harmonic gain over three switching cycles is given by the cube of A_{SH}. Setting this equal to negative one-tenth (the imbalance inverts every cycle, so the sub-harmonic gain over an odd number of cycles will be negative) and plugging in the expression for A_{SH} from (15) yields:

$$s_{C3} = \frac{s_D - 0.1^{(\frac{1}{3})} s_E}{1 + 0.1^{(\frac{1}{3})}} \approx \frac{2s_D - s_E}{3}. \tag{18}$$

As shown in Figure 15, applying a compensating slope equal to s_{C3} suppresses 90% of the initial imbalance di_{L0} by the end of the third switching cycle.

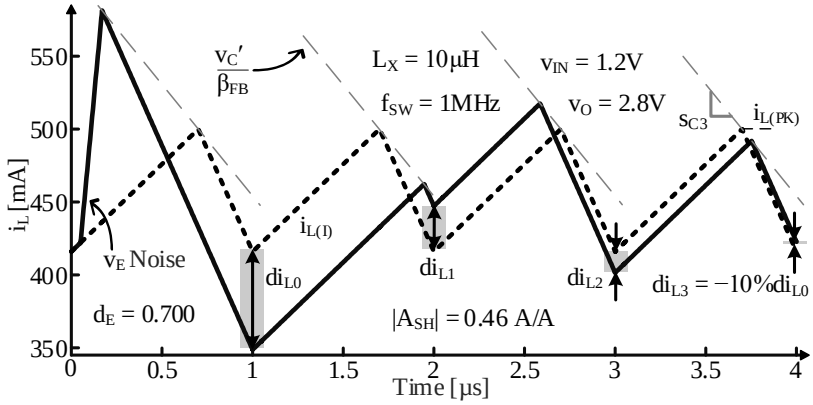

Figure 15. Simulated proposed slope compensation in a buck–boost: 90% imbalance reduction within three switching cycles.

4.3. Sloped Control Loop Implementation

This sloped peak is obtained by adding a falling ramp sawtooth waveform v_S to v_C, as shown in the slope-compensated peak-current loop in Figure 16. v_S is sloped at the desired compensation slope s_C.

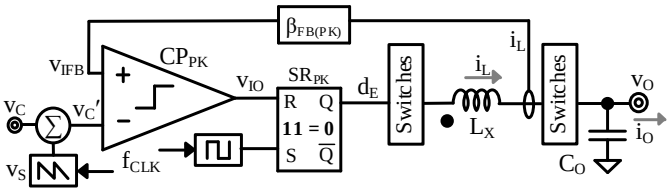

Figure 16. Constant-period slope-compensated peak-current loop.

5. Characterization

5.1. Valley-Current Control

The valley loop in Figure 17 is the complement of the peak loop. CP_{VL} starts t_E when v_{IFB} falls below v_C' (v_{IFB} falls in t_D), after which v_{IFB} rises until f_{CLK} ends t_E and starts another t_D. Therefore, v_C' sets $v_{IFB(LO)}$ and f_{CLK} fixes t_{SW}. It uses a set of dominant SR latches. Figure 2 shows the inductor current in a constant-period valley-current loop over two switching cycles. DCM is not feasible in the valley loop, as enforcing zero inductor current each cycle eliminates the ability to control the valley. The feedback loop regulates valley reference $i_{L(VL)}$, given by:

$$i_{L(VL)} = v_C \left(\frac{A_{FW(VL)}}{1 + A_{FW(VL)} \beta_{F\beta(VL)}} \right) \approx \frac{v_C}{\beta_{F\beta(VL)}}. \tag{19}$$

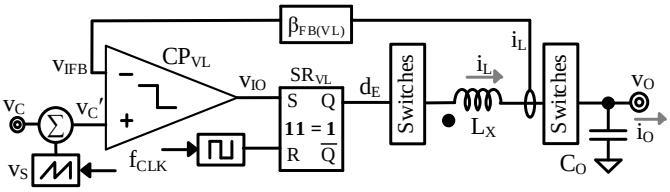

Figure 17. Constant-period slope-compensated valley-current loop.

Following the same process as in peak control, A_{SH} in valley control without compensation is derived to be:

$$A_{SH} \equiv \frac{di_{L1}}{di_{L0}} = -\left(\frac{1 - d_E}{d_E} \right). \tag{20}$$

(20) indicates that, unlike peak, sub-harmonic oscillations are a problem in valley mode when d_E is 0.5 or less. The expression for A_{SH} with slope compensation in valley control is:

$$A_{SH} = \frac{s_C - \frac{v_E}{L_X}}{s_C + \frac{v_D}{L_X}}. \quad (21)$$

So, the compensation slope boundary expression is reversed in valley control, given by:

$$s_C > s_{C(O)} = \frac{1}{2}\left(\frac{di_L}{dt_E} - \frac{di_L}{dt_D}\right) = \frac{1}{2}\left(\frac{v_E - v_D}{L_X}\right). \quad (22)$$

5.2. Stability Regions

Figure 18 shows theoretical (solid and broken lines for peak and valley mode respectively) and simulated (crosses) $|A_{SH}|$ over a range of duty cycles without compensation. The system is unstable ($|A_{SH}|$ is greater than one) when $d_E \geq 0.5$ in peak and $d_E \leq 0.5$ in valley mode. For this simulation, a buck–boost converter is used, and the input and output voltages are systematically varied to realize the desired energize duty cycle d_E.

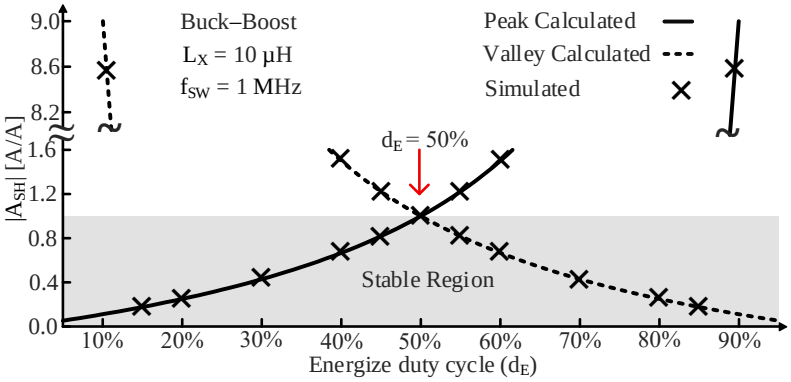

Figure 18. Calculated and simulated $|A_{SH}|$ without slope compensation.

Figure 19 shows $|A_{SH}|$ when a compensating slope 10% higher than the oscillating slope is applied in the unstable duty cycle ranges. A slope 10% higher than the compensation slope boundary is chosen as a small margin above the boundary that reduces the sub-harmonic gain below unity while remaining close to the stability boundary, thereby enabling visualization of a system operating just within the stable region. Theoretically, any compensating slope infinitesimally above the stability boundary is sufficient to ensure stability. Unlike in Figure 18, $|A_{SH}|$ always stays below one, indicating successful suppression of oscillations. Applying the proposed compensation slope of s_{C3} results in a constant sub-harmonic gain of about 0.46 (shown by the gray dotted trace), as expected, the cube of which is 10% or 0.1, meaning 90% suppression over three cycles. Figure 19 also uses a buck–boost converter with systematically varying input and output voltage to realize the desired d_E.

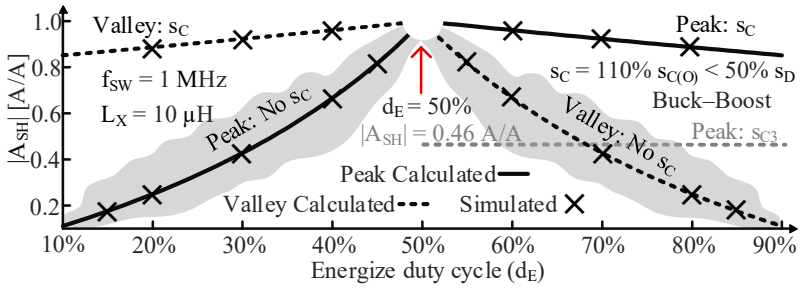

Figure 19. Calculated and simulated $|A_{SH}|$ with slope compensation.

Figure 20 shows how the oscillating slope changes with d_E for fixed values of v_E/v_D in peak/valley mode. For each trace in peak mode with a fixed v_E and in valley mode with a fixed v_D, v_D and v_E are varied to realize the desired d_E, respectively.

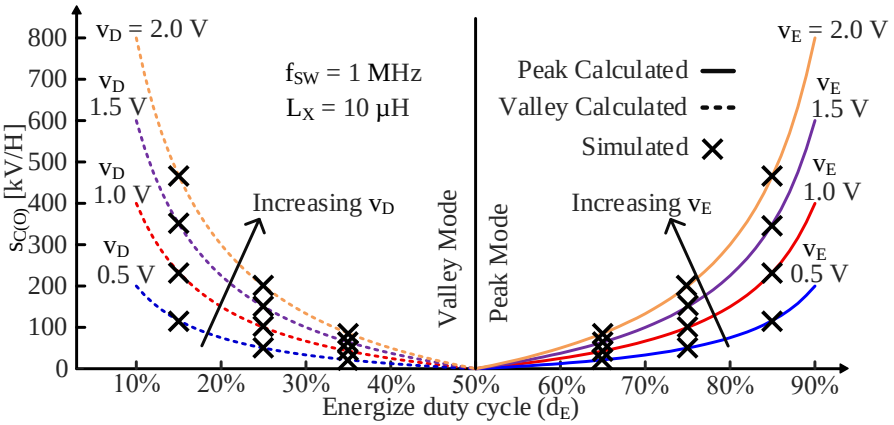

Figure 20. Calculated and simulated buck–boost oscillating slope.

As discussed in Section 2.3, parasitic resistances increase the energize duty cycle d_E relative to its ideal value d_E'. Consequently, an uncompensated system with parasitic resistances crosses the sub-harmonic gain of unity, and thus becomes unstable, at an ideal energize duty cycle d_E', computed from the ideal energize and drain voltages, that is below the 50% threshold. This effectively means that the stability boundary predicted by an energize duty cycle of 0.5 in the absence of parasitics has shifted. This behavior is illustrated in Figure 21 for a representative operating condition with an average inductor current of 1 A and parasitic resistances of 200 mΩ. This plot is obtained by holding v_D constant and varying v_E to realize the desired duty cycle d_E.

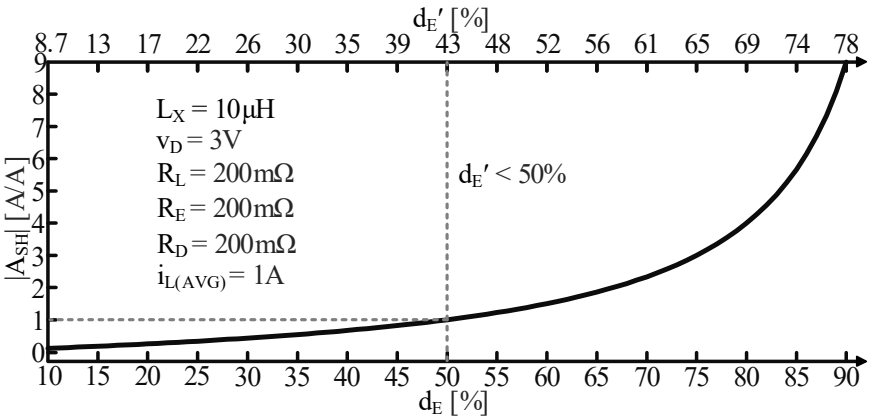

Figure 21. Variation in d_E' and $|A_{SH}|$ with d_E for an uncompensated buck–boost power stage with parasitic resistances.

Figures 22 and 23 show (crosses represent simulated datapoints) the extended slope compensation region that maintains stability beyond the limits of the traditional half-drain slope rule in peak mode and half-energize slope in valley mode, respectively. The regions on the plots marked 'also stable' illustrate the additional regions of stable operation beyond what is already unanimously accepted in the literature (the 'stable region' parts). For these results, a buck–boost converter is used, with the input and output voltages systematically varied to realize the desired energize duty cycle d_E, while the compensating slope is independently adjusted to study its effect on sub-harmonic gain. f_{SW} is 1 MHz for both.

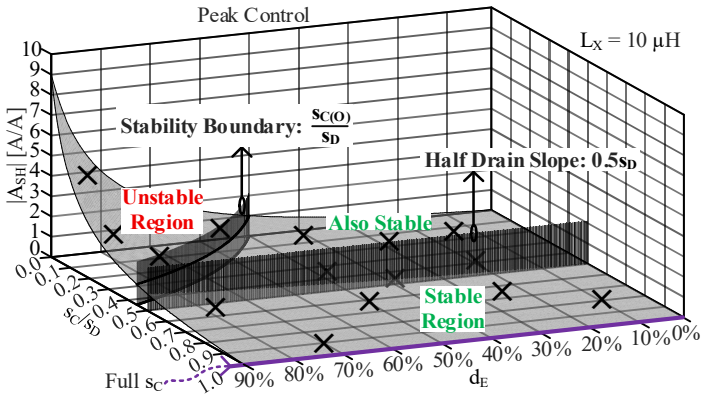

Figure 22. Calculated and simulated peak mode buck–boost's $|A_{SH}|$ with slope compensation.

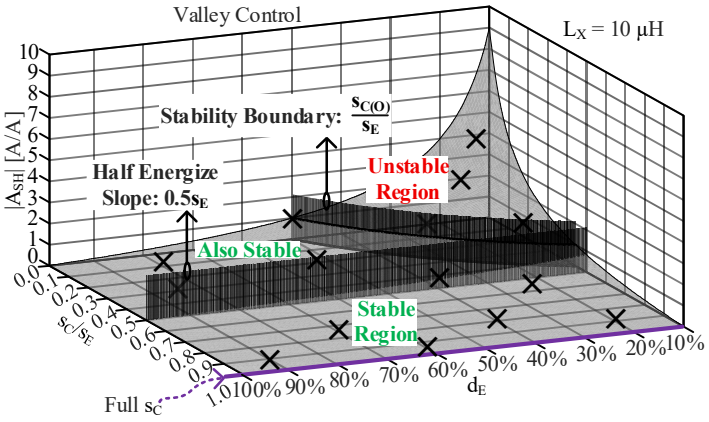

Figure 23. Calculated and simulated valley mode buck–boost's $|A_{SH}|$ with slope compensation.

To get a sense for how the compensation slope boundary, the half-drain slope criterion widespread in the literature, and the proposed slope s_{C3} with its targeted suppression compare to each other, we plot these over a range of duty cycles for a system with the parameters specified in Figure 24. The energize voltage is held constant while the drain voltage is varied to realize the desired d_E. The simulated compensation slope required to suppress 90% of the initial imbalance within three cycles closely matches the value predicted by (18).

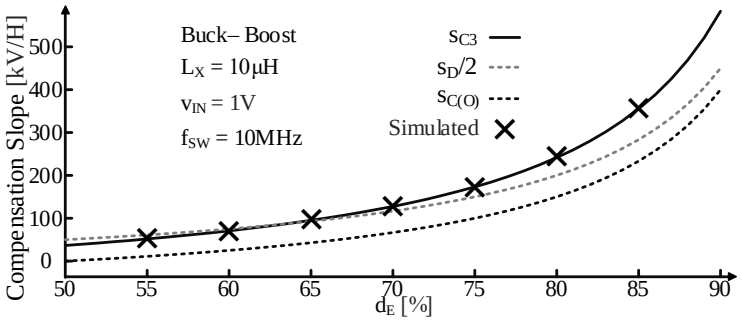

Figure 24. Variation in simulated and theoretical s_{C3}, $s_{C(O)}$ and $s_D/2$ with d_E.

Having established s_{C3} as an effective compensating slope for suppressing most (90%) of the imbalance within three switching cycles, it is instructive to compare its performance against other slope choices on this metric. To quantify the degree of immediate suppression over three switching cycles, Figure 25 presents both calculated and simulated percentages of imbalance suppression in three switching cycles for compensating slopes expressed as multiples of $s_{C(O)}$. Although the exact percentage of imbalance suppressed depends

on the circuit parameters (this plot is for the circuit parameters specified in Figure 25), the incremental improvement from increasing the compensation slope monotonically diminishes as the level of compensation rises. This simulation is based on a buck–boost converter operating at a duty cycle of 55%, realized using energize and drain voltages of 1.8 V and 2.2 V, respectively, chosen to represent a typical operating condition.

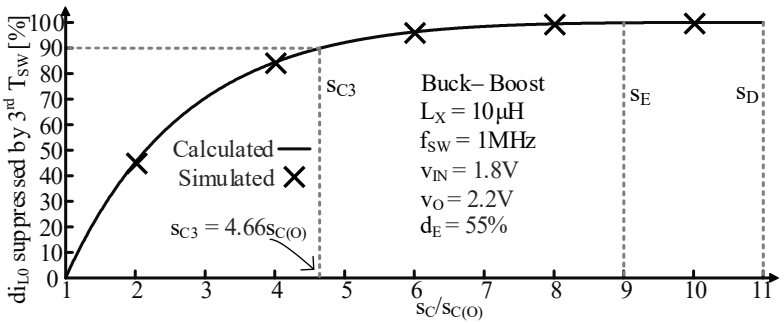

Figure 25. Calculated and simulated percentage of initial imbalance suppressed in three switching cycles over a range of compensation slopes in a constant-period peak-current buck–boost.

5.3. Control Input Step Response

In a real circuit, the current reference v_C is a regulated quantity itself. Dynamic loads at the output can often cause changes in v_C. Thus, it is useful to think about the impact of a sudden change in v_C on inductor current. To study this, we simulate a constant-period peak-current mode non-inverting buck–boost power supply with circuit parameters specified in Figure 26.

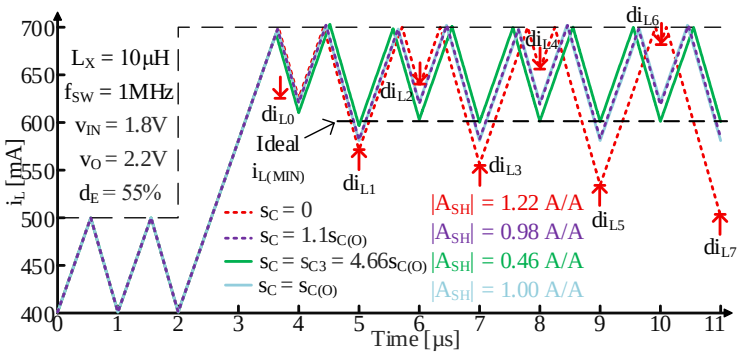

Figure 26. Simulated peak reference step in a buck–boost with various compensation slopes.

Stepping up v_C suddenly causes sub-harmonic oscillations to break out in the absence of any compensation, as shown by the dotted red trace. For this simulation, a peak-current reference step of about 200 mA, or 40% of the original peak, representative of many practical applications, is chosen. Applying a compensating slope equal to the oscillating slope $s_{C(O)}$ will lead to repeating oscillations, as shown by the solid blue trace.

Therefore, a larger slope is needed for suppression, which naturally raises the question: how much larger must it be? A 10% increase is chosen as a small increment above the oscillatory slope $s_{C(O)}$, sufficient to reduce the sub-harmonic gain below unity while remaining close to the stability boundary, thereby allowing the effect of minimal overcompensation on the rate of imbalance suppression to be assessed, as shown by the dotted purple trace. Theoretically, any compensating slope infinitesimally above the stability boundary is sufficient to ensure stability.

Table 2 lists the inductor current imbalances at the end of a few cycles after the current reference step. The imbalances are computed as the magnitude of the difference between the minimum value of each perturbed inductor current trace at the end of a switching cycle

and the corresponding minimum value of the ideal unperturbed inductor current, denoted by the horizontal line $i_{L(MIN)}$.

Table 2. Current imbalances at end of switching cycles in Figure 26.

Imbalance	$s_C = 0$	$s_C = s_{C(O)}$	$s_C = 1.1s_{C(O)}$	$s_C = s_{C3} = 4.66s_{C(O)}$
di_{L0}	24.4 mA	20.0 mA	19.6 mA	9.30 mA
di_{L1}	29.8 mA	20.0 mA	19.2 mA	4.30 mA
di_{L2}	36.5 mA	20.0 mA	18.8 mA	2.01 mA
di_{L3}	44.5 mA	20.0 mA	18.4 mA	920 µA
di_{L4}	54.5 mA	20.0 mA	18.1 mA	440 µA
di_{L5}	66.5 mA	20.0 mA	17.7 mA	191 µA

For the constant-period peak-current mode non-inverting buck–boost power supply with circuit parameters specified in Figure 26, the value of s_{C3} is given by 93.2 kV/H, which is about 4.66 times the oscillating slope $s_{C(O)}$. Applying this compensation suppresses 90% of the imbalance in three switching cycles, as shown in Figure 26 and Table 2, with the imbalance reducing from 9.3 mA to 920 µA over this interval.

6. Conclusions

This work presents an insightful, comprehensive, and generalized time-domain framework to analyze sub-harmonic oscillations in constant-period peak- and valley-current control and suppress them using slope compensation. Unstated and unvalidated in the existing literature, the exact slope compensation boundary is derived to be half of the difference in the drain and energize slopes in peak mode and half of the difference in the energize and drain slopes in valley mode, lying beyond the traditionally accepted half-drain slope in peak mode and half-energize slope in valley mode criteria. This boundary is expressed explicitly in terms of basic operating parameters: input/output voltages and inductance, enabling straightforward interpretation and direct application at the design stage. The expressions derived for sub-harmonic gain and the compensation boundary are validated through simulations, with calculated and simulated results showing strong agreement across a wide range of duty cycles in both peak and valley mode. All simulations presented in this work are conducted in SPICE at 1 MHz, a typical operating frequency for constant-period peak/valley-current loops.

The impact of non-idealities on the energize duty cycle is quantified through simulations that incorporate inductor parasitic resistance and the on-resistance of the power converter switches. An analytical expression for the energize duty cycle in the presence of these parasitics is derived. Using practical ranges of parasitic resistances and inductor current, the results show that the energize duty cycle increases significantly relative to its ideal value, with simulation results showing strong agreement with the derived expression. Specifically, for parasitic resistances ranging from 100 mΩ to 500 mΩ and average inductor current from 400 mA to 1 A, the energize duty cycle increases by 12% to 150%. Given the duty-cycle-based limit ($d_E = 0.5$ for a system without parasitics), beyond which sub-harmonic oscillations arise, these results demonstrate that parasitics have a substantial impact on the onset of instability and must be carefully accounted for in design.

The absence of sub-harmonic oscillations in the Discontinuous-Conduction mode is also confirmed through simulation by examining how perturbations evolve across switching cycles. Unlike in CCM, where an initial imbalance propagates and transforms into subsequent imbalances depending on the sub-harmonic gain, DCM forces the inductor current to return to zero before the end of every switching period, eliminating any residual

imbalance from one cycle to the next. This behavior is validated in simulation by selecting an appropriately low peak-current reference.

Additionally, the widely recommended half-drain slope compensation in peak mode, although always stabilizing, does not provide a targeted measure of imbalance suppression and does not consistently align with optimal transient performance across duty cycles, being more aggressive than necessary over some energize duty cycle ranges and less effective in others. To enable a more pre-emptive performance-oriented design approach, a compensating slope s_{C3} is introduced, defined to suppress 90% of the initial imbalance within three switching cycles.

Across a range of duty cycles, the simulated compensation slope required to achieve 90% suppression in three switching cycles closely matches the value predicted by the analytical expression for s_{C3}, confirming its accuracy and generality. Furthermore, the suppression trends for the third cycle imbalance show that while increasing the compensation slope improves immediate imbalance reduction, the incremental benefit diminishes progressively, highlighting s_{C3} as a well-balanced and effective design choice.

A current-reference step response modeling a rapid change in load current in a practical circuit is used to evaluate how sub-harmonic oscillations can manifest and are suppressed under realistic transient conditions. The oscillating and stabilizing responses corresponding to the oscillating slope and a slightly higher slope (10% higher) are demonstrated to validate the theoretical boundary and its immediate vicinity. While $s_{C(O)}$ is shown to produce sustained oscillations and $1.1s_{C(O)}$ ensures stability with slow decay, these results establish that operating just beyond the boundary does not guarantee rapid suppression. The utility of s_{C3} is demonstrated in the same step response example, where it rapidly, as predicted, reduces the imbalance from 9.3 mA to 920 µA within three switching cycles.

To contextualize our contributions relative to the existing literature, Table 3 summarizes key analytical and design capabilities across relevant and representative prior works and highlights the gaps addressed by this work.

Table 3. Comparison with references.

Reference	Analysis Domain	Generalized Across Variants	Correct and Explicitly Derived Slope Boundary	Valley-Mode Covered	Parasitics Included	DCM Addressed	Targeted Suppression (Like s_{C3})
[3]	Both	No	No	No	No	No	No
[4]	Time	No	No	No	No	No	No
[6]	Both	Yes	No	No	No	No	No
[7]	Frequency	Yes	Partially	No	Partially	No	No
[8]	Both	Yes	No	No	No	No	No
[9]	Frequency	Yes	No	No	No	Partially	No
[10]	Both	Yes	No	No	No	No	No
[11]	Time	No	No	No	No	No	No
[16]	Both	No	No	No	No	No	No
[17]	Time	No	No	No	No	Yes	No
[19]	Time	No	No	No	No	No	No
[20]	Time	No	No	No	No	No	No
[21]	Time	No	No	No	No	No	No
[22]	Time	Yes	No	No	No	No	No

Table 3. *Cont.*

Reference	Analysis Domain	Generalized Across Variants	Correct and Explicitly Derived Slope Boundary	Valley-Mode Covered	Parasitics Included	DCM Addressed	Targeted Suppression (Like s_{C3})
[23]	Both	Yes	No	No	No	No	No
[25]	Both	Yes	Partially	No	No	No	No
[27]	Frequency	No	No	No	Partially	No	No
[28]	Time	No	No	No	No	No	No
[29]	Time	Yes	No	No	No	No	No
[30]	Time	No	No	No	No	No	No
This work	Time	Yes	Yes	Yes	Yes	Yes	Yes

Author Contributions: Conceptualization, A.T. and G.A.R.-M.; methodology, G.A.R.-M.; validation, A.T.; formal analysis, A.T. and G.A.R.-M.; investigation, A.T.; resources, G.A.R.-M.; writing—original draft preparation, A.T.; writing—review and editing, A.T. and G.A.R.-M.; visualization, A.T. and G.A.R.-M.; supervision, G.A.R.-M.; project administration, G.A.R.-M. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

Nomenclature

$A_{FW(PK)}$	Forward gain in a peak-current loop.
$A_{FW(VL)}$	Forward gain in a valley-current loop.
A_{SH}	Sub-harmonic gain.
$\beta_{FB(PK)}$	Feedback gain in a peak-current loop.
$\beta_{FB(VL)}$	Feedback gain in a valley-current loop.
C_O	Power stage output capacitor.
$C_{P(PK)}$	Peak-current loop comparator.
$C_{P(VL)}$	Valley-current loop comparator.
d_D	Draining the duty cycle.
d_D'	Ideal draining duty-cycle in absence of parasitics.
d_E	Energizing duty-cycle.
d_E'	Ideal energizing duty-cycle in absence of parasitics.
di_{L0}	Initial deviation from ideal unperturbed inductor current.
di_{L1}	End-of-first-cycle deviation from ideal unperturbed inductor current.
di_{L2}	End-of-second-cycle deviation from ideal unperturbed inductor current.
$di_{L(D)}$	Deviation from $i_{L(I)}$ generated in t_D.
$di_{L(E)}$	Deviation from $i_{L(I)}$ generated in t_E.
dt_D	Change in drain time.
dt_E	Change in energize time.
f_{CLK}	External clock's switching frequency.
f_{SW}	Switching frequency.
i_{IN}	Input current.
i_L	Inductor current.
$i_{L(I)}$	Ideal unperturbed inductor current.
$i_{L(MIN)}$	Minimum value of unperturbed ideal inductor current in peak mode.
$i_{L(PK)}$	Inductor peak-current reference.

$i_{L(VL)}$	Inductor valley-current reference.
i_{LD}	Load current.
i_{LI}	Flyback primary (input) side current.
i_{LO}	Flyback secondary (output) side current.
Δi_L	Inductor current ripple.
i_O	Output current.
k_T	Transformer voltage induced ratio.
L_X	Inductance.
L_{XI}	Flyback primary coil inductance.
L_{XO}	Flyback secondary coil inductance.
P_I	Input power.
P_O	Output power.
R_D	Total resistance of draining path.
R_{DG}	Ground drain switch on-resistance.
R_{DO}	Output drain switch on-resistance.
R_E	Total resistance of energizing path.
R_{EG}	Ground energize switch on-resistance.
R_{EI}	Input energize switch on-resistance.
R_L	Inductor parasitic resistance.
s_C	Applied compensation slope.
s_{C3}	Compensation slope at which 90% of imbalance is suppressed in three cycles.
$s_{C(O)}$	Compensation slope at which sub-harmonic gain is 1.
s_D	Draining slope of the inductor current.
S_{DG}	Ground drain switch.
S_{DO}	Output drain switch.
s_E	Energizing slope of the inductor current.
S_{EG}	Ground energize switch.
S_{EI}	Input energize switch.
SR_{PK}	Peak-current SR latch.
SR_{VL}	Valley-current SR latch.
t_C	Conduction time in DCM.
t_{CLK}	External clock's time period.
t_D	Draining portion of the switching period.
t_{DCM}	Time interval of zero inductor current in DCM.
t_E	Energizing portion of the switching period.
t_{SW}	Switching period.
v_C	Current loop reference voltage.
$v_C{}'$	Current loop reference voltage after adding compensation slope.
v_D	Draining voltage across the inductor.
$v_D{}'$	Ideal drain voltage in absence of parasitics.
v_E	Energizing voltage across the inductor.
$v_E{}'$	Ideal energize voltage in absence of parasitics.
v_{IFB}	Current-feedback voltage.
v_{IN}	Input voltage.
v_{IO}	Amplified current-error voltage.
v_O	Output Voltage.
v_{RD}	Ohmic voltage drop across R_D.
v_{RE}	Ohmic voltage drop across R_E.
v_{RL}	Ohmic voltage drop across R_L.
v_S	Sawtooth waveform needed for slope compensation.
v_{SWI}	Input switching node voltage.
v_{SWO}	Output switching node voltage.

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