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Transistor Frequency-Response Analysis: Recursive Shunt-Circuit Transformations

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Abstract: Frequency-response analysis is critical in circuit design. Frequency response encodes crucial information, like gain, accuracy, bandwidth, response time, phase shift, stability, and more. Unfortunately, existing methods are either algebraic and obscure or approximations with inaccuracies. So applying them to more complex circuits is often arduous or unreliable. This paper proposes recursive shunt-circuit transformations: a simple, rigorous, and insightful analytical method for conceptualizing and designing electronic circuits. The method asserts that (a) each equivalent capacitance shunts away its parallel resistance past its RC frequency. This (b) decreases the gain (induces a pole) and (c) changes the circuit. (d) The next dominant capacitance shunts its parallel resistance past the next pole and so on until all remaining capacitances shunt their parallel resistances past the poles they establish. The method also asserts that (e) bypass capacitances increase gain (induce zeros) and (f) cross-amp capacitances couple stages and poles. By applying this method and concepts, designers can (i) simplify an arbitrarily complex circuit into simpler coupled/decoupled stages and (ii) determine and manage poles and zeros with insight. This method was applied to design and analyze single- and multi- stage amplifier circuits and results were benchmarked against traditional methods and NGSPICE simulations, demonstrating its accuracy and broad applicability.

Keywords: frequency response; open-circuit approximation; short-circuit approximation; shunt-circuit approximation; common-gate/source/drain transistor stages; common-base/emitter/collector transistor stages; poles and zeros; time constants; Miller capacitance

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1. Introduction: Frequency Response in Electronic Circuits

Electronic circuits have carved for themselves a very fundamental place in today's modern world. From the smallest mobile phone to the largest spaceships, everything runs on semiconductor integrated circuit (IC) chips. These ICs have various electronic circuits designed for specific applications.

The design of a circuit is typically done by investigating its poles and zeros, i.e., the transfer function and frequency response. Figure 1 shows a general representation of an electronic circuit transfer function in terms of the input and output signals and impedances, i.e., $A_Z = v_O/i_I$.

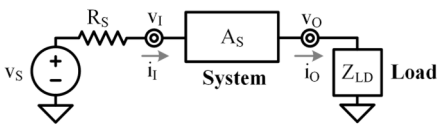

Figure 1. A general description of any electronic system.

Equations (1) and (2) show the transfer function of the system in terms of the DC gain A_{S0} and its various negative, real-valued poles and real zeros in the s-domain.

$$A_S = A_{S0}\left[\frac{\left(1 \pm \frac{s}{2\pi z_1}\right)\left(1 \pm \frac{s}{2\pi z_2}\right)\ldots\left(1 \pm \frac{s}{2\pi z_M}\right)}{\left(1 + \frac{s}{2\pi p_1}\right)\left(1 + \frac{s}{2\pi p_2}\right)\ldots\left(1 + \frac{s}{2\pi p_N}\right)}\right], \tag{1}$$

and

$$s = i2\pi f_O. \tag{2}$$

The transfer function can also be written in terms of its gain and phase as:

$$A_S = |A_S|\angle A_S, \tag{3}$$

where the gain is calculated by taking the modulus of the transfer function as:

$$|A_S| = A_{S0}\left[\frac{\sqrt{1 + \left(\frac{f_O}{z_1}\right)^2}\sqrt{1 + \left(\frac{f_O}{z_2}\right)^2}\ldots\sqrt{1 + \left(\frac{f_O}{z_M}\right)^2}}{\sqrt{1 + \left(\frac{f_O}{p_1}\right)^2}\sqrt{1 + \left(\frac{f_O}{p_2}\right)^2}\ldots\sqrt{1 + \left(\frac{f_O}{p_N}\right)^2}}\right], \tag{4}$$

and the phase is calculated by summing the different arguments in the transfer function as:

$$\begin{aligned}\angle A_S = \pm\tan^{-1}\left(\frac{f_O}{z_1}\right) \pm \tan^{-1}\left(\frac{f_O}{z_2}\right)\ldots\pm\tan^{-1}\left(\frac{f_O}{z_M}\right)\\ -\tan^{-1}\left(\frac{f_O}{p_1}\right) - \tan^{-1}\left(\frac{f_O}{p_2}\right)\ldots-\tan^{-1}\left(\frac{f_O}{p_N}\right).\end{aligned} \tag{5}$$

As can be seen from Equations (3)–(5), the poles decrease both gain and phase. Contrarily, the zeros increase the gain but add/subtract phase depending on whether they are in-phase "non-inverting" zeros or out-of-phase "inverting" zeros. These will be discussed further in Sections 4.3 and 5.3.

The frequency response of an electronic system is a useful tool in the designer's belt because it immediately makes evident the DC gain, bandwidth, minimum phase, poles and zeros of the system, phase loss/recovery of up to 90° by each pole/zero, phase difference of up to 90° between successive poles/zeros, gain plot slope after each pole/zero, etc. as seen in Figure 2. Therefore, it simplifies the analysis and makes drawing reliable conclusions pertaining to the gain, speed, and stability of the system intuitive and quicker.

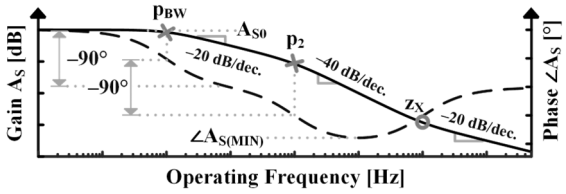

Figure 2. Sample frequency response for the system shown in Figure 1.

Because frequency response is such a useful tool, over the years, there has been a lot of interest in plotting it [1–10]. The most notable methods to obtain the transfer function and the frequency response are exact analysis using Kirchhoff's laws (KCL and KVL) [11–13], Miller's decomposition [4,6,11,14–17], Huijsing's shorting capacitance approximation [18,19], method of time constants [5,8,16,17,20–27], Middlebrook's generalized N-extra element theorem [28–30], and graphical analyses [31,32].

All the above methods are rigorous and mathematically intensive, but except for [18], lacking in insight. [18] develops insight for simpler higher order pole calculations but is often incorrect due to its misguided intuition (i.e., incorrect approximation that capac-

itances short beyond their poles). Therefore, there is a lack of an insightful method to calculate frequency responses of complex circuits accurately and hence, designers turn to numerical/symbolic simulations for reliable calculation of higher order poles/zeros to make design decisions [33–36].

In this paper, the authors propose an insightful design-oriented circuit analysis method to calculate poles and zeros and by extension, frequency responses accurately. They note that capacitances do not short past their RC frequencies, rather, they shunt their equivalent parallel resistances to reduce gain to the output and induce poles. They also remark that bypass capacitances increase gain to the output and induce zeros and cross-amplifier capacitances couple subsequent stages and poles.

They employ these and other fundamental concepts [1,37] to offer designers an intuitive and straightforward method for identifying and regulating circuit elements to achieve the desired frequency response during circuit design. Thus, the proposed insightful design-based analysis approach helps the designer conceptualize circuits, reduces his dependence on circuit simulations, alleviates challenges, and enhances the efficiency of circuit analysis and design by simplifying the analyses.

Section 2 introduces the readers to the tools required to apply the proposed method. Sections 3–5 show the treatment of basic single-stage amplifier circuits. Section 6 depicts the application of the method on multi-stage amplifier circuits. Section 7 comments on the accuracy and benefits of the method. Section 8 reiterates the findings of the paper by presenting the conclusions.

2. Proposed Frequency-Response Analysis

This section showcases and strengthens the four basic concepts the reader should know to apply the proposed frequency response analysis. Wherever applicable, it also mentions the concepts' intended use in the method. It culminates in an integrated idea which will be built upon in the following sections.

A short note on voltage/current naming convention: Uppercase variables with uppercase subscripts are dc signals. Lowercase variables with lowercase subscripts are ac signals and lowercase variables with uppercase subscripts are complete signals, i.e., ac riding on dc.

2.1. Shunt Circuits

A shunt circuit is a parallel combination of a signal source, R_{SH} and C_{SH} as depicted in the left part of Figure 3. Any circuit can be represented as a shunt circuit in its Norton equivalent. And every shunt circuit will have a RC pole frequency p_{SH} (given by (7)) when C_{SH}'s impedance equals R_{SH} as seen in (6).

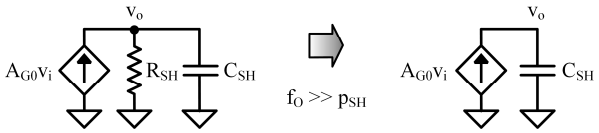

Figure 3. A shunt circuit below shunting pole p_{SH} and above p_{SH}.

Above p_{SH}, the C_{SH} bypasses R_{SH} by presenting the input with a lesser impedance path to ground and as a result, the effects of the resistance at the output begin fading. Sufficiently above p_{SH} ($f_O > 10p_{SH}$), R_{SH} completely disappears. See Figure 3. Simply put, C_{SH} shunts parallel R_{SH} past p_{SH} or, R_{SH} fades past p_{SH} because:

$$|Z_C| = \frac{1}{2\pi f_O C_{SH}}\Big|_{f_O \geq p_{SH}} \leq R_{SH}, \tag{6}$$

and

$$p_{SH} = \frac{1}{2\pi R_{SH} C_{SH}}. \tag{7}$$

The gain and phase error per pole/zero incurred by this simplification as compared to an exact analysis is given by:

$$\left|A_{V(Error)}\right|_{f_O=10p_{SH}} = \left|\frac{A_{G0}R_{SH}C_{SH}}{1+sR_{SH}C_{SH}}\right| - \left|\frac{A_{G0}}{sC_{SH}}\right| = \frac{A_{G0}R_{SH}}{\sqrt{101}} - \frac{A_{G0}R_{SH}}{10} \approx 0.5\% \tag{8}$$

and

$$\angle A_{V(Error)}\Big|_{f_O=10p_{SH}} = -\tan^{-1}\left(\frac{f_O}{p_{SH}}\right) - (-90^\circ) = -84^\circ + 90^\circ = 6^\circ. \tag{9}$$

Therefore, this simplification is a very good approximation to exact analysis that helps the designer gain insight into the circuit across frequency.

2.2. Feedback–Forward Split

Figure 4 shows an amplifier A_{G0} with a cross-amplifier capacitance C_X between the input and output nodes. At any given frequency, the capacitance C_X can be written as an equivalent two-port Norton input-Norton output circuit (refer middle third of Figure 4). The split can be defined in terms of the Y-parameters as:

$$\begin{cases} i_1 = y_{11}v_I + y_{12}v_O \\ i_2 = y_{21}v_I + y_{22}v_O \end{cases}. \tag{10}$$

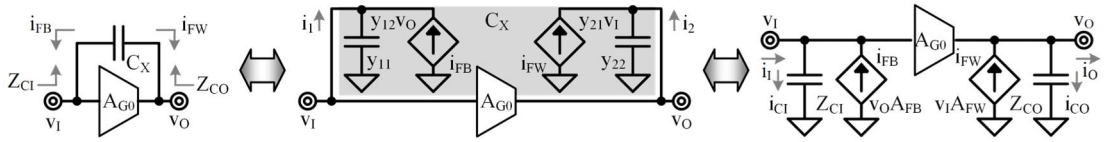

Figure 4. Cross-amp capacitance: splitting feedback and forward effects.

The equivalent input impedance is calculated by removing the load's feedback current (i.e., $v_O = 0$) as:

$$Z_{CI} = \frac{1}{y_{11}} = \frac{v_I}{i_I}\bigg|_{v_O=0} = \frac{1}{sC_X}. \tag{11}$$

The forward effect is the current C_X feeds to the unloaded (shorted) output (i.e., $v_O = 0$):

$$i_{FW} = v_I y_{21} = v_I A_{FW} = v_I\left(\frac{i_{FW}}{v_I}\right)\bigg|_{v_O=0} = \frac{v_I}{Z_{CI}} = v_I sC_X. \tag{12}$$

Similarly, the equivalent output impedance is calculated by removing the source's forward effect (i.e., $v_I = 0$):

$$Z_{CO} = \frac{1}{y_{22}} = \frac{v_O}{i_O}\bigg|_{v_I=0} = \frac{1}{sC_X}, \tag{13}$$

and the feedback effect is the current C_X feeds to the shorted input (i.e., $v_I = 0$):

$$i_{FB} = v_O y_{12} = v_O A_{FB} = v_O\left(\frac{i_{FB}}{v_O}\right)\bigg|_{v_I=0} = \frac{v_O}{Z_{CO}} = v_O sC_X. \tag{14}$$

These feedback and forward effects of C_X affect the higher order pole/zero calculations.

2.3. Cross-Amp Capacitance Split

At any given frequency, the cross-amp capacitance C_X in Figure 5 can also be split into an equivalent input/output capacitance C_{XI}/C_{XO}. This capacitance draws the same input/output current i_{XI}/i_{XO} as before, i.e., i_I/i_O.

By definition, the frequency-dependent voltage gain from the input to the output is:

$$A_V = \frac{v_O}{v_I}. \tag{15}$$

Therefore, the equivalent input conductance, i.e., the ratio of current through the equivalent input capacitance to the input voltage is:

$$G_{XI} = \frac{i_{XI}}{v_I} = \frac{i_{CI} - i_{FB}}{v_I} = \frac{v_I/Z_{CI} - v_O sC_X}{v_I} = (1 - A_V)sC_X \equiv sC_{XI}, \tag{16}$$

and similarly, the equivalent output conductance is:

$$G_{XO} = \frac{i_{XO}}{v_O} = \frac{i_{CO} - i_{FW}}{v_O} = \frac{v_O/Z_{CO} - v_I sC_X}{v_O} = \left(1 - \frac{1}{A_V}\right)sC_X \equiv sC_{XO}. \tag{17}$$

As seen in (16), the feedback effect increases the capacitance manyfold. The forward effect in (17), in contrast, decreases the capacitance. Since the voltage gain considered is frequency dependent, this cross-amplifier splitting concept, and the effects observed due to it are exact and rigorous across frequency. This is the same as Miller's effect and is used to transform the circuit to its shunt-circuit equivalent.

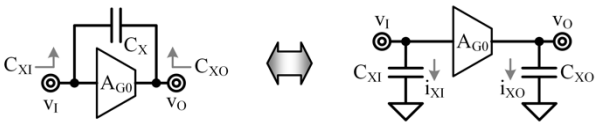

Figure 5. Cross-amp capacitance: splitting into input and output capacitances.

2.4. Recursive Shunt-Circuit Transformations

By the repeated application of concepts discussed in Sections 2.1–2.3, any circuit can be represented as an N-stage shunt-circuit, as observed in Figure 6. By employing the method of open-circuit time constants (OCTC) with the dominant pole approximation, p_1 is approximately the pole from an arbitrary X1th stage (Xi is a general index for the stage with the ith pole):

$$p_1 \approx \frac{1}{2\pi \mathrm{Max}_{k=1}^{N}\{R_k{}'C_k{}'\}} = \frac{1}{2\pi R_{X1}{}'C_{X1}{}'}. \tag{18}$$

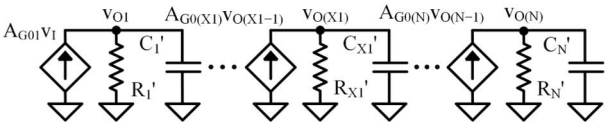

Figure 6. First-pole N-stage shunt-circuit.

Where $R_k{}'/C_k{}'$ denotes resistance/capacitance at the kth-stage in the 1st-pole shunt circuit. In general, $R_k{}'^M/C_k{}'^M$ denotes resistance/capacitance at the kth-stage in the Mth-pole shunt circuit. It is important to note that Xi may not be the ith stage.

The circuit is now changed to reflect $R_{X1}{}'$ being shunted away. A new shunt-circuit equivalent is calculated by merging the remaining capacitances and splitting the resulting

cross-amp capacitances. p_2 at the X2th stage (may not be the stage right after X1) is then computed by applying OCTC and dominant pole approx. again, albeit without R_{X1}':

$$p_2 \approx \frac{1}{2\pi \mathrm{Max}_{k=1,k\neq X1}^{N}\{R_k'' C_k''\}} = \frac{1}{2\pi R_{X2}'' C_{X2}''}. \tag{19}$$

Now the circuit is again changed to reflect the shunting away of R_{X2}'''. Similarly, the Mth pole of the circuit is given by applying OCTC and dominant pole approximation without $R_{X1}'^{(M-1)}$, $R_{X2}'^{(M-1)}$...$R_{X(M\text{-}1)}'^{(M-1)}$ as:

$$p_M \approx \frac{1}{2\pi \mathrm{Max}_{k=1,k\neq\{Xi\}}^{N}\left\{R_k'^{M}\middle|C_k'^{M}\right\}} = \frac{1}{2\pi R_{XM}'^{M} C_{XM}'^{M}}. \tag{20}$$

Above this frequency, $R_{X1}'^{M}$, $R_{X2}'^{M}$...$R_{XM}'^{M}$ have been shunted away. Therefore, the general idea thus becomes as follows: Apply suitable transformations to construct a shunt circuit. Then calculate the p_1 using OCTC and dominant pole approx. Now, shunt R_{X1} away and apply transformations to get another shunt circuit and repeat.

Note: The methodology proposed in this section applies most directly to analog broadband circuits like op-amps, voltage references, linear regulators, comparators, data converters, etc. whose sensitivity to on-chip and bond-wire introduced parasitic nH-pH inductances is often negligible. Therefore, the analysis only considers parasitic capacitances to calculate the poles/zeros (and frequency response).

3. Common-Gate Stage

Figure 7 shows a general single-stage common-gate circuit. This circuit has two independent nodes v_I and v_O, and no cross-amp capacitances.

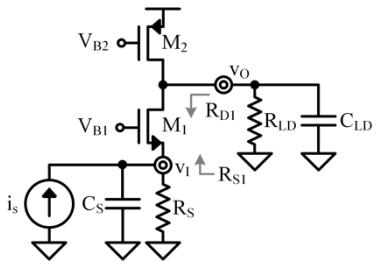

Figure 7. Common-gate stage.

3.1. Low-Frequency Circuit for Common-Gate Stage

Figure 8 shows the small-signal equivalent circuit. It is important to note that in this and subsequent figures, for the sake of compactness, the symbol for M_1 with a gray background represents the low-frequency small-signal model (with the "$-g_m v_{gs}$" current source i_{g1} and resistance r_{ds1} absorbed in it, i.e., resistive and transconductive components are included and capacitive and large-signal static dc components are excluded).

For low frequencies, the capacitances open and the circuit only presents resistive and transconductive components. The equivalent input resistance of this circuit includes R_{S1}, the resistance looking up into the source of M_1 and is given by:

$$R_I = R_S || R_{S1} = R_S || \frac{r_{ds1} + r_{ds2} || R_{LD}}{1 + g_{m1} r_{ds1}} \approx R_S || \frac{1}{g_{m1}}, \tag{21}$$

and the equivalent output resistance of the circuit includes R_{D1}, the resistance looking down into the drain of source degenerated M_1 and is given by:

$$R_O = R_{D1}||r_{ds2}||R_{LD} = (R_S + r_{ds1} + g_{m1}r_{ds1}R_S)||r_{ds2}||R_{LD} \approx r_{ds2}||R_{LD}. \quad (22)$$

Therefore, the low-frequency transimpedance gain is given by:

$$A_{Z0} = \frac{v_o}{i_s} = R_I A_{V0} = R_I g_{m1} R_O \approx \left(R_S||\frac{1}{g_{m1}}\right) g_{m1}(r_{ds2}||R_{LD}). \quad (23)$$

3.2. First-Pole Shunt Circuit for Common-Gate Stage

At intermediate frequencies, the circuit is shown in Figure 8. Now, input and output RC frequencies are compared to find the dominant pole.

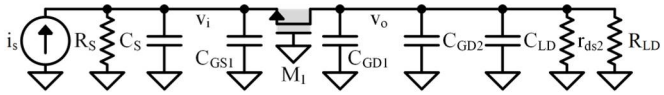

Figure 8. Small-signal model for the common-gate stage.

The input resistance R_I' is same as R_I calculated for A_{Z0} and is the parallel combination of resistances connecting v_i to ground:

$$R_I' = R_S||\frac{r_{ds1} + r_{ds2}||R_{LD}}{1 + g_{m1}r_{ds1}} \approx R_S||\frac{1}{g_{m1}}. \quad (24)$$

The equivalent input capacitance C_I' is the parallel combination of capacitances connecting v_i to ground:

$$C_I' = C_S + C_{GS1}. \quad (25)$$

Similarly, the equivalent output resistance R_O' is the parallel combination of all the resistances (to ground) at v_o:

$$R_O' = R_{LD}||r_{ds2}||(r_{ds1} + R_S + g_{m1}r_{ds1}R_S) \approx R_{LD}||r_{ds2}. \quad (26)$$

The equivalent output capacitance C_O' is the parallel combination of all the capacitances (to ground) at v_o:

$$C_O' = C_{LD} + C_{GD1} + C_{GD2} \approx C_{LD}. \quad (27)$$

Usually, f_O is dominant because of much higher R_O' in (26) yielding the highest RC product. Therefore, p_1 is given by:

$$p_1 = f_O = \frac{1}{2\pi R_O' C_O'} \approx \frac{1}{2\pi(R_{LD}||r_{ds2})C_{LD}}. \quad (28)$$

This p_1 is same as what Miller's approximation calculates.

3.3. Second-Pole Shunt Circuit for Common-Gate Stage

At frequencies much greater than p_1, R_O' fades away. Now, v_i is the only node with a resistance (refer (29)) and thus, produces p_2 with C_I'' in the input to output gain translation. The new input resistance R_I'' reflects the fading of R_O' and is:

$$R_I'' = R_S||\frac{1}{g_{m1}}||r_{ds1} \approx R_S||\frac{1}{g_{m1}}. \quad (29)$$

The new equivalent input capacitance C_O'' is:

$$C_I'' = C_S + C_{GS1}. \tag{30}$$

Therefore, p_2 is given by:

$$p_2 = f_I \approx \frac{1}{2\pi R_I'' C_I''} \approx \frac{1}{2\pi\left(R_S || \frac{1}{g_{m1}}\right)(C_S + C_{GS1})}. \tag{31}$$

3.4. Frequency Response for Common-Gate Stage

Figure 9 shows the Bode plot overlay of the frequency response calculated from proposed method over the simulated response from NGSPICE. Recall that the circuit has two independent nodes.

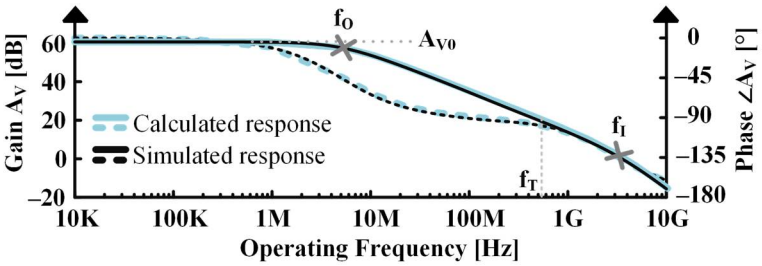

Figure 9. Frequency response of the common-gate stage.

As observed in the previous sections, each independent node has a pair of equivalent shunt capacitance and resistance that produce a pole. Therefore, the Bode plot is expected to, and observed, to have two poles, each losing up to 90° of phase. It is evident that the calculated response tracks the simulated one closely.

Table 1 presents the 180-nm transistor model parameters used in the circuits in Sections 3–6. As R_I'/R_I'' is highly sensitive to R_S, choosing a small R_S of the order of $\sim 1/g_m$ helps emphasize the g_m translation in it. Another factor motivating a small R_S is the mitigation of the source degenerating effect of R_S on g_m. Hence, a small R_S was chosen to aid in demonstrating the rigor of the method.

Table 1. Transistor Parameters Used in Simulations.

Parameters		
I_{CS} = 10 µA	W_{CS} = 20 µm	L = 1 µm
I_{CD} = 1 mA	W_{CD} = 5 mm	L_{OL} = 30 nm
I_{CG} = 10 µA	W_{CG} = 50 µm	K_N' = 200 µA/V [2]
C_{OX}'' = 7 fF/µm [2]	$\lambda_{N/P}$ = 2%	K_P' = 40 µA/V [2]
$R_{S(CS/CD)}$ = 5 MΩ [1]	$R_{LD} \rightarrow \infty$ Ω	V_{DD} = 5 V
$f_{T(CS)}$ = 470 MHz [2]	$f_{T(CD)}$ = 290 MHz [2]	$f_{T(CG)}$ = 280 MHz [2]
$V_{TN0} = \lvert V_{TP0} \rvert$ = 0.4 V	C_{J0} = 50 fF	tf = 100 ps
β_0 = 100 A/A	$I_{2/4(CE-CD)}$ = 200 µA	V_A = 50 V
I_S = 1fA	$I_{3/4(CS-CG-CD)}$ = 10 µA	γ = 600 mV

[1] R_S used for the common-gate stage is 200 Ω; [2] Calculated as per $f_T = \frac{g_m}{2\pi(C_{GS}+C_{GD})}$.

Note: For all the MOSFETs, body effect was neglected in Sections 3–5 for the sake of simplicity and clarity. However, including it is straightforward by adding back g_{mb} to transconductances and resistances (refer Sections 6.1 and 6.2). The reader is encouraged to interact with the designed circuit, adapt the equations to their circuit and verify their correctness.

Table 2 in Section 7 shows the comparison results between this work and poles extracted from other methods.

4. Common-Source Stage

Figure 10 shows a generalized single-stage common-source circuit. This circuit has two independent nodes v_I and v_O, and one cross-amp capacitance C_{GD1}.

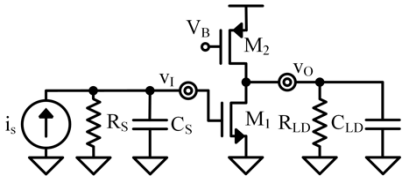

Figure 10. Common-source stage.

4.1. Low-Frequency Circuit for Common-Source Stage

Figure 11 shows the small-signal equivalent circuit. Once again, M_1 represents i_{g1} and r_{ds1}. Again, for low frequencies, the capacitances open. Therefore, the low-frequency transimpedance gain is given by:

$$A_{Z0} = \frac{v_o}{i_s} = R_S A_{V0} = R_S(-g_{m1})(r_{ds1}||r_{ds2}||R_{LD}). \tag{32}$$

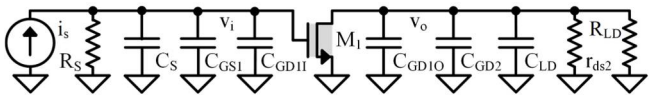

Figure 11. Small-signal model for the common-source stage.

4.2. First-Pole Shunt Circuit for Common-Source Stage

At intermediate frequencies, the circuit in Figure 10 can be redrawn as Figure 11 by employing the cross-amp capacitance splitting concept. The equivalent input resistance for the circuit is:

$$R_I' = R_S. \tag{33}$$

The equivalent input capacitance is the parallel combination of the capacitances connecting the input node v_i to ground, including the cross-amp capacitance that was split:

$$C_I' = C_S + C_{GS1} + C_{GD1I} \approx C_S + C_{GS1} + C_{GD1}(-A_{V0}). \tag{34}$$

Note: the cross-amp capacitance splitting has magnified C_{GD1} by a factor of A_{V0}.

Similarly, the output resistance is calculated by considering all the resistances connecting v_o to ground as:

$$R_O' = r_{ds1}||r_{ds2}||R_{LD}. \tag{35}$$

The equivalent output capacitance also includes the effect of the cross-amp capacitance splitting. It is given by:

$$C_O' = C_{GD1O} + C_{GD2} + C_{LD} \approx C_{GD1} + C_{GD2} + C_{LD}. \tag{36}$$

Note: the cross-amp capacitance splitting yields negligible effect at the output for circuits when voltage gain A_{V0} is much lesser than -1.

Again, both the input and output RC corner frequencies are compared, and f_I is found to be dominant due to the highest RC product as a result of the capacitance multiplicative effect at the input in (31). Therefore, p_1 is equal to f_I, as noted below:

$$p_1 = f_I \approx \frac{1}{2\pi R_I' C_I'} \approx \frac{1}{2\pi R_S[C_S + C_{GS1} + C_{GD1}(-A_{V0})]}. \tag{37}$$

This p_1 is same as what Miller's approximation calculates.

4.3. Second-Pole Shunt Circuit for Common-Source Stage

At frequencies much greater than p_1, R_I' fades away. Thus, the circuit is analyzed by breaking C_{GD1} using the feedback-forward split from Section 2. Other concepts can be used to redraw the circuit [4,6], but they are more mathematical whereas this tends to be simpler and gives more insight into the circuit, and is thus, preferred.

Now, the first thing to do is calculate the zero. This is because the effect of the forward component i_{FW} of C_{GD1} is exactly accountable at this stage. i_{FW} mixes with the current source i_{g1} in M_1 and results in a frequency dependent transconductance G_M:

$$G_M = \left.\frac{i_{FW} - i_{g1}}{v_I}\right|_{v_o=0} = v_i\left(\frac{sC_{GD1} - g_{m1}}{v_i}\right) = -g_{m1}\left(1 - \frac{sC_{GD1}}{g_{m1}}\right). \tag{38}$$

This G_M has a right half plane, positive, out-of-phase "inverting" zero. This zero occurs when i_{FW} of C_{GD1} competes with and overpowers i_{g1} of M_1 (refers (38) and (39)) and as a result, inverts the transconductance from negative to positive values. Beyond this zero, i_{g1} slowly fades away. Since the zero is drawing current from the system, it subtracts up to 90° of phase.

$$i_{FW} = v_i sC_{GD1}|_{f_O \geq z_{CS}} \geq i_{g1} = v_i g_{m1} \tag{39}$$

and

$$z_1 = z_{CS} = \frac{g_{m1}}{2\pi C_{GD1}}. \tag{40}$$

Once the zero has been noted, the forward components can be dropped to redraw the circuit. C_{GD1} can be rejoined to study the feedback effects affecting the second pole. Since the forward and feedback effects are linear, they can be decoupled, analyzed individually and later clubbed using superposition; this makes the analysis simpler. The circuit is given by Figure 12.

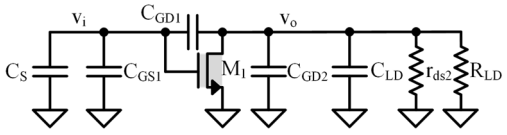

Figure 12. Equivalent second-pole common-source shunt circuit without forward components.

Figure 12 shows that C_{GD1}, C_S and C_{GS1} form a voltage divider from v_o to v_i. This feedback effect tends to diode connect M_1, as any change in v_o changes v_{gs1} (and i_{g1}). It appears as an equivalent resistance at the v_o given by:

$$R_{GM1} = \frac{v_o}{i_{g1}} = \frac{v_o}{g_{m1}v_i} = \frac{C_S + C_{GS1} + C_{GD1}}{g_{m1}C_{GD1}} \approx \frac{C_S + C_{GS1}}{g_{m1}C_{GD1}}. \tag{41}$$

Thus, the equivalent output resistance has contributions from R_{LD}, r_{ds1}, r_{ds2} and the voltage-divided g_m resistance R_{GM1}:

$$R_O'' = R_{GM1}||r_{ds1}||r_{ds2}||R_{LD} \approx R_{GM1}. \tag{42}$$

This voltage divider also effects the output capacitance C_O'' by appearing as an additional capacitance at v_o. A note on convention: $\oplus$ denotes a series connection, which means series capacitances are mathematically parallel, i.e., $C_A \oplus C_B = (C_A C_B)/(C_A + C_B)$.

$$C_O'' = [(C_S + C_{GS1}) \oplus C_{GD1}] + C_{GD2} + C_{LD}. \tag{43}$$

Therefore, p_2 at the output node v_o is given by:

$$p_2 = f_O \approx \frac{1}{2\pi R_O'' C_O''} \approx \frac{g_{m1} C_{GD1}}{2\pi (C_S + C_{GS1}) C_O''}. \tag{44}$$

4.4. Frequency Response for Common-Source Stage

Figure 13 shows the Bode plot overlaying the frequency response calculated from the proposed method over a NGSPICE simulation. The circuit has two independent nodes and one cross-amp capacitance.

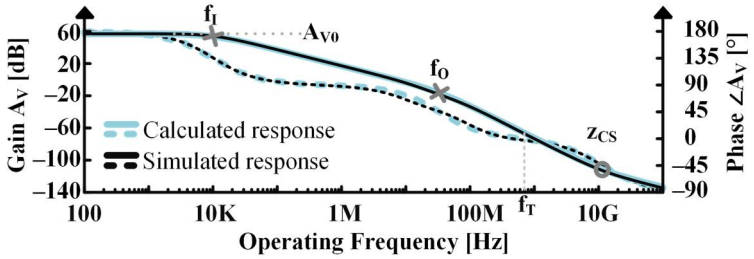

Figure 13. Frequency response of the common-source stage.

Recall that each independent node has a pair of equivalent shunt capacitance and resistance that produce a pole. Similarly, each cross-amp capacitance mixes with its transistor's i_g current source to produce a zero. Therefore, the Bode plot is expected to, and observed, to have two poles and a zero.

Each pole is losing up to 90° of phase and the inverting zero is losing another 90° of phase. It is evident that the calculated response tracks the simulated one closely. Table 2 in Section 7 shows a comparison of poles/zeros extracted from the proposed method versus the state-of-the-art methods.

5. Common-Drain Stage

Figure 14 shows a general single-stage common drain circuit. This circuit also has two nodes and a cross-amp capacitance. Therefore, it is also expected to have two poles and a zero.

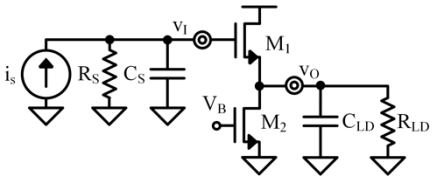

Figure 14. Common-drain stage.

5.1. Low-Frequency Circuit for Common-Drain Stage

Figure 15 shows the small-signal equivalent circuit. M_1 represents i_{g1} and r_{ds1}. The low-frequency transimpedance gain is given by:

$$A_{Z0} = \frac{v_o}{i_s} = R_S A_{V0} = R_S(g_{m1}) \left(\frac{1}{g_{m1}} || r_{ds1} || r_{ds2} || R_{LD} \right) \approx R_S. \tag{45}$$

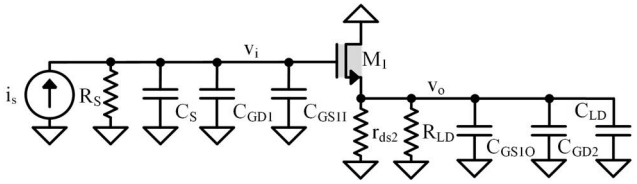

Figure 15. Small-signal model for the common-drain stage.

5.2. First-Pole Shunt Circuit for Common-Drain Stage

At intermediate frequencies, the circuit is drawn as Figure 15 by employing the cross-amp capacitance splitting concept on C_{GS1}. The equivalent input resistance for the circuit is:

$$R_I' = R_S. \tag{46}$$

The equivalent input capacitance is the parallel combination of the capacitances connecting the input node v_i to ground, including the effect of the cross-amp capacitance that was split:

$$C_I' = C_S + C_{GD1} + C_{GS1I} \approx C_S + C_{GD1}. \tag{47}$$

Similarly, the output resistance is calculated by considering all the resistances connecting v_o to ground. This includes the $1/g_{m1}$ resistance observed when looking up into the source of M_1:

$$R_O' = \frac{1}{g_{m1}} || r_{ds1} || r_{ds2} || R_{LD} \approx \frac{1}{g_{m1}}. \tag{48}$$

The equivalent output capacitance also includes the effect of the cross-amp capacitance splitting. It is given by:

$$C_O' = C_{GS1O} + C_{GD2} + C_{LD} \approx C_{GD2} + C_{LD} \approx C_{LD}. \tag{49}$$

Again, the input and output RC frequencies are compared, and f_I is found to be dominant due to the much higher R_I' in (46) yielding a higher RC product. Therefore, p_1 equals f_I, as noted below:

$$p_1 = f_I \approx \frac{1}{2\pi R_I' C_I'} \approx \frac{1}{2\pi R_S (C_S + C_{GD1})}. \tag{50}$$

p_1 is the result one would have obtained by applying Miller's approximation. Note: An important consequence of the cross-amp capacitance splitting concept is that in systems with positive voltage gain, the equivalent input/output capacitance decreases. If A_V is approximately one, like in the present case, $C_{XI/O}$ disappears. Refers (16), (17), (47) and (49).

5.3. Second-Pole Shunt Circuit for Common-Drain Stage

At frequencies much greater than p_1, R_I' fades away. Thus, the circuit is analyzed by breaking C_{GS1} using the feedback-forward split from Section 2.

Once again, the zero is calculated. It accounts for the forward effects of the cross-amplifier capacitance, C_{GS1}. i_{FW} and i_{g1} in M_1 mix to give a frequency dependent G_M as:

$$G_M = \left.\frac{i_{FW} + i_{g1}}{v_i}\right|_{v_o=0} = v_i \left(\frac{sC_{GS1} + g_{m1}}{v_i}\right) = g_{m1}\left(1 + \frac{sC_{GS1}}{g_{m1}}\right). \tag{51}$$

This G_M has a left half plane, negative, in-phase "non-inverting" zero. This zero occurs when i_{FW} overpowers i_{g1} in magnitude (refers (51) and (52)) by providing the source with

a lower impedance path to the output. Beyond this frequency, i_{g1} will slowly fade away. Since the zero is feeding current into the system, it recovers up to 90° of phase:

$$i_{FW} = v_i s C_{GS1}|_{f_O \geq z_{CD}} \geq i_{g1} = g_{m1} v_i \tag{52}$$

and

$$z_1 = z_{CD} = \frac{g_{m1}}{2\pi C_{GS1}}. \tag{53}$$

Once the zero has been noted, the forward components can be dropped to redraw the circuit as Figure 16. C_{GS1} is rejoined to study the feedback effects affecting the second pole. The only node with a resistance is v_o, so the pole appears at v_o.

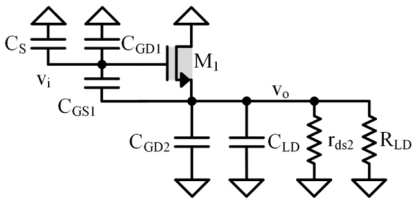

Figure 16. Equivalent second-pole common-drain shunt circuit without forward components.

Here, C_{GS1}, C_S and C_{GD1} form a voltage divider from v_o to v_i. This feedback effect tends to diode connect M_1, as any change in v_o changes v_{gs1} (and i_{g1}). It appears as an equivalent resistance at the v_o given by:

$$R_{GM1} = \frac{v_o}{i_{g1}} = \frac{v_o}{g_{m1} v_{gs}} = \frac{C_S + C_{GD1} + C_{GS1}}{g_{m1}(C_S + C_{GD1})} \approx \frac{C_S + C_{GS1}}{g_{m1} C_S}. \tag{54}$$

Thus, the equivalent output resistance has contributions from R_{LD}, r_{ds1}, r_{ds2} and the voltage-divided g_m resistance R_{GM1}:

$$R_O'' = R_{GM1} || r_{ds1} || r_{ds2} || R_{LD} \approx R_{GM1}. \tag{55}$$

This voltage divider also effects the output capacitance C_O'' by appearing as an additional capacitance in parallel at v_o. It is given by:

$$C_O'' = [(C_S + C_{GD1}) \oplus C_{GS1}] + C_{GD2} + C_{LD}. \tag{56}$$

Therefore, p_2 at the output node v_o is given by:

$$p_2 = f_O \approx \frac{1}{2\pi R_O'' C_O''} \approx \frac{g_{m1} C_S}{2\pi (C_S + C_{GS1}) C_O''}. \tag{57}$$

5.4. Frequency Response for Common-Drain Stage

Figure 17 shows the Bode plot overlay of the frequency response calculated from proposed method over the simulated response from NGSPICE. Each pole is losing up to 90° of phase and the non-inverting zero is recovering up to 90° of phase. It is evident that the calculated response tracks the simulated one closely. Table 2 in Section 7 shows a comparison of poles/zeros extracted from the proposed method versus the state-of-the-art methods.

Table 1 shows the design parameters used to simulate the circuit. R_{GM1} is noted to be very sensitive to the source capacitance. Any appreciable C_S will minimize the voltage division to produce a ~$1/g_m$ result as a simplification of the form in (54). Therefore, the circuit was designed without it.

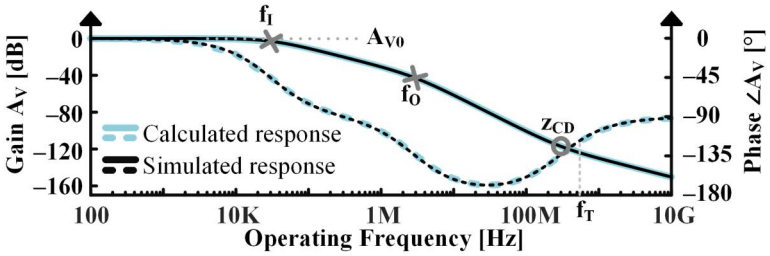

Figure 17. Frequency response of the common-drain stage.

6. Clustered Poles

In complex designs, the N-stage shunt circuit often exhibits closely spaced poles. This occurs when two or more capacitances shunt their respective parallel resistances less than a decade apart; this spacing is insufficient for the capacitances to fully shunt their parallel resistances. Consequently, the impedances interact as they are being shunted and the successive pole calculation sees the effect of the resistance from the "previous pole". In such scenarios, the treatment is dependent on whether the components exhibiting the pole are coupled or decoupled, as explained below.

6.1. Coupled Poles

A circuit has coupled stages when capacitances couple the shunt resistances connected at its ends. Therefore, a cross-amp. capacitance couples the input and output nodes it is connected across. The possibilities for such coupling appear in circuits with common-source/emitter stages through the C_{GD} or C_{BC}/C_{μ} capacitance as shown in gray in Figure 18, or common-drain/collector stages through the C_{GS} or C_{BE}/C_{π} capacitance as shown in gray in Figure 19.

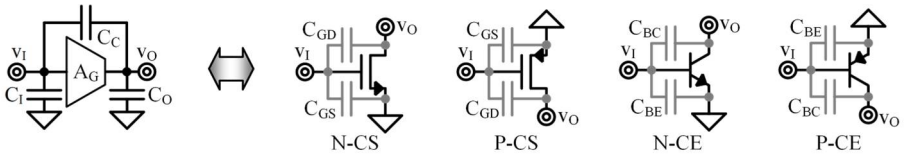

Figure 18. Coupling capacitances in common-source/emitter stages.

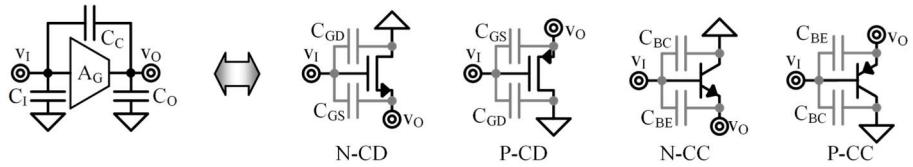

Figure 19. Coupling capacitances in common-drain/collector stages.

For two coupled poles p_1 and p_2 set by the RC corner frequencies f_I and f_O with $f_I < f_O$, f_I is RC frequency at the input node and is given by:

$$f_I = \frac{1}{2\pi R_I' C_I'}. \tag{58}$$

Similarly, f_O is the RC corner frequency at the output node and is given by:

$$f_O = \frac{1}{2\pi R_O' C_O'}. \tag{59}$$

Since the individual RCs are close together, their impedances interact and the effect of their RCs add. Therefore, the first pole, p_1, is approximated by their combined time constants as:

$$p_1 \approx \frac{1}{2\pi(R_I'C_I' + R_O'C_O')} = \frac{1}{1/f_I + 1/f_O} = f_I||f_O. \quad (60)$$

This means that the first pole is the parallel combination of the individual RC frequencies and is lower than the lowest of the two. The higher pole (lower time constant), p_2, tends to be higher than the first pole in the ratio of the individual time constants and can be mathematically expressed as:

$$p_2 \approx \frac{1}{2\pi(R_I'C_I' + R_O'C_O')R_O'C_O'/(R_I'C_I')} = p_1\left(\frac{R_I'C_I'}{R_O'C_O'}\right) = p_1\left(\frac{f_O}{f_I}\right). \quad (61)$$

Common Emitter–Common Drain Design Example

Figure 20 shows a general cascaded common emitter–common drain circuit. Since this circuit has cross-amp capacitances between subsequent nodes (and a wire short between o/p of Q_1 and i/p of M_3), this is an example of a coupled stage. Its transistor parameters are given in Table 1. It has three independent nodes v_I, v_X, and v_O and two cross-amp capacitances ($C_{\mu 1}$, C_{GS3}). Therefore, it is expected to have three poles and two zeros.

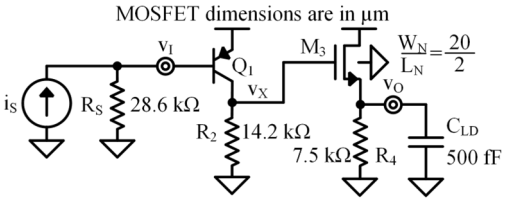

Figure 20. Cascaded common emitter–common drain circuit.

1. Low-Frequency Common Emitter–Common Drain Circuit

Figure 21 shows the small-signal equivalent. Here, Q_1 represents i_{g1}, $r_{\pi 1}$, and r_{o1} and M_3 represents i_{g3}, r_{ds3}. The low-frequency transimpedance gain is given by:

$$A_{Z0} = R_I A_{V0} = R_S||r_{\pi 1} A_{V10} A_{V30} \approx -R_I g_{m1}(r_{o1}||R_2) g_{m3}\left(\frac{1}{g_{m3}}||\frac{1}{g_{mb3}}||r_{ds3}||R_4\right). \quad (62)$$

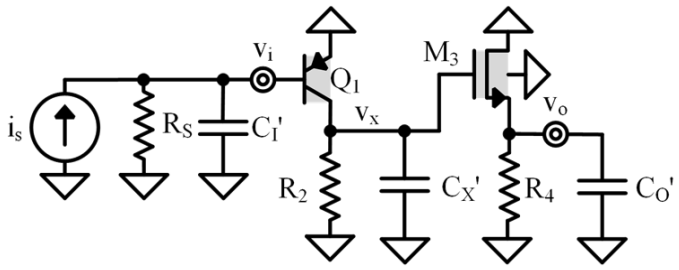

Figure 21. Small-signal model for the cascaded common emitter–common drain circuit.

2. First-Pole Common Emitter–Common Drain Shunt-Circuit

At intermediate frequencies, the capacitances come into play and the circuit is drawn by employing the cross-amp capacitance splitting concept on C_{BC1} and C_{GS3}. The poles at each node are compared, and f_I is found to be dominant due to the highest RC product

because of the capacitance multiplicative effect at the input. Therefore, p_1 equals f_I, as noted below:

$$p_1 = f_I \approx \frac{1}{2\pi R_I{}' C_I{}'} \approx \frac{1}{2\pi (R_S || r_{\pi 1})\left[C_{\mu 1} + C_{GD1}(-A_{V10})\right]}. \tag{63}$$

3. Second-Pole Common Emitter–Common Drain Shunt Circuit

At frequencies much greater than p_1, $R_I{}'$ fades away. Thus, the circuit is redrawn as Figure 22 using concepts from Section 2. $C_{\mu 1}$ now diode connects Q_1 and will lead to a voltage-divided gm at v_x. First, the forward effect is accounted for to get the zero from the common-emitter stage as:

$$z_{CE} = \frac{g_{m1}}{2\pi C_{\mu 1}}. \tag{64}$$

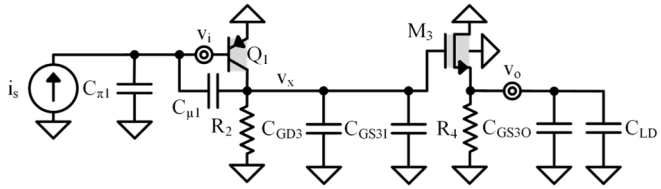

Figure 22. Second-pole common emitter–common drain shunt circuit.

Now, the RC product of $R_X{}''$ and $C_X{}''$ is computed. $R_X{}''$ is given as:

$$R_X{}'' = R_{GM1} || r_{o1} || R_2 \approx R_{GM1}, \tag{65}$$

where R_{GM1} is the voltage-divided g_m resistance given by:

$$R_{GM1} = \frac{C_{\pi 1} + C_{\mu 1}}{g_{m1} C_{\mu 1}} \approx \frac{C_{\pi 1}}{g_{m1} C_{\mu 1}}. \tag{66}$$

The equivalent capacitance at $C_X{}''$ is:

$$C_X{}'' = \left[C_{\pi 1} \oplus C_{\mu 1}\right] + C_{GD3} + C_{GS3I} = \left[C_{\pi 1} \oplus C_{\mu 1}\right] + C_{GD3} + C_{GS3}(1 - A_{V30}), \tag{67}$$

Then, the RC product of $R_O{}''$ and $C_O{}''$ is computed. $R_O{}''$ is given by:

$$R_O{}'' = \frac{1}{g_{m3}} || \frac{1}{g_{mb3}} || r_{ds3} || R_4. \tag{68}$$

The net capacitance at $C_O{}''$ is:

$$C_O{}'' = C_{GS3O} + C_{LD} = C_{GS3}\left(1 - \frac{1}{A_{V30}}\right) + C_{LD}, \tag{69}$$

Then, the RC products of $R_X{}'' C_X{}''$ and $R_O{}'' C_O{}''$ are compared to find that they are similar in magnitude with $R_O{}'' C_O{}''$ being slightly larger ($f_O{}'' < f_X{}''$). Therefore, p_2 in the i_s to v_o gain translation is given by:

$$p_2 \approx \frac{1}{2\pi (R_O{}'' C_O{}'' + R_X{}'' C_X{}'')} = f_O{}'' || f_X{}''. \tag{70}$$

4. Third-Pole Common Emitter–Common Drain Shunt Circuit

Typically, at frequencies much greater than p_2, $R_O{}''$ fades away. However, as $R_O{}'' C_O{}'' \approx R_X{}'' C_X{}''$ in this design, $R_O{}''$ persists for p_3 calculation. Thus, the circuit is

redrawn as Figure 23 using concepts from Section 2. First, the forward effect is accounted for to get the zero from the common-drain stage:

$$z_{CD} = \frac{g_{m3}}{2\pi C_{GS3}}. \tag{71}$$

Then, the next pole is calculated by employing the theory developed at the beginning of this section as:

$$p_3 \approx \frac{1}{2\pi(R_O''C_O'' + R_X''C_X'')R_X''C_X''/(R_O''C_O'')} = p_2\left(\frac{R_O''C_O''}{R_X''C_X''}\right) = p_2\left(\frac{f_X''}{f_O''}\right). \tag{72}$$

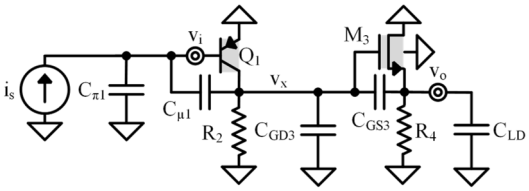

Figure 23. Third-pole common emitter–common drain shunt circuit.

5. Frequency Response for Common Emitter–Common Drain Circuit

Figure 24 shows the Bode plot overlay of the calculated poles/zeros from proposed method over the simulated response from NGSPICE. Table 3 in Section 7 shows the calculated results.

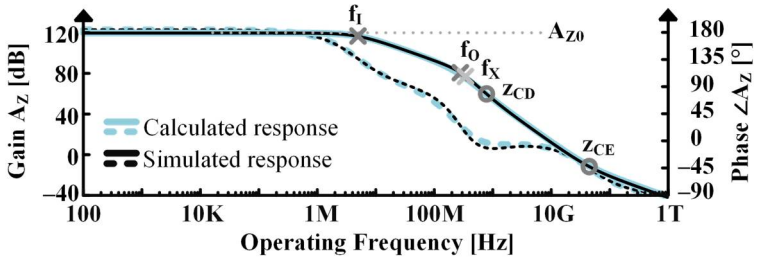

Figure 24. Frequency response of the common emitter–common drain circuit.

As can be seen from Table 3 and Figure 24, since the successive poles/zeros are within 1.5× of each other, they all act as clustered poles/zeros and influenced the circuit analysis/design accordingly. The proposed method was successfully able to predict the location of the poles by identifying the contributing element, enabling the circuit designer to control them as per the requirements of the design.

6.2. Decoupled Poles

Whenever a circuit decouples two nearby shunt resistances, it has decoupled stages which lead to decoupled poles. Therefore, the absence of a shorting connection (i.e., cross-amp capacitance) between the output of the first stage and the input of the next decouples the successive stages. The only possibility of such decoupling in a circuit is with a common-gate/base stage as shown in Figure 25.

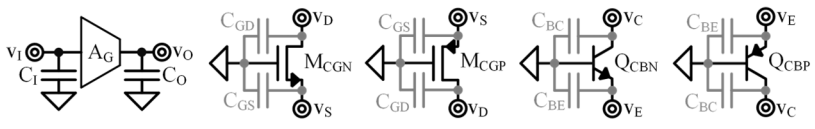

Figure 25. Decoupling capacitances in common-gate/base stages.

For two decoupled poles p_1 and p_2 set by the RC corner frequencies f_I and f_O with $f_I < f_O$, the poles are given by the individual RC frequencies independent of the other. The first pole becomes the one with the larger RC product. Therefore, p_1 is given by:

$$p_1 \approx f_I = \frac{1}{2\pi R_I{}' C_I{}'}. \tag{73}$$

Similarly, p_2 is given by the lower RC product as:

$$p_2 \approx f_O = \frac{1}{2\pi R_O{}' C_O{}'}. \tag{74}$$

Common Source–Common Gate–Common Drain Design Example

Figure 26 shows a general cascaded common source–common gate–common drain circuit. Since v_X and v_Y do not have a shorting connection between them, the common-source stage is decoupled from the common-drain stage. Its transistor parameters are also given in Table 1. It has four independent nodes v_I, v_X, v_Y, and v_O and two cross-amp capacitances (C_{GD1}, C_{GS5}). Therefore, it is expected to have four poles and two zeros.

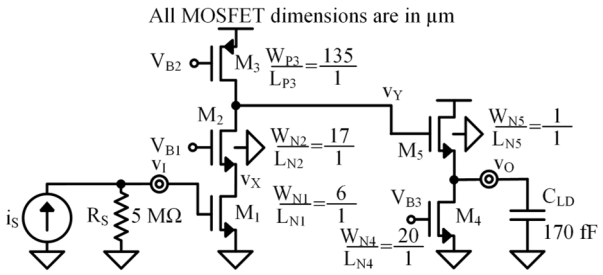

Figure 26. Cascaded common source–common gate–common drain circuit.

1. Low-Frequency Common Source–Common Gate–Common Drain Circuit

Figure 27 shows the small signal equivalent circuit (where the body terminals have been dropped to favor clarity). Here, M_i represents i_{gi}, and r_{dsi}. The low-frequency transimpedance gain depends on the different resistances in the signal path from i_S to v_O. The equivalent resistance at the drain of M_1 is:

$$R_{D1} = r_{ds1} || \frac{r_{ds2} + r_{ds3}}{1 + (g_{m2} + g_{mb2}) r_{ds2}} \approx \frac{2}{g_{m2} + g_{mb2}}. \tag{75}$$

Similarly, the equivalent resistance at the drain of M_2 is:

$$R_{D2} = r_{ds3} || (r_{ds1} + r_{ds2} + g_{m2} r_{ds1} r_{ds2}) \approx r_{ds3}. \tag{76}$$

The equivalent resistance at the source of M_5 is:

$$R_{S5} = r_{ds4} || \frac{1}{g_{m5} + g_{mb5}} || r_{ds5} \approx \frac{1}{g_{m5} + g_{mb5}}. \tag{77}$$

Therefore, the low-frequency transimpedance gain is:

$$\begin{aligned} A_{Z0} &= R_I A_{V0} = R_S A_{V10} A_{V20} A_{V50} \\ &= -R_I g_{m1} R_{D1} g_{m2} R_{D2} g_{m5} R_{S5} \approx -2 R_S g_{m1} r_{ds3}. \end{aligned} \tag{78}$$

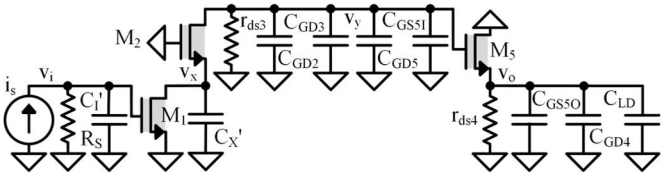

Figure 27. Small-signal model for the cascaded common source–gate–drain circuit.

2. First-Pole Common Source–Common Gate–Common Drain Shunt Circuit

At intermediate frequencies, the circuit is still given by Figure 27 with the capacitances being finite. The RC corner frequencies at each node are compared, and it is found that $f_I \approx f_Y$ with $R_I'C_I'$ being slightly larger. The equivalent input resistance is:

$$R_I' = R_S. \tag{79}$$

The equivalent input capacitance after application of the cross-amp capacitance split is:

$$C_I' = C_{GS1} + C_{GD1}(1 - A_{V10}). \tag{80}$$

The equivalent resistance at the node v_y is the parallel combination of the output resistance of source degenerated M_2 and r_{ds3}. Usually, r_{ds3} is much lesser and survives:

$$R_Y' = R_{D2} \approx r_{ds3}. \tag{81}$$

The equivalent capacitance at v_y after application of the cross-amp capacitance split is:

$$C_Y' = C_{GD2} + C_{GD3} + C_{GD5} + C_{GS5}(1 - A_{V50}). \tag{82}$$

Since $f_I \approx f_Y$ with $R_I'C_I'$ being slightly larger, p_1 equals f_I, as noted below:

$$p_1 \approx f_I = \frac{1}{2\pi R_I'C_I'} = \frac{1}{2\pi R_S(C_{GS1} + C_{GD1}(1 - A_{V10}))}. \tag{83}$$

3. Second-Pole Common Source–Common Gate–Common Drain Shunt Circuit

Typically, at frequencies much greater than p_1, R_I' fades away. However, as $R_I'C_I' \approx R_Y'C_Y'$ in this design, R_I' persists for p_2 calculation. Thus, the circuit is still given by Figure 27. First, the forward effect is accounted for to get the zero from the common-source stage:

$$z_{CS} = \frac{g_{m1}}{2\pi C_{GD1}}. \tag{84}$$

Then, the RC product at node v_y is computed to find the next pole as:

$$p_2 = f_Y \approx \frac{1}{2\pi R_Y'C_Y'}. \tag{85}$$

4. Third-Pole Common Source–Common Gate–Common Drain Shunt Circuit

At frequencies much greater than p_2, R_I' and R_Y' fade away. Thus, the circuit is redrawn as Figure 28 using cross-amp capacitance splitting for M_5. Again, the RC products are compared to find f_O as the dominant pole. The equivalent output resistance in this new shunt circuit is:

$$R_O''' \approx R_{S5} = \frac{1}{g_{m5} + g_{mb5}}. \tag{86}$$

The equivalent output capacitance after the application of cross-amp capacitance split for M_5 is:

$$C_O''' = C_{GS5}\left(1 - \frac{1}{A_{V50}}\right) + C_{GD4} + C_{LD}. \tag{87}$$

Therefore, p_3 is given by:

$$p_3 = f_O \approx \frac{1}{2\pi R_O''' C_O'''}. \tag{88}$$

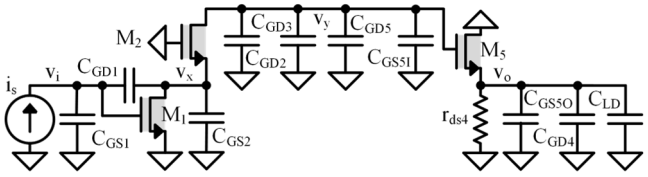

Figure 28. Third-pole common source–common gate–common drain shunt circuit.

5. Fourth-Pole Common Source–Common Gate–Common Drain Shunt Circuit

At frequencies much greater than p_3, R_O''' fades away. Thus, the circuit is redrawn as Figure 29 by using the feedback-forward splitting concept. First, the forward effect is accounted for to get the zero from the common-drain stage as:

$$z_{CD} = \frac{g_{m5}}{2\pi C_{GS5}}. \tag{89}$$

Then, the equivalent resistance at v_x is calculated as:

$$R_X'''' = R_{GM1} || r_{ds1} || \frac{1}{g_{m2} + g_{mb2}} || r_{ds2} \approx R_{GM1} || \frac{1}{g_{m2} + g_{mb2}}, \tag{90}$$

where R_{GM1} is the voltage-divided g_m resistance of M_1 given by:

$$R_{GM1} = \frac{C_{GS1} + C_{GD1}}{g_{m1} C_{GD1}}. \tag{91}$$

The equivalent capacitance at v_x includes the effect of the voltage divider established by C_{GD1} and C_{GS1} in M_1 and is given by:

$$C_X'''' = (C_{GD1} \oplus C_{GS1}) + C_{GS2}. \tag{92}$$

Therefore, p_4 is given by:

$$p_4 = p_X \approx \frac{1}{2\pi R_X'''' R_X''''}. \tag{93}$$

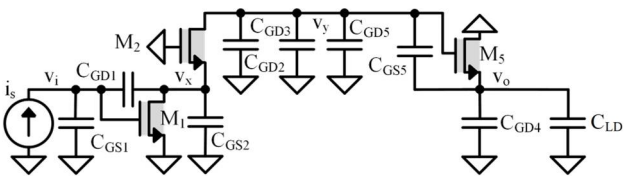

Figure 29. Fourth-pole common source–common gate–common drain shunt circuit.

6. Frequency Response for Common Source–Common Gate–Common Drain Circuit

Figure 30 shows the Bode plot overlay of the calculated poles/zeros from proposed method over the simulated response from NGSPICE. Table 3 in Section 7 shows the calculated results.

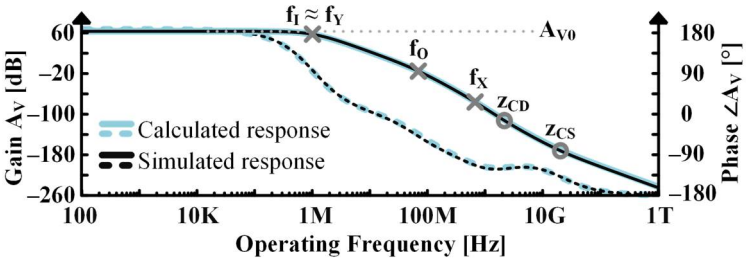

Figure 30. Frequency response of common source–common gate–common drain circuit.

As can be seen from Table 3 and Figure 30, there is a double pole at 1 MHz which is correctly predicted by the proposed method. Moreover, it identifies the contributing component for each pole and gives the designer a way to insightfully control such clustered poles reliably.

7. Benefits for Design

This section introduces the reader to the design perspective of an IC designer and the appropriate analytical methods investigated for analyzing and designing electronic circuits. It then compares them with the proposed methodology to validate its strength as compared to the others. Finally, the section concludes with comments upon the benefit of using the proposed methodology in addition to commercial circuit simulation tools.

7.1. Design Perspective

An IC design engineer is looking for small-signal circuit analysis methods which allow the engineer to readily and insightfully conceptualize and analyze a circuit to predict performance as reliably as commercial circuit simulation tools. The ability to conceptualize a circuit and decompose it into its fundamental components, helps the engineer to simplify and quicken the design process, since he is designing based on his conceptual understanding, and not trial-and-error using simulations.

This implies that range of applicability, ease of application and computation time are of utmost importance in these methods. Thus, Kirchoff's circuit laws [11], Miller's decomposition [14], Huijsing's capacitance short approximation [18], Andreani and Mattisson's modification [20] to Cochrun-Grabel's method [8] and graphical analyses [31,32] are identified as the state-of-the-art (SoA) methods to compare against.

7.2. Direct Analysis

Applying Kirchoff's laws gets the designer the circuit's exact transfer function. However, it is a tedious and purely mathematical process. For complicated circuits, the transfer function's poles and zeros become unsolvable by hand.

A numerical solver can be used to aid the analysis. If the poles are clustered together, the solver may return pairs of complex conjugate poles instead of real ones. In this case, a dominant terms approximation can be used.

To apply the approximation, first, the denominator of the transfer function of the circuit is written in the form of a polynomial as:

$$f(s) = a_n s^n + a_{n-1} s^{n-1} + \ldots + a_1 s + 1. \tag{94}$$

According to this approximation, at extremely low frequencies (for p_1), the linear and constant terms dominate and p_1 is given by:

$$f(s)|_{f \to p_1} \approx a_1 s + 1 = 0 \Rightarrow p_1 \approx -\frac{1}{2\pi a_1} \tag{95}$$

At intermediate frequencies (e.g., p_2), the quadratic and linear terms dominate the expression. This implies that p_2 is given by the following equation:

$$f(s)|_{f\to p_2} \approx a_2 s^2 + a_1 s = 0 \Rightarrow p_2 \approx -\frac{a_1}{2\pi a_2} \tag{96}$$

At even higher frequencies, the subsequent terms dominate and the calculation repeats. Therefore, the p_n becomes:

$$f(s)|_{f\to p_n} \approx a_n s^n + a_{n-1} s^{n-1} = 0 \Rightarrow p_n \approx -\frac{a_{n-1}}{2\pi a_n} \tag{97}$$

Verification: Let $f(s) = s^4 + 57s^3 + 361s^2 + 555s + 250$. The exact roots are -1, -1, -5, and -50 rad/s. The approximation yields -0.45, -1.5, -6.3, and -57 rad/s. Note: This approximation is extremely accurate when each pole is at least a decade away from the others. It is a less accurate but still extremely useful estimate for the locations of clustered poles. However, as explained above, obtaining the circuit's transfer function (or characteristic equation) for such an analysis becomes a daunting task as the circuit complexity increases.

7.3. Graphical Analyses

As an alternative to the daunting direct analysis, [31] uses driving port impedances combined with signal flow graphs to compute both, the poles, and zeros. While the process is easy to follow and exact, it is mathematically involved and becomes abstruse with increasing circuit complexity. In contrast, [32] develops insight into pole placement and their root-loci but does not connect the poles with changes occurring in the circuit because of them. Therefore, both these methods fail to equip the designer with a streamlined process to control each pole individually.

7.4. Short-Circuit Approximation

Instead of applying the above methods, designers can use an amalgamation of methods [14,18,20] for finding the poles/zeros of a transfer function. Ref. [14] brings insight for the lowest frequency pole. Ref. [18] introduces insight for higher poles but is misguided due to the underlying short circuit assumption– it assumes that capacitances short past their poles and diode-connect their corresponding transistors. This assumption produces $1/g_m$ instead of the voltage-divided-g_m suggested by (41) or (54) for R_O'' and often leads to errors in the final answer (refer common-source/drain p_O in Table 2).

Zero calculation using [20] is exact but mathematically intensive due to the calculation of multiple driving port time constants. It requires the designer to familiarize himself with two uncommon and not-so-straightforward components: the norator and nullator. It is also devoid of intuition into the circuit behaviour across the entire frequency spectrum.

To emphasize, the SoA methods either ascertain only the poles or zeros or calculate both but are tedious to apply on complicated circuits. Either way, they lack the beauty and simplicity of insight. Ref. [18] is a good compromise as it is the only insightful method (resulting in a simpler design process for larger, complex circuits) amongst the SoA. However, it is limited to the poles and often yields incorrect results.

7.5. Proposed Shunt-Circuit Approximation

The proposed method to calculate frequency response surpasses the SoA by not needing complex mathematical operations regardless of the circuit's complexity. It offers the design engineer insightful and accurate circuit analysis to predict both poles and zeros across the frequency range while retaining simplicity without losing sight of the circuit's functionality. It employs a shunt circuit approximation because, capacitances do not short

past their poles, instead, their parallel resistances fade. It swiftly makes evident the circuit element responsible for each pole/zero and provides a way to control/account for it in subsequent analyses during circuit design. To reiterate, the proposed method is a physical model (not a mathematical one) based on intuition which is used to conceptualize, analyze and design circuits and not simulating them.

Table 2 compares the poles/zeros (rounded off to two significant figures) calculated using SPICE simulations, Kirchoff's circuit laws (direct analysis), the SoA comprising of the combination of methods from [14] (p_1), [18] (p_2) and [20] (z_1), and the proposed method. The extraction of poles/zeros from the simulation was straightforward. p_1 is the frequency where the gain drops by 3 dB below the dc value (alternatively, phase loses 45° from the corresponding dc value) and p_2 is the frequency where the phase loses 90° (additional 45° from p_1 and 45° from p_2) from p_1's phase value. For an inverting zero (e.g., z_{CS}), z_1 is the frequency where it loses 90° (additional 45° from p_2 and 45° from z_1) from p_2's phase. On the other hand, for a non-inverting zero (e.g., z_{CD}), z_1 is the frequency where it partially cancels up to 45° of p_2's additional loss to return to the same phase value as that of p_2.

Table 2. Simulated Versus Calculated Single-Stage Amplifiers.

Stage	Pole Zero	Sim.	Direct	SoA	Error with Sim.	This Work	Error with Sim.
CG	p_O	5.0 MHz	4.9 MHz	4.9 MHz	−2.5%	4.9 MHz	−2.5%
	p_I	3.6 GHz	3.6 GHz	3.6 GHz	+1.9%	3.6 GHz	+1.9%
CS	p_I	10 kHz	10 kHz	10 kHz	−1.9%	10 kHz	−1.9%
	p_O	34 MHz	35 MHz	310 MHz	+810%	34 MHz	−2.6%
	z_{CS}	11 GHz	11 GHz	11 GHz	+0.9%	11 GHz	+0.9%
CD	p_I	30 kHz	30 kHz	31 kHz	+3.3%	31 kHz	+3.3%
	p_O	3.1 MHz	3.0 MHz	58 MHz	+1800%	3.0 MHz	−3.2%
	z_{CD}	280 MHz	300 MHz	300 MHz	+7.1%	300 MHz	+7.1%

Since the common-gate circuit did not have a cross-amplifier capacitance, there were fewer approximations in the equations and all the three methods resulted in very similar poles.

For all the methods, the zero expressions were identical to each other. The primary reason being that Kirchoff's circuit laws and the method in [20], are exact. As are the expressions derived in this work due to complete consideration of the forward effects.

As can be seen from Table 2, the direct analysis gets the closest results to the simulation. This work provides an alternative close approximation to the simulation that is quick and easy to use and provides insight into actual changes in the circuit. Therefore, for demonstrating the strength of the method for multi-stage amplifiers, it will be compared to results obtained from direct analysis.

Table 3. Calculated Multi-Stage Amplifier Examples.

Stage	Pole Zero	Direct	SoA	This Work
CE-CD	p_I	4.9 MHz	5.0 MHz	5.0 MHz
	p_O	230 MHz [1]	450 MHz	280 MHz
	p_X	370 MHz [1]	950 MHz	390 MHz
	z_{CD}	800 MHz	800 MHz	800 MHz
	z_{CE}	46 GHz	46 GHz	46 GHz
CS-CG-CD	p_I	500 kHz [1]	1.0 MHz	1.0 MHz
	p_Y	2.0 MHz [1]	17 MHz	1.0 MHz
	p_O	60 MHz	70 MHz	70 MHz
	p_X	680 MHz	730 MHz	680 MHz
	z_{CD}	2 GHz	2 GHz	2 GHz
	z_{CD}	20 GHz	20 GHz	20 GHz

[1] Calculated using dominant terms method.

As can be seen from Table 3, this work is very close to the direct analysis even for multi-stage circuits with clustered poles. As shown in Section 6, any large circuit of arbitrary complexity can be decomposed into a combination of the three primitive single-stage transistors stages presented in Sections 3–5. With the analyses formally discussed above, any combination of the primitive transistor stages can be completely analyzed and understood.

Once a large circuit is decomposed into its primitive stages (fundamental components), using the method proposed in this work, the design engineer can accurately predict the frequency response during circuit inspection. The accurately calculated poles and zeros streamline the design process and help the designer achieve the desired response in the preliminary design without multiple iterations. With the insight thusly gained, the design engineer can minutely control poles and zeros of any CMOS and bipolar technology circuit without having to rely solely on commercial circuit simulators or symbolic circuit analysis tools for making design decisions. Thus, the method can be very easily used to insightfully understand and design frequency responses of large circuits of arbitrary complexity simply.

Often, symbolic circuit analysis tools used to calculate poles/zeros produce complex equations that are hard to grasp and simplifying them might lead to significant pole/zero displacements from the original locations [33]. Circuit simulators, used to bridge this gap, are inadequate because they depend on numerical factors the engineer may not fully understand–this leads to circuits designed by "trial and error" as opposed to insight. This work enables the engineer to effectively address the aforementioned gap with insight. Since the preliminary design has the desired frequency response, supplementing it with simulations leads to a higher quality design with fewer iterations in the transistor parameters, i.e., the proposed method simplified the analysis and design of the circuit.

After the design engineer has designed a circuit, it needs to be stabilized. Typically, for analog broadband circuits considered in this paper, both open loop and closed loop (with negative feedback) stability are ensured using either dominant-pole compensation or pole-splitting compensation (Miller's compensation and its variants). This can be achieved using algebraic manipulation [38,39] to extract parameter values, graphical methods [32,40] to vary parameters until desired specifications are met, or solving for phase margin [41] to check stability while varying parameters.

Apart from [41], none of the other methods are as straightforward to employ with increasing circuit complexity. In a similar vein as [41], using the proposed method to predict the poles and zeros, designers can very easily check the stability of the circuit by inspecting the phase margin. Since the proposed method also equips the designer with the insight to control the poles and zeros, tweaking them (in the feedback network or otherwise) to meet specifications becomes a trivial matter. Hence, the proposed method is a design-oriented analytical method which organically lends itself to also simplifying feedback control of circuits regardless of circuit complexity.

8. Conclusions

This paper proposes an insightful design-based frequency response analysis of transistor circuits that also serves as the reference analysis for all single-stage amplifier primitives. The biggest challenge in a frequency response analysis is the lack of an easy, conceptual method to deduce the higher order poles. State-of-the-art (SoA) methods like short-circuit approximations in [18] are applicable but lead to a tedious procedure with often incorrect results. The proposed design-oriented analytical method outperforms the SoA by its ability to predict (without abstract math) and control circuit components that establish poles and zeros in a circuit. It recognizes that shunt capacitances reduce gain to the output, thereby inducing poles. Similarly, bypass capacitances increase gain to the output and induce zeros in the circuit. The proposed method also notes that resistances fade when their

parallel capacitances shunt them past their respective RC frequencies. As the resistances fade, the circuit changes and this method equips the design engineer to track all such changes across the entire frequency spectrum while ensuring comprehensive and rigorous results without sacrificing generality. Further, this work also identifies that cross-amplifier capacitances couple subsequent stages and lead to coupled poles in a circuit. By applying this method, the designer can recognize capacitances that cause poles/zeros as well as the coupled/decoupled stages in the circuit during inspection itself. It also provides the engineer with insight into how poles/zeros alter gain in circuits.

This was demonstrated by applying the methodology to design and analyze single-stage common-gate, common-source and common-drain stages and multi-stage cascaded common emitter–common drain and common source–common gate–common drain amplifiers. The results from the method were compared with those from established methods in the literature and NGSPICE simulations. The results agreed with the simulated values in a relatively tight ~5% error band as opposed to 800%+ error in the SoA. This establishes it as an invaluable tool for designers thanks to the insight provided and easier design and control of a stable circuit facilitated, as opposed to designing using abstract algebraic equations which hide concepts and make individual effects of components harder to decipher.

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