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Digital LDO Analysis and All-Stable High-PSR One-LSB Oscillator Design

Utsav Vasudevan [1,*] and Gabriel A. Rincón-Mora [2]

[1] Analog Devices Inc., Wilmington, MA 01887, USA
[2] School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332, USA; rincon-mora@gatech.edu
* Correspondence: utsav.vasudevan@analog.com

Abstract: Digital low-dropout (LDO) regulators are popular in research today as compact power supply solutions. This paper provides a unique approach to analyze digital LDO feedback mechanics and stability, to reduce voltage ripple and extend operating speed over the state-of-the-art. A novel error-subtracting counter is proposed to exponentially improve the response time of any digital LDO, to keep the loop stable outside the typical operating limits, and to increase power-supply rejection (PSR). This leverages the fact that digital LDOs are fundamentally one-bit relaxation oscillators in steady-state. Theory and simulations show how the analog-to-digital (ADC) and digital-to-analog converters (DAC) in these systems affect stability. When compromised, a digital LDO produces uncontrolled sub-clock oscillations at the output that the proposed error-subtracting counter removes.

Keywords: digital control; ADC; stabilization; regulation; power-supply rejection; fast transient; limit-cycle oscillation; noise; DVFS; SoC

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1. Introduction: On-Chip Power Supplies for Digital Systems

Digital systems are pervasive due to their inherent noise tolerance. As devices shrink and more functionality is packed into a limited space, power demands increase, and engineers turn to Dynamic Voltage and Frequency Scaling (DVFS) [1]. Each functional block within a System-on-Chip (SoC) requires an optimized supply voltage, leading to the use of local Point-of-Load (PoL) supplies. LDOs stand out here due to their compactness and low-noise outputs when compared to Switched-Mode Power Supplies (SMPS).

LDOs take in a supply voltage from an off-chip SMPS and convert it to a lower level that is tailored for each SoC block. They provide a fixed output voltage free from noise with high Power-Supply Rejection (PSR) [2], which is critical for sensitive analog circuits such as ADCs, oscillators, amplifiers, filters, and mixers. However, with noise-tolerant CMOS digital loads, PSR may be sacrificed to obtain a lower LDO input to output voltage for higher efficiency, especially at low input voltages [3]. The Digital Low-Dropout (DLDO) regulator [4] is designed with this in mind. DLDOs need to be internally stabilized for compact on-chip applications, so their internal integrating counter, as discussed further below, sets the loop's dominant pole. Compared to analog LDOs [2,5] or analog-digital hybrid LDOs [6–8], a DLDO has a lower input-to-output voltage difference, improving efficiency as well as lowering the output resistance. Consequently, with lower output resistance, the non-dominant output pole shifts to higher frequencies, improving stability with less area than an output-stabilized LDO. Another feature is that its quiescent power consumption is proportional to the frequency of its clock, making efficiency control straightforward.

Figure 1 shows a typical application. In an SoC with several tens of cores [7,9] or in data center applications, with each core requiring a separate supply, an analog LDO is not easy to integrate since a separate off-chip output capacitor is required to stabilize each LDO, making board routing impractical. A hybrid LDO is not applicable either since it requires a large silicon area to integrate both analog and digital control loops, making it hard to place

near the load. In conclusion, simple DLDOs are better-suited on-chip as they do not need additional loops or capacitors.

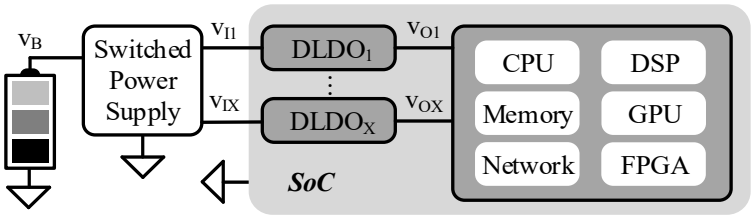

Figure 1. Multi-CPU system with Digital LDOs.

Sections 2–4 explore the features and frequency response of DLDO blocks. The analysis provided here makes it easier to design and validate DLDO systems when compared to the incomplete and difficult-to-follow explanations in the state-of-the-art since it discusses the parasitic effects in a baseline DLDO, which can later be applied to more complex systems. A DLDO's oscillatory behavior is analyzed in Section 5, and a novel technique is introduced, using an error subtracting counter. With this proposed technique, the addition of a simple digital circuit enables designers to exponentially increase the response time of the prior all-digital compact DLDOs [10] without compromising on stability. This is irrespective of the locations of parasitic poles and zeros in the system, which makes the design all-stable. The higher response speed may be traded for higher DC regulation accuracy. Additionally, PSR has typically been poor in prior DLDOs due to the lower output resistance. The proposed circuit also qualitatively improves the PSR of DLDOs at lower frequencies as an added bonus, and this is discussed in Section 6, followed by conclusions.

2. Digital LDO

The application considered supplies a load with an output voltage v_O from 0.5 to 1.1 V and load current i_{LD} ranging from 1 to 50 mA. The input voltage v_I from an SMPS (or battery) may vary between 0.6 and 1.2 V. The on-chip output capacitor C_O is chosen to be 100 pF (for transient response purposes only). A 1 MHz system clock is used to align with the bandwidth of typical analog LDOs. Neglecting LDO internal power consumption, worst-case efficiency works out to 42% at maximum input-to-output voltage.

Most prior works specify operation at a partial or narrow load current, input voltage, or output voltage ranges. As a result, the power device, which is made up of an array of segments, is within manageable ranges—up to a few hundred devices in parallel. However, in practical scenarios, an LDO must operate at larger load current ranges over the entire input voltage range. This is the first work to show such a system, which brings forward an issue in the basic DLDO architecture—the power device array becomes very large; with thousands of devices needed for the above-mentioned modest voltage and current range. With such a large array needed for full resolution, response time is extremely slow, requiring GHz speed clocks for reasonable performance, thus increasing power consumption beyond practical values. The technique presented in this work alleviates this trade-off to bring DLDOs into the realm of practicality.

2.1. Operation

A generic DLDO is depicted in Figure 2. The power pass device is an array of equal-sized (linearly weighted) pMOS transistors M_{PO} used as switches in triode. It is controlled by a feedback loop that sets the output voltage v_O by turning devices on or off. The loop consists of the load, the output capacitor C_O, feedback resistor divider $R_{FB1,2}$, comparator CP_E, a counter CNTR [10], and decoder logic DEC, followed by an inverting driver DRV driving M_{PO}. A reference voltage v_R and a clock f_{CLK} are also needed.

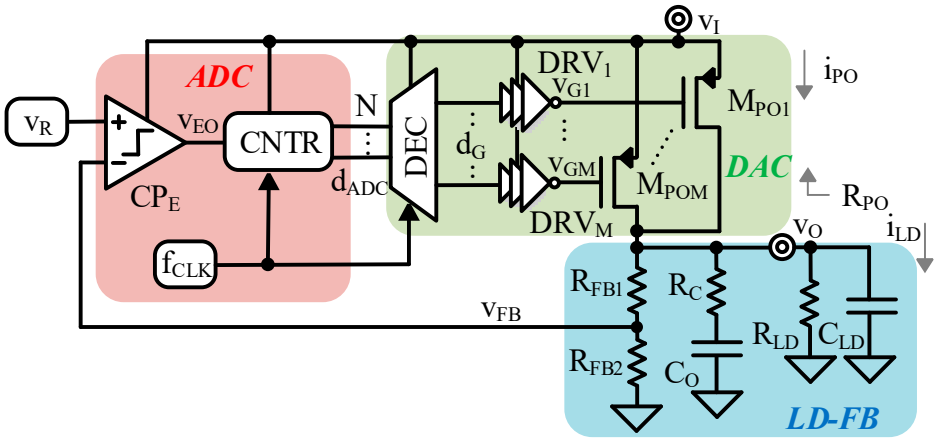

Figure 2. Digital LDO Composition.

The feedback loop sets v_O as follows: If v_O falls below the desired target, say due to a load disturbance, the feedback voltage v_{FB} becomes lower than the reference voltage v_R. The comparator detects this and sets the error output v_{EO} high (or 1). The counter responds by increasing the stored binary digital word d_{ADC} by 1, the Least Significant Bit (LSB). The decoder translates this word to a proportional number of turned-on power devices using logic gates, which goes up by 1 as well. Each pMOS device has a triode channel on-resistance when used as a switch [11]. Here, v_{SG} is source-gate voltage, v_{SD} is source-drain voltage, v_{TP} is threshold voltage, K_P' is transconductance parameter, and W/L is aspect ratio:

$$R_{LSB} = \frac{1}{K_P'\left(\frac{W}{L}\right)\left(v_{SG} + v_{TP} - \frac{v_{SD}}{2}\right)} = \frac{1}{K_P'\left(\frac{W}{L}\right)\left(\frac{v_I + v_O}{2} + v_{TP}\right)} \quad (1)$$

By activating one additional parallel power device, total pass device current i_{PO} increases by one LSB value i_{LSB}:

$$i_{LSB} = \frac{v_{SD}}{R_{LSB}} = \frac{v_I - v_O}{R_{LSB}}, \quad (2)$$

effectively reducing resistance R_{PO} in the power delivery path:

$$R_{PO} = \frac{R_{LSB}}{d_{ADC}}. \quad (3)$$

The extra current raises both v_O and v_{FB}. This process occurs once every clock cycle and continues until v_{FB} matches v_R and power device current i_{PO} matches load current i_{LD}:

$$i_{PO} = d_{ADC} i_{LSB}. \quad (4)$$

The feedback resistors set the ratio β_{FB} between v_O and v_{FB}, enabling the choice of v_O to be independent of the typically fixed v_R:

$$\beta_{FB} = \frac{v_{FB}}{v_O} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \approx \frac{v_R}{v_O}. \quad (5)$$

A similar process occurs when v_O exceeds the target. v_{FB} is above v_R, so the counter counts down to turn off power devices to lower i_{PO} and bring v_O back into regulation. Note that i_{LSB} is chosen based on minimum load current i_{LD} at maximum input-to-output voltage difference, which sets a single LSB power device switch's resistance R_{LSB}. To prevent metastability errors in this scheme, it is advisable to trigger the counter after the comparator makes its decision. For instance, after half a clock cycle for clocked comparators [12,13].

Note that process-voltage-temperature (PVT) variations do not significantly affect the simple system in Figure 2 since the control is implemented synchronously. The clock is generated by a feedback system such as a phase-locked loop, and the controller is in the digital domain with large margins. The power device array M_{PO} is the only section with PVT sensitivities via process variations in transconductance parameter K_P', aspect ratio (W/L), and threshold voltage v_{TP}, since these directly affect output resistance, output pole, DAC gain/phase, and unity gain-bandwidth frequency (f_{0dB}), as explained further below. This sensitivity is minimized by having a unit (equally) weighted M_{PO} to improve DAC linearity, ensuring robust PVT performance when compared to analog and hybrid LDOs.

2.2. Loop Model

A DLDO in the simplest form is shown in Figure 3. It consists of an ADC, a DAC, and loaded feedback (LD-FB). The ADC, driven by a clock, compares v_R and v_{FB} to output a proportional digital word d_{ADC}. The ADC considered here is made up of a comparator and a binary counter. However, alternative architectures exist, such as a flash ADC [14], which needs higher power and area; a Successive-Approximation Register (SAR) ADC [15,16], requiring high power for a low offset comparator and large capacitive DAC; a delay-based ADC [17], which is susceptible to PVT variations causing instability; or a sub-ranging ADC, which is harder to design, and hence these are not considered here. Additionally, the comparator CP_E may operate in continuous time, which needs higher power, or be clocked, having lower gain and higher kickback noise, but is preferred for low power.

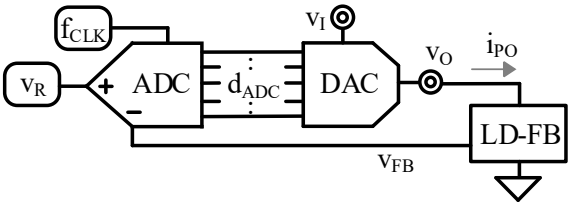

Figure 3. Loop model showing functional blocks of a DLDO.

The DAC outputs a current proportional to ADC output word, or d_{ADC}. Within the DAC, the decoder converts d_{ADC} into a thermometer code d_G for the gate driver (a string of 0s and 1s with the number of 1s equal to the binary value), and the driver controls the large power device array M_{PO}. M_{PO} may be in a linearly or exponentially (e.g., W/L size in powers of 2) weighted array [4], with pMOSs biased in the triode region (low v_I to v_O difference) for efficiency. Linear (equal) weighting is preferred as opposed to binary [18] to avoid DAC non-linearity (manufacturing mismatches causing missing codes) and MSB transition spikes. However, this does complicate the decoder and driver, which need significant area and may become a bottleneck to reducing area. Note that if v_O is lower than M_{PO}'s threshold voltage v_{TP}, M_{PO} turns on in saturation, pulling output pole lower in frequency.

The loaded feedback block includes the load and the feedback. It receives the DAC current i_{PO} to generate a voltage v_{FB} for the ADC. The load is modeled here in Figure 2 as a combination of resistance R_{LD} (often in parallel with a current source), the output capacitor C_O with its Equivalent Series Resistance (ESR) R_C, a bypass load capacitor C_{LD}, and the feedback divider resistors R_{FB1} and R_{FB2}. The control signal traversing through the feedback loop experiences a loop gain A_{LG}, defined as the product of the gains of the ADC, DAC, and LD-FB blocks, denoted by A_{ADC}, $A_{DAC,}$ and Z_{FB}, respectively:

$$A_{LG} = A_{ADC} \times A_{DAC} \times Z_{FB}. \quad (6)$$

Loop gain is analyzed and verified in the following sub-sections through simulation using a replica loop to bias the loop broken for testing [19], and then the frequency response of these sub-blocks is analyzed [5].

All following analyses rely on SPICE for low ADC count models and shift to Verilog-A models for higher count to simplify simulations. Specifically, the comparator, counter, and decoder are modeled with behavioral SPICE blocks such as sampler, delay, counter, and behavioral voltage functions, and the rest are implemented with circuit-level models. The behavioral sources are then translated to Verilog-A code to enable scaling to a higher ADC full-scale count. This can then be easily fed to a synthesis tool in the implementation phase.

Digital systems are usually analyzed in discrete-time (z-domain). However, for mixed-signal feedback systems such as the Digital LDO, it is advantageous to analyze in continuous-time (s-domain) due to the following reasons:

1. Z-domain analysis masks effects beyond clock frequency, which might hide effects that show up when the clock is varied in DVFS;
2. There already exists a multitude of prior art techniques outlining ways to improve system stability that use s-domain analysis that may be easily leveraged by a designer when compared to the more arcane z-domain analysis;
3. S-domain analysis is more intuitive since it directly relates to component-level effects from resistors, capacitors, etc. that are easily converted to ohmic translations to avoid solving non-intuitive difference equations;
4. Z-domain analysis assumes a zero-order-hold approximation for DACs, with voltages and currents assumed to be fixed in between clock cycles, so this cannot be extended to slow clock systems or for power supply ripple analysis.

For these reasons, this paper takes the s-domain approach, which has not been presented for Digital LDOs in prior art.

2.3. Loaded Feedback Translation

The low-frequency LD-FB gain is a function of LDO output resistance R_O and β_{FB}. The '0' in the gain subscript refers to low-frequency gain:

$$Z_{FB0} = R_O\beta_{FB} = [R_{PO} \,||\, (R_{FB1} + R_{FB2}) \,||\, R_{LD}]\, \beta_{FB}. \tag{7}$$

R_O depends on M_{PO}'s resistance R_{PO}, the load resistance R_{LD}, and the feedback resistors R_{FB1} and R_{FB2}. The output capacitor C_O provides charge on demand to the load until the feedback loop can respond to v_O changes, helping with LDO transient response. Typically, C_O is selected to minimize the v_O droop within a specified time at the worst-case load current step. C_O and R_O form an output pole p_O (C_O trades response speed with phase margin):

$$p_O \approx \frac{1}{2\pi[R_{PO} \,||\, (R_{FB1} + R_{FB2}) \,||\, R_{LD}](C_O + C_{LD})} \approx \frac{1}{2\pi R_O C_O}. \tag{8}$$

The pole introduces a phase delay $\angle Z_{FB}$ and lowers the magnitude of loaded feedback's gain $|Z_{FB}|$. Below the output pole frequency p_O, the gain $|Z_{FB}|$ changes little. At p_O, it experiences a 3 dB reduction, and beyond p_O, it decreases by 20 dB per decade ($10\times$) increase in frequency. Loaded feedback's phase delay $\angle Z_{FB}$ follows an inverse tangent function and corresponds to a 45° additional delay at p_O and up to a 90° delay at much higher operating frequencies f_O. Notably, p_O varies with power device resistance R_{PO} and consequently with i_{PO} and the ADC count d_{ADC}.

A large on-chip C_O brings a large ESR R_C. This ESR limits C_O's drop in impedance at higher frequencies, creating a zero z_C. This is typically at a frequency higher than p_O [20]:

$$z_C = \frac{1}{2\pi R_C C_O}. \tag{9}$$

At these frequencies, z_C cancels the effects of gain drop and delay from p_O. A bypass load capacitor C_{LD} may be intentionally added [5] to reduce the transient droop in v_O caused by R_C, which adds a load pole to the system. The capacitance associated with the

load may also be modeled within this pole. If neither is present, as is assumed here, the capacitance is dominated by the parasitic drain-body capacitance of the power device M_{PO} and varies with the count d_{ADC}, as in the frequency response of Figure 4.

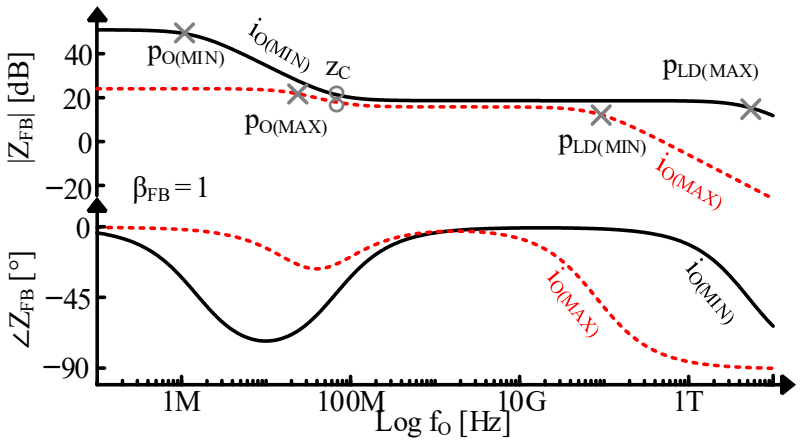

Figure 4. Simulated frequency response of the loaded feedback block LD-FB.

C_{LD} reduces the output impedance beyond the load pole p_{LD}:

$$p_{LD} \approx \frac{1}{2\pi R_C C_{LD}}. \tag{10}$$

In any LDO, output pole p_O exhibits significant variation with i_{PO} and load current i_{LD}. In a DLDO, it is additionally dependent on input voltage v_I through power device LSB resistance, and this effect is missed by most DLDO designers. Output resistance R_O also varies with v_I since DLDO power device resistance R_{PO} is low and comparable to load resistance R_{LD}. These dependencies are depicted in Figure 5 and must be accounted for while designing the power device LSB size and M, the full-scale ADC count (total number of power device sections).

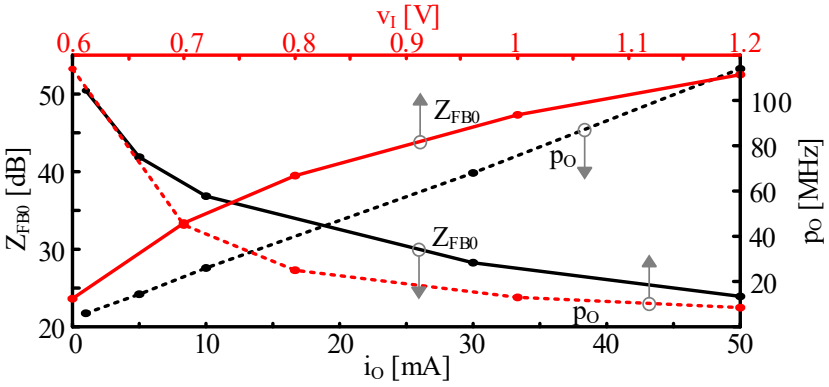

Figure 5. Changes in feedback with output current and input voltage.

3. ADC Response

3.1. Flash ADC

Sampling effects are illustrated with the simplest ADC, the flash. It converts an analog voltage to an equivalent digital code instantaneously, using an array of 2^N comparators. Each comparator has one LSB difference in their references, and together they produce a thermometer code at the output. Error voltage v_E is the difference in the ADC's inputs v_R and v_{FB}:

$$v_E = v_R - v_{FB}. \tag{11}$$

Sampling period t_{CLK} and 'N' quantization levels set the ADC's accuracy. For fast analog signals at frequencies close to sampling clock f_{CLK}, non-idealities of the ADC start to show.

Depending on the sampling instant, the digital word's equivalent analog amplitude may be a few to several percentage points lower than the analog signal, as seen in Figure 6, and consequently, the ADC gain is less than the ideal value. ADC gain [5] in Equation (12) is expressed in LSB/V, where A_E is the comparator's gain, v_{DD} and v_{SS} are the supply rail voltages, and $\Delta v_{ID(MIN)}$ is the minimum input difference needed for a deterministic 0 to 1 (or 1 to 0) comparator output transition:

$$A_{ADC0} = \frac{d_{ADC}}{\Delta v_{ID(LSB)}} = d_{ADC}\left(\frac{A_E}{v_{DD} - v_{SS}}\right) = d_{ADC}\left(\frac{A_E}{v_I}\right)\left[\frac{LSB}{V}\right]. \quad (12)$$

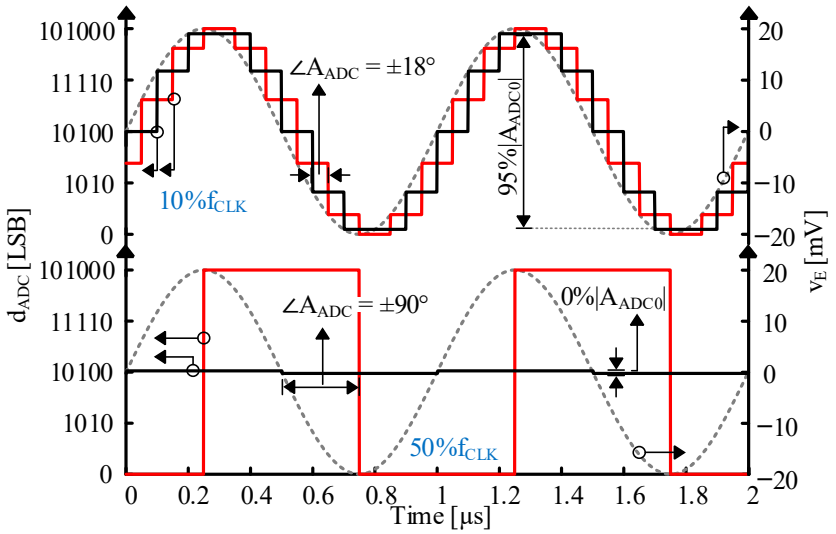

Figure 6. Simulation of sampling close to clock frequency.

A comparator's gain is often assumed to change with input for small signals; this understanding is tied to an ideal comparator. A real comparator's gain is defined by its offset—a larger offset implies lower gain; as seen in Equation (12). Any input smaller than the offset causing a comparator transition is a random metastability event and hence does not contribute to actual signal gain. On the other hand, an input larger than the offset will result in a proportionally larger number of 1s at the output v_{EO}, translating to a larger gain.

Next, the sample and hold effect from a non-zero period t_{CLK} introduces a delay between the analog signal and the digital word. The ADC's gain is a statistical function of the sampling instant's location, i.e., the relative phase between the f_{CLK} and f_O. For instance, when the input signal frequency is at 10% of f_{CLK}, there can be up to a 5% drop in ADC gain (Figure 6, black trace, upper plot), and the delay can be up to 18° depending on the first sample location. This could worsen to a 100% gain reduction (Figure 6, black trace, lower plot) when the input frequency is at $f_{CLK}/2$ and a delay of up to 90°.

The worst-case must be accounted for in design, with delay $\angle A_{ADC}$ being:

$$\angle A_{ADC} = \pm\left(\frac{360^\circ}{2}\right)\left(\frac{f_O}{f_{CLK}}\right) = \pm\frac{\pi f_O}{f_{CLK}} = \pm(180^\circ)\left(\frac{f_O}{f_{CLK}}\right), \quad (13)$$

and corresponding worst-case drop in ADC gain $|A_{ADC}|$ is:

$$|A_{ADC}| = k_S A_{ADC0} = \mathrm{Sin}(90^\circ + \angle A_{ADC})\, A_{ADC0}, \quad (14)$$

and their combined effect is modeled as a sampling pole p_S. Here, k_S is the gain drop factor. Although this worst-case delay cannot be precisely modeled as an analog pole, sampling

pole p_S is assumed for consistency to be the frequency at which the 18° delay at $f_{CLK}/10$ extrapolates to 45° in the analog pole inverse tangent function:

$$\angle A_{10\%} \equiv -\mathrm{Tan}^{-1}\left(\frac{10\% f_{CLK}}{p_S}\right) = \mathrm{Min}\angle A_{ADC(10\%)} = -18^\circ. \quad (15)$$

Here, $\angle A_{10\%}$ is the worst-case delay at 10% f_{CLK}, and $\angle A_{ADC(10\%)}$ is the ADC phase delay at 10% f_{CLK}. Consequently, sampling pole p_S comes out to be 31% of f_{CLK}:

$$p_S = 31\% f_{CLK}. \quad (16)$$

Prior art does not consider the effect of this pole, which is the main cause for stability issues and needing to overcompensate systems. This concept is applied to DLDOs for the first time and is discussed further in the sub-clock oscillation sub-section. However, note that the gain and phase response curves drop at a much higher rate than with an analog pole, and this approximation is optimistic.

3.2. Timed ADC for Higher Resolution

A single comparator serves as a 1-bit ADC. While this can simplify design, it comes at the cost of increased quantization error. To enhance resolution with minimal additional power, an alternative approach leverages time and accumulation: If an ADC slower than the flash is acceptable, a comparator with a counter can be considered. Comparator output v_{EO} can be summed up (integrated) by feeding it to a counter with an arbitrarily large full-scale count d_{FS}, as shown in Figure 2. d_{ADC}'s full-scale value d_{FS} is much higher than a comparator's full scale of 1, and thus ADC resolution improves, albeit at the cost of speed.

Additionally, pragmatic area and delay limits set how large full-scale d_{FS} can be. With a limited value, the counter may finish counting all the way up to d_{FS} within the positive half cycle of slow analog signals as in Figure 7 (top plot). As input frequency goes up, it is only able to count to a fraction of d_{FS} (bottom plot) in the positive cycle, resulting in lower output amplitude and lower ADC gain. Additionally, the counter introduces a longer delay at higher input frequencies since the clock period t_{CLK} is a bigger fraction of input period. The gain reduction and delay are modeled as a counter-pole p_C [16]. Like the sampling pole p_S, the phase delay is only approximately like an analog pole, and the gain drops only at frequencies beyond 1.6 times the counter-pole p_C, at which point the delay added is about 55°.

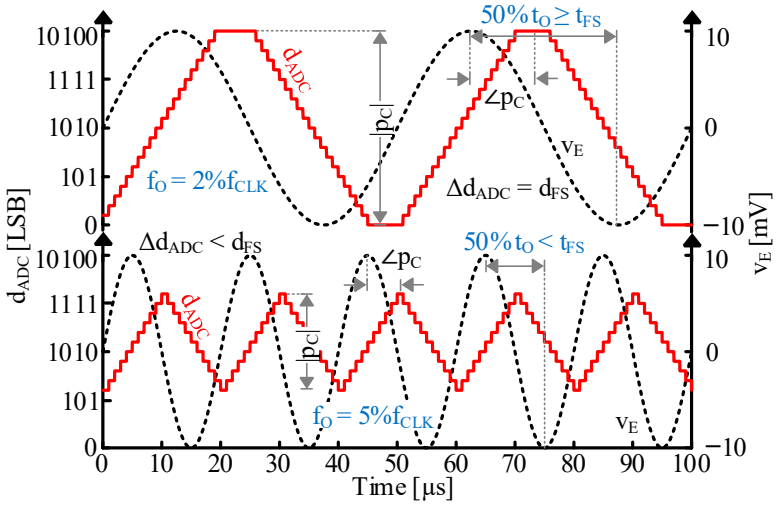

Figure 7. Simulation of counter-pole reducing gain and phase.

An analog pole response (dotted gray plot) is fit to match the response with p_C (red plot) in Figure 8. The counter has a linear response $\Delta v_{E(L)}$, taking t_R time to respond to the peak error voltage $\Delta v_{E(MAX)}$:

$$\Delta v_{E(L)} = \Delta v_{E(MAX)} \left(\frac{t}{t_R} \right). \tag{17}$$

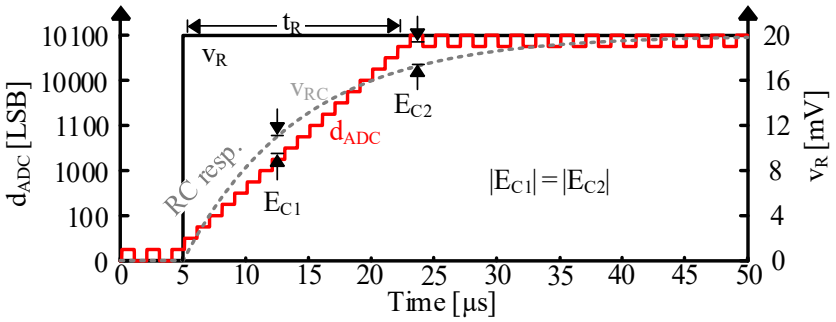

Figure 8. Simulated equivalent RC response of counter-pole.

The equivalent fit RC analog pole response $\Delta v_{E(RC)}$ is a decaying-exponential rise and is modeled with a time constant τ_{RC}:

$$\Delta v_{E(RC)} = \Delta v_{E(MAX)} \left(1 - e^{-t/\tau_{RC}} \right), \tag{18}$$

resulting in a pole modeling error E_C:

$$E_C = \Delta v_{E(RC)} - \Delta v_{E(L)}. \tag{19}$$

For best fit, error E_C is minimized when τ_{RC} is about 52% of t_R:

$$\text{Min } E_C = E_C \Big|_{\tau_{RC} = 52\% t_R}. \tag{20}$$

Thus, the counter-pole p_C depends on f_{CLK} and the change in count d_{ADC} (which is the full-scale value d_{FS} at low frequency):

$$p_C = \frac{1}{2\pi\tau_{RC}} \approx \frac{1}{2\pi(52\% t_R)} \approx \frac{f_{CLK}}{\pi d_{ADC}}. \tag{21}$$

Prior art approximates the location of this pole at 0 Hz with the z-domain approach [16]. The more accurate model presented here helps better understand the sensitivities of this pole to manage its effects on stability, as will be seen in the next section.

In summary, the ADC has two poles, counter-pole p_C, and sampling pole p_S. Its frequency response is depicted in Figure 9. The dotted green and blue lines are best-case and worst-case phase values, respectively, and the data points in between illustrate the effect of unpredictable phase between f_{CLK} and input frequency across different cycles of v_O. The shaded red region represents the possible gain variation. Some designs employ clocks that adapt to error voltage v_E but require high-resolution ADCs and complicate stability analysis due to randomness in p_S [21,22].

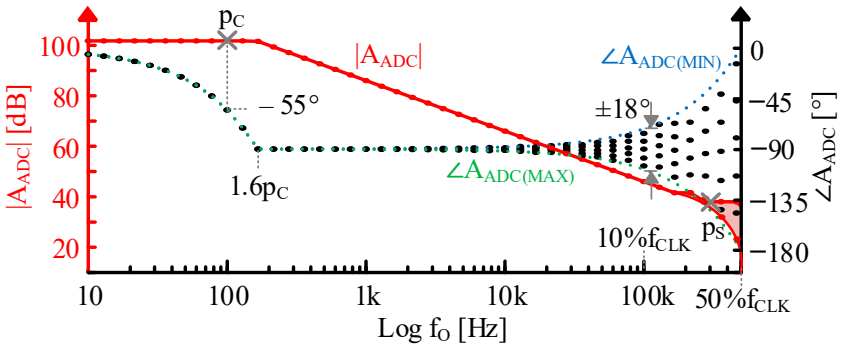

Figure 9. Simulated ADC open-loop frequency response.

4. DAC Response

4.1. Low-Frequency Gain

The DAC translates a counter output change to a corresponding power device current i_{PO} change in A/LSB, where $i_{PO(FS)}$ is full scale i_{PO} change:

$$A_{DAC0} \approx \frac{i_{PO(FS)}}{d_{FS}} = i_{LSB} \left[\frac{A}{LSB}\right]. \tag{22}$$

The count d_{ADC} is a binary word that is converted to thermometer gate driver code d_G in Figure 2. The number of 1s in d_G corresponds to the number of power devices M_{PO} turned on in triode when the driver pulls M_{PO}s gate voltage v_G down to 0 V. Conversely, the 0s indicate the number of turned off M_{PO}s, with the driver setting v_G to input voltage v_I, causing M_{PO} to be cutoff. Some designs additionally control M_{PO} body voltage [23] and rely on parallel feedback loops, which complicate design by requiring one loop to be much faster than the other over the entire f_{CLK} range in DVFS and are hence not considered here. Other designs [24] set v_G to values other than 0 and v_I, but doing so requires a complex analog loop and drivers, increasing power, delay, and area.

4.2. Frequency Response

The driver propagation delay t_P is modeled as a pole p_D:

$$p_D \approx \frac{1}{t_P} \gg \frac{1}{t_{CLK}} = f_{CLK}, \tag{23}$$

and must be contained well within a clock period for practical purposes. Typically, p_D is set at 10–100 times f_{CLK}. When choosing between pMOS and nMOS pass devices, the former is preferred since it does not require a charge-pump-based driver at low SoC-level voltages (which would introduce complexity, noise, and higher power) to generate high v_G. A unit pMOS pass device in triode exhibits inherent negative feedback through v_{SD} and gate-drain parasitic capacitance $C_{GD(LSB)}$ [25]. However, this same capacitance also creates a feed-forward path from v_G to v_O, resulting in a cross-switch zero z_X:

$$z_X = \frac{i_{LSB}}{2\pi C_{GD(LSB)}} = \frac{v_I - v_O}{2\pi R_{LSB} C_{GD(LSB)}} \gg f_{CLK}. \tag{24}$$

Note that i_{LSB} in the above equation has units in A/LSB, which is a transconductance. This out-of-phase (right-half-plane) zero z_X increases loop gain A_{LG} at frequencies above the zero and adds delay at the same time, degrading both phase (PM) and gain margin (GM) of the system, and it must be avoided for stability and noise (spikes in v_O at every clock edge). It is set to be much higher than f_{CLK}. Alternatively, a more involved approach to designing gate drivers [26] may be adapted to a pMOS pass device to convert this zero to an in-phase one. Since the zero depends on LSB power device current i_{LSB}, it is also sensitive

to input v_I. This is shown in Figure 10 in the DAC's frequency response. These effects are highlighted here to help designers keep these parasitic effects beyond loop bandwidth.

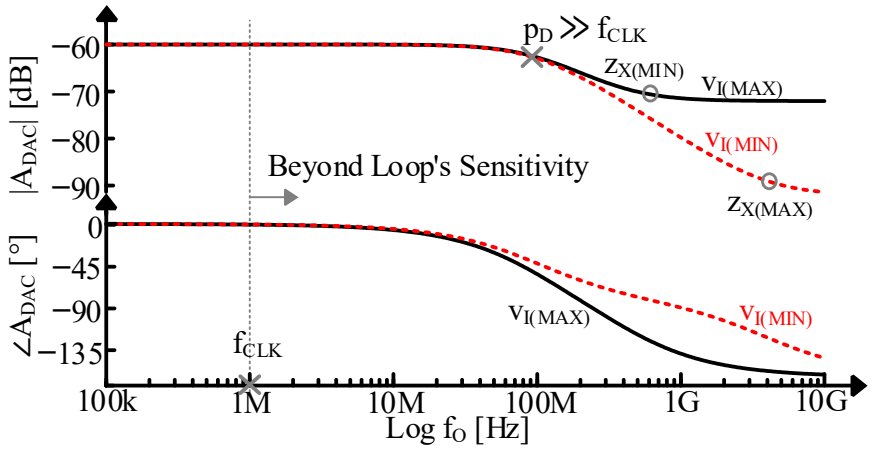

Figure 10. Simulated DAC open-loop frequency response.

5. Closed-Loop Operation

5.1. Oscillator

In Section 2, DLDO regulation is explained using negative feedback. However, DLDOs also exhibit positive feedback, leading to oscillations and instability. Positive feedback arises at specific frequencies from loop delays and unity gain feedback, i.e., when total delay across the loop reaches 360° and cycle-to-cycle gain is 1. To mitigate this issue, low-frequency loop gain A_{LG0} is set to a high value for low ripple error from this oscillation and hence higher accuracy:

$$A_{LG0} = A_{ADC0} \times A_{DAC0} \times Z_{FB0} = \frac{A_E \times i_{PO(FS)} \times Z_{FB0}}{v_I} \approx \frac{A_E \times v_O \times \beta_{FB}}{v_I} \approx \frac{A_E \times v_R}{v_I}. \quad (25)$$

The comparator exhibits a very high, but time-dependent gain $A_{E(MAX)}$ during its output v_{EO} transitions:

$$0 \leq A_E \leq A_{E(MAX)} \gg 1, \quad (26)$$

as also seen in Figure 11. However, between decisions or clock cycles, its gain is 0. As in Figure 12, when feedback voltage v_{FB} is close to the reference v_R in steady state and assuming comparator output v_{EO} was deterministically 1, the count d_{ADC} increments by 1 LSB, causing v_O to overshoot its target. As a result, in the next clock cycle the comparator outputs 0 and counter decrements by 1, pulling v_O below the target. This repetitive behavior in v_{EO} in closed-loop arising from finite ADC resolution is known as limit-cycling. This is the first work to show positive feedback as the cause of limit cycling, as explained in the following paragraph.

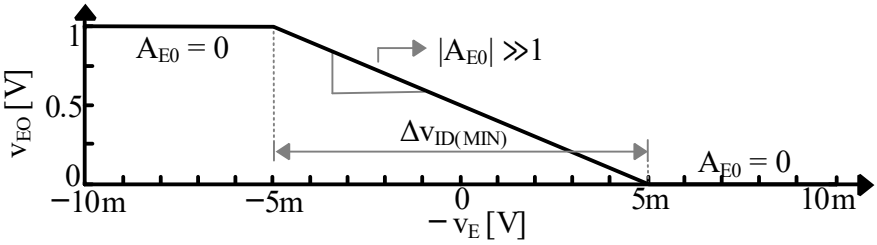

Figure 11. Simulated comparator gain at clock edge.

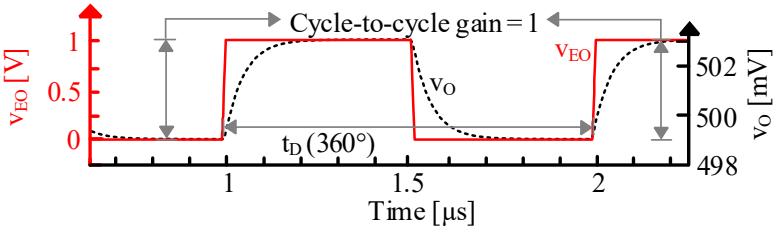

Figure 12. Simulation showing condition for oscillation.

The counter and sampling poles together introduce a 180° phase delay as seen in Figure 9 at the operating frequency of $f_{CLK}/2$, which adds with the 180° phase shift from negative feedback (due to an odd number of inversions from the comparator, driver, and M_{PO}) to produce a total of 360° loop phase delay $\angle A_{LG}$ at $f_{CLK}/2$:

$$\angle A_{LG}\Big|_{\frac{f_{CLK}}{2}} = 180^\circ + \angle A_{ADC} = 180^\circ - \left(\frac{t_D}{2t_{CLK}}\right)(360^\circ) = 0^\circ. \tag{27}$$

Here, t_D is the ADC delay and f_{OSC} the oscillation frequency, $f_{CLK}/2$. The comparator's limiting action resembles automatic gain control (AGC) and forces the loop gain to 1 at $f_{CLK}/2$:

$$A_{LG}\Big|_{\frac{f_{CLK}}{2} = f_{OSC}} = 1\angle 0^\circ = |A_{LG(OSC)}|\angle A_{LG(OSC)}, \tag{28}$$

as also seen in Figure 12. Here, 'OSC' in the gain subscript refers to gain at f_{OSC}. This applies only when all other delay sources in the loop are negligible and sum to a fraction of t_{CLK}:

$$t_D = t_{CLK} = \frac{t_{OSC}}{2} \gg \frac{1}{p_O} + \frac{1}{z_C} + \frac{1}{p_{LD}} + \frac{1}{p_D} + \frac{1}{z_X}. \tag{29}$$

Output voltage v_O's ripple Δv_O is then calculated as:

$$\Delta v_O = \Delta d_{ADC} A_{DAC} R_O = (1) i_{LSB} R_O \approx (v_I - v_O)\left(\frac{R_{PO}||R_{LD}}{R_{LSB}}\right). \tag{30}$$

5.2. Sub-Clock Oscillation

The next significant delay in the loop is output pole p_O. It exhibits considerable variation with load current i_{LD} and input voltage v_I. Due to its additional delay, the assumption in Equation (29) is not satisfied at certain operating points and p_O values, leading to the positive feedback oscillation condition in Equation (28) being met at a frequency f_{OSC}' that is less than $f_{CLK}/2$ and increasing phase delay $\angle A_{LG}'$:

$$\angle A_{LG}'\Big|_{f_{OSC}' = \frac{1}{2t_D'} < \frac{f_{CLK}}{2}} = 0^\circ. \tag{31}$$

This reduction in f_{OSC} to f_{OSC}' causes sub-clock oscillations, increasing the oscillation amplitude from Figure 12 to that seen in Figure 13 [13]. This is undesirable for a low-ripple supply (single prime in superscript refers to the same variables with sub-clock oscillations included). The counter cycles through multiple digital words d_{ADC}' even at steady state. A detailed mathematical modeling technique for these sub-clock oscillations is provided in [27]. However, this sub-section reviews the cause of sub-clock oscillations in the transient domain for a better understanding of how a fix was developed for it.

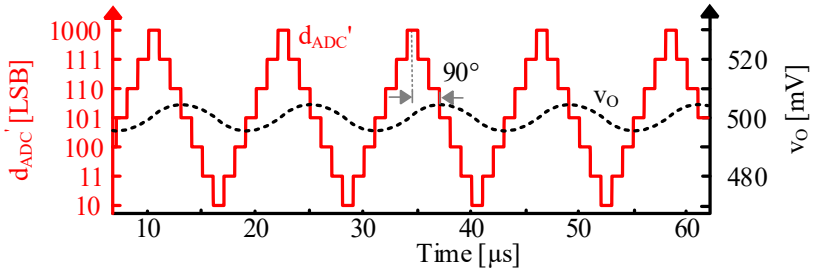

Figure 13. Simulated sub-clock oscillation.

When the counter counts up and reaches its ideal value for that operating condition $d_{ADC(i)}$ and if there is a low t_P delay across M_{PO}, the power device current i_{PO} also instantly reaches the optimal load current i_{LD}. However, the output pole's delay t_{PO} exceeds a single clock cycle, and the rise in v_O is unable to reach its optimal value $v_{O(i)}$ before the next clock cycle. Thus, the comparator still perceives v_O's translation, the feedback voltage v_{FB}, to be lower than the reference v_R and continues to drive the counter to increase count beyond $d_{ADC(i)}$. Depending on p_O's delay, the comparator finally notices v_{FB} reaching the reference a few clock cycles later, by which time the count is higher than $d_{ADC(i)}$ by a few LSBs.

At this point, the comparator finally outputs a 0, reducing the count by 1 LSB, but it remains above $d_{ADC(i)}$. Consequently, power device current i_{PO} decreases but remains greater than i_{LD}, causing output voltage v_O to charge up higher despite comparator output v_{EO} being 0. v_O overshoots further, causing comparator output v_{EO} to continue staying at 0. Eventually, the power device current i_{PO} drops enough to equal the load current i_{LD} when d_{ADC}' reaches $d_{ADC(i)}$, but v_O is still above $v_{O(i)}$ due to the previous overcharging, so v_{EO} remains at 0 despite reaching optimal count. At this point, the count drops below $d_{ADC(i)}$, and i_{PO} drops below i_{LD}, and by the time v_O drops to $v_{O(i)}$, d_{ADC}' is a few LSBs below $d_{ADC(i)}$. This process repeats, sustaining the oscillation, as summarized in Figure 14.

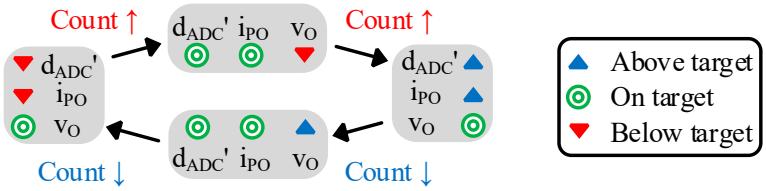

Figure 14. Cause for sub-clock oscillation.

Importantly, the count d_{ADC}' and output voltage v_O are 90° out of phase at f_{OSC}' due to the combined delay from f_{CLK} and output pole p_O. This adds to the 90° delay from the counter-pole p_C and 180° from negative feedback to produce a 360° loop delay. In this case, the counter acts as the AGC by counting the number of t_{CLK}s that fit within the loop delay t_{PO} (named so for the delay with lower p_O). The counter sets the loop gain to 1 at the frequency f_{OSC}' that corresponds to the integer value greater than the ratio of t_{PO} and t_{CLK} (represented here using the ceiling function), and the sub-clock oscillation period t_D' becomes:

$$t_D' = \left\lceil \frac{t_{PO}}{t_{CLK}} \right\rceil t_{CLK} = \frac{t_{OSC}'}{2} > t_{CLK}. \tag{32}$$

The counter ripple $\Delta d_{ADC}'$ is:

$$\Delta d_{ADC}' = \frac{0.5 f_{CLK}}{f_{OSC}'} = t_D' f_{CLK} = \left\lceil \frac{t_{PO}}{t_{CLK}} \right\rceil, \tag{33}$$

and translates to output voltage ripple $\Delta v_O'$:

$$\Delta v_O' = \Delta d_{ADC}' A_{DAC} R_O \approx \Delta d_{ADC}' i_{LSB} R_{PO} = (v_I - v_O)\left(\frac{\Delta d_{ADC}'}{d_{ADC}'}\right). \tag{34}$$

Alternately, this is inferred [13] as a higher ripple at a higher f_{CLK} to p_O ratio.

Further, the spectral content of v_O' and count d_{ADC}' is shown in Figure 15. Due to digital sampled control, harmonics of f_{OSC}' are expected. In the frequency domain, d_{ADC}' (red plot) has a tone at f_{OSC}' and its harmonics. Additionally, there are components of f_{CLK} and its harmonics/sub-harmonics that are lower in v_O (black plot) due to p_O. The effects of sampling and aliasing create these undesired spurs. At high f_{CLK}, the noise spectrum is akin to a ΔΣ modulator in an oversampling ADC due to integration [28].

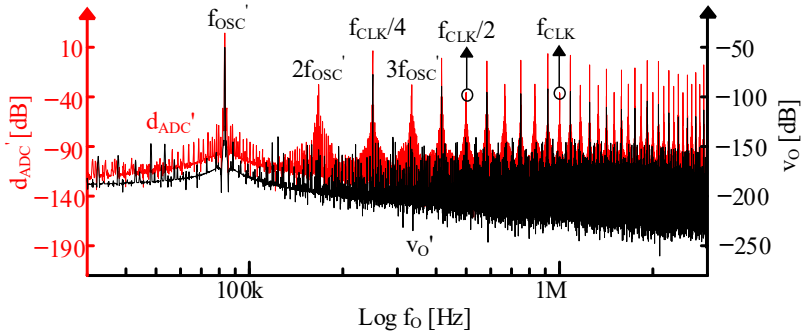

Figure 15. Frequency spectrum of sub-clock oscillation.

5.3. One-LSB Regulator

This sub-section highlights the operation of the proposed novel block. Typically, stability at higher frequencies is achieved with derivative control. The basic approach is to detect a high slope in v_O at steady-state and correct for it with a fast feedback loop [16]. For this application, though, the lack of high-speed, high-resolution ADCs limits slope detection accuracy. In the simple system of Figure 2, this may be carried out by applying a correction on the counter when a v_O excursion is detected, with a delay line-based slope detector sensing comparator output v_{EO}, but it lowers the counter-pole and reduces ADC gain and accuracy. A more elegant and robust solution is offered here.

The DLDO transforms into a one-LSB regulator with the addition of a digital block, the error-subtracting counter, that enforces oscillations at a one-LSB amplitude:

$$\Delta d_{ADC}'' \equiv 1, \tag{35}$$

and sets the oscillation frequency f_{OSC}'' back at $f_{CLK}/2$. With this, the system cancels the effects of all delays other than clock delay (double prime in superscript refers to variables in the one-LSB regulator).

The comparator output v_{EO} is a string of 1s for the positive half cycle input and 0s for the negative half and captures information on the oscillation period t_{OSC}''. By counting the number of 1s and 0s and multiplying by t_{CLK}, the t_{OSC}'' is readily obtained, which may then simply be deducted from the count with an error subtractor. Design-wise, the counter block in the original DLDO in Figure 2 is replaced by the error-subtracting counter system in Figure 16 below to make the DLDO a one-LSB regulator. The solution is adding an extra counter $CNTR_2$ (black section) alongside the original counter $CNTR_1$ (gray section).

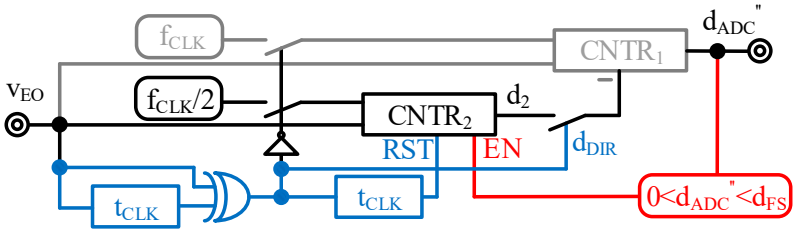

Figure 16. Error-subtracting counter.

$CNTR_2$ uses this information from v_{EO} to measure the length of the string of 1s (or 0s) and subtracts half of it from $CNTR_1$ upon reaching steady-state to cancel oscillation. This also eliminates ringing from overshoot or undershoot caused by load disturbance as an added benefit. An exclusive-OR (XOR) gate (blue section) takes v_{EO} values from the current and previous clock cycles (the t_{CLK} blocks in Figure 16 represent one clock-cycle delay). It outputs 0 if both its inputs are equal, implying an excursion from a steady state. Otherwise, it outputs 1 when current and previous states are unequal, indicative of having reached steady state v_O limit-cycling [29]. This signal d_{DIR} triggers oscillation cancellation and subsequently resets $CNTR_2$ and serves as a marker of the end of half of t_{OSC}″, just like a peak detector. An example is shown in Figure 17, where v_{EO} is 1 when the count increases and 0 when it reduces, and d_{DIR} is usually 0 but becomes 1 at the points marked in green when the count changes direction and triggers a subtraction.

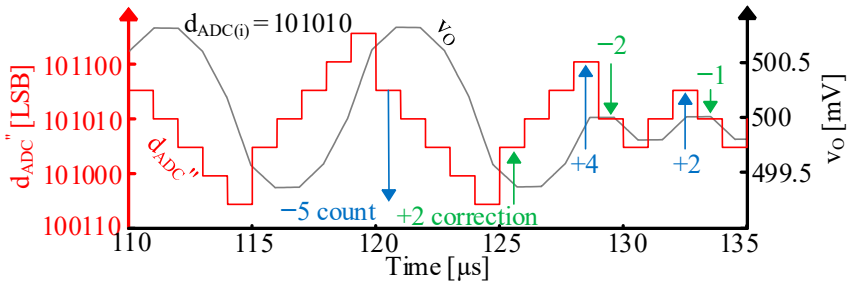

Figure 17. Simulation of constant delay being canceled.

In the p_O-induced v_O″ ringing in Figure 17, $CNTR_1$ counts up by 4, of which the first 2 LSBs bring it up to optimal count $d_{ADC(i)}$, while the subsequent 2 LSBs result from the 90° delay between power device current i_{PO} and v_O caused by output pole delay. These 2 extra LSBs represent the amplitude (half of 4) of the sub-clock oscillation and must be subtracted from the counter at the end of the string of 1s in v_{EO} to bring d_{ADC}″ back to $d_{ADC(i)}$. Unlike $CNTR_1$, $CNTR_2$ is made to count once every 2 clock cycles (at $f_{CLK}/2$) so its count d_2 goes up by half as much as $CNTR_1$. Assume this parallel count d_2 is 0 at the beginning of this string of 1s. While main count d_{ADC}″ goes up by 4 LSBs, parallel count d_2 goes up to 2 LSB, and this is subtracted from $CNTR_1$ at the point when the count d_{ADC}″ changes direction. As a result, d_{ADC}″ is set to its optimal value $d_{ADC(i)}$ at the exact same point when v_O is at its optimal value. This wards off p_O delays from sustaining any oscillations.

The XOR gate marks the end of 1s and triggers this subtraction. Also, parallel count d_2 is reset to 0 using the signal d_{DIR} at the next clock cycle to prepare for the next oscillation occurrence. It is essential to disable the counting on both $CNTR_1$ and $CNTR_2$ during the clock cycle when the subtraction occurs to prevent metastability errors. Next, in cases where delays occur infrequently, such as during load dumps, line steps, or noise spikes, these corrective actions must be taken only a few times. However, due to the constant delay introduced by the output pole p_O in the loop, this corrective action needs to be constantly taken every oscillation half cycle at those operating points. With the proposed solution, the designer can eliminate inevitable oscillations at low p_O that plagued prior art and restrict operating range to higher p_O or low f_{CLK} (slower response).

In summary, the error-subtracting counter plays a crucial role in mitigating transient or stability errors within the DLDO. Though based on a simple concept that is almost like auto-zeroing, it has a profound impact—its use can be extended to asynchronous DLDOs in [30–33]; that have lower stability; or further to other digitally controlled feedback systems to suppress ringing. The best way to compare LDOs in terms of response time is with the plot of the output voltage while reacting to a large load current transient (blue plot). Figure 18 illustrates this load dump response for both typical DLDO designs with two different phase margins (green and dotted red plots) and additionally shows the effect of the addition of the error-subtracting counter (black plot). The system with higher output capacitance C_O (green plot) experiences smaller undershoots since it can deliver

more charge in the same time window before the loop can respond. However, it exhibits sustained ringing due to lower p_O and PM compared to the system using a smaller C_O (dotted red plot), which has a more pronounced undershoot. This trade-off is released in the one-LSB regulator (black plot), and there is no ringing upon recovery from undershoot.

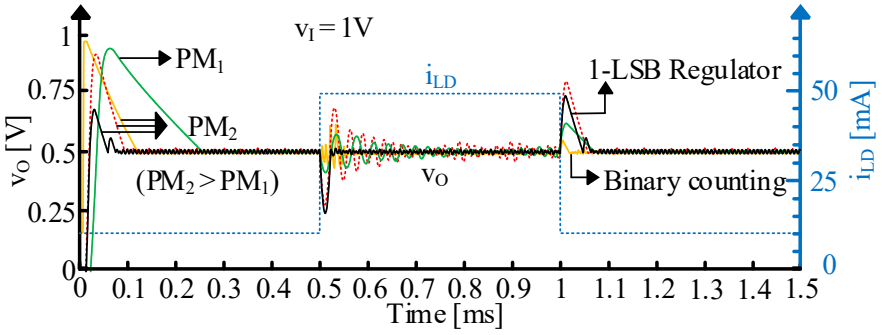

Figure 18. Simulated load dump response with 10 ns edge.

Thus, C_O can be increased arbitrarily (only limited by application area limits) without affecting stability. However, upon closer inspection, the black plot in Figure 18 shows slight ringing at startup and recovery from high to low i_{LD}. This is because under the two special cases of startup or counter "railing out" (reaching full-scale d_{FS}), parallel count d_2's value does not correspond to $t_{OSC}''/4$ (half of undershoot—quarter the cycle) since it has not stopped counting parallelly with $CNTR_1$. To address this, the error-subtracting counter is disabled under these two conditions by deactivating and resetting $CNTR_2$. The red section in Figure 16 illustrates this control path addition, where $CNTR_2$ is enabled only when d_{ADC}'' is not recovering from 0 (startup) or d_{FS} (railing out). This functionality is realized with a flip-flop that clears when the count is either 0 or d_{FS} and sets when the XOR output d_{DIR} is high the next time (upon reaching steady-state). This effectively gets rid of all ringing in the system. However, Figure 18 shows that startups are faster without this extra feature. Designers may choose to accept some ripple at startup for faster turn-on while retaining the disable feature for full-scale. In summary, steady-state one-LSB limit cycling provides a means to cancel sub-clock oscillations to improve stability and response time, which was limited in prior art due to the large power device array size.

To further improve speed and PSR, the concept of the one-LSB regulator is readily extended to a binary count scheme using the same idea of removing half the oscillation delay, as seen in the yellow plot in Figure 18. Since $CNTR_1$'s change in count now doubles every clock cycle, the other counter, also doubling, must return to the count corresponding to half the recovery time (instead of half the count) to correspond to the lowest point on the undershoot (or highest in the overshoot), i.e., at $t_{OSC}''/4$, when v_O has a slope of 0, which points to the instant when power device current i_{PO} matches load current i_{LD} demand. For example, if parallel count d_2 is 32 when XOR output d_{DIR} goes high, then the count to be subtracted should correspond to half of the time (and not half the value), which occurred when d_2 was 4 (instead of 16). The value subtracted should thus be $32 - 4 = 28$. For this, two parallel counters are employed, one operating at f_{CLK} for subtracting 32 and the other at $f_{CLK}/2$ to add 4. Note that only the counters are made exponential and not the power device weighting to maintain DAC linearity for steady-state accuracy.

The exponential counting generates a slightly higher ripple within the first clock cycle before it is cancelled by the error-subtracting counter, and that is more pronounced at low i_{PO} and low p_O values since loop gain A_{LG0} is high. Designers may choose to trade this additional ripple with speed while still being faster than a linear count system by considering other counting schemes such as exponential with power less than 2 [34] (or greater than 2 for even higher speeds, only limited by high clock power dissipation), recursive Fibonacci series, or interval search [29]. Note that with a binary counting scheme, LSB size can be further reduced to achieve higher accuracy at light load without significantly affecting response time, since delay is now a logarithmic function of array size. Future

work will focus on shifting between counting methods based on the loop delay measured by the parallel counter via d_2.

6. Output Regulation

Negative feedback plays a crucial role in regulating the output voltage of a DLDO for its load. It helps set output voltage V_O:

$$V_O = V_R A_{CL0} = V_R \left(\frac{A_{ADC} A_{DAC} R_O}{1 + A_{LG0}} \right) \approx \frac{V_R}{\beta_{FB}}. \quad (36)$$

Uppercase is used for low-frequency values of variables defined earlier. A high comparator gain in Equation (25) maintains the low-frequency closed loop gain A_{CL0} close to $1/\beta_{FB}$. A higher loop gain A_{LG0} results in a smaller error between A_{CL0} and $1/\beta_{FB}$, leading to lower steady-state error and higher accuracy. At steady state, an LDO is characterized by line regulation (effect of input v_I changing on v_O accuracy) and load regulation (effect of output resistance change on v_O accuracy). Negative feedback is effective in DLDOs only at lower frequencies. At higher frequencies, positive feedback dominates and disrupts operation under specific conditions. Therefore, it is proposed to use the error-subtracting counter for good regulation.

6.1. Power-Supply Rejection

PSR and line regulation are critical functions of an LDO. The ability to maintain a fixed v_O despite v_I variations determines the quality of a power supply. A higher PSR translates to a lower gain from input to output. In a DLDO, the power device M_{PO} operates as a switch. Hence, the fraction of v_I's AC ripple showing up in v_O depends on the resistor divider formed by power device resistance R_{PO} and loaded feedback resistance $R_{LD} \mid\mid R_{FB}$. Since M_{PO} is in triode, R_{PO} is quite small, allowing a significant portion of v_I ripple to pass through to v_O, yielding high supply gain or low PSR.

Most designers ignore PSR, with the assumption that CMOS loads can tolerate any ripple. However, ripple eats into noise margins, requiring stronger logic drive and more power. Additionally, the dynamic nature of CMOS loads causes sudden undershoots in output v_O as blocks turn on from sleep mode that combine with input ripple to adversely affect performance by causing unintended resets, metastability-related timing errors, and memory corruption. This is typically managed by either setting a guard band period in the load after turn-on, by limiting larger undershoots as in Figure 18 with low output current range, or by using large output capacitors. However, this either slows down the system or the number of regulators increase and area increases. A DLDO offering some PSR at even low SoC-level voltages can accomplish the same task with no area or power overhead.

In a DLDO, however, sub-clock oscillations extend loop delay and further increase supply gain by increasing loop output resistance [5] with positive feedback. The one-LSB regulator extends negative feedback to higher operating frequencies and cancels any ripple or disturbance in the system at a frequency lower than $f_{CLK}/2$. Thus, even ripples injected from input to output are removed after a half-cycle, like in Figure 17. This improves PSR; however, it remains much lower than what analog LDOs achieve, where M_{PO} acts as a current source in saturation and presents a higher impedance to input [2].

Note that PSR improvement in the one-LSB regulator applies only in the small-signal context. With large signals, for instance, a sinusoidal input voltage with a high frequency or amplitude will still propagate to v_O if it exceeds the slew rate at which the counter can make M_{PO} turn on or off. Beyond this limit, large-signal variations in v_I cannot be rejected, resulting in a residue ripple in the count d_{ADC}''' given by $\Delta d_{ADC}'''$ (triple prime in superscript refers to variables with power supply ripple considered):

$$\Delta d_{ADC}''' = \left\lceil \frac{\partial v_I / \partial t}{\Delta v_O / t_{CLK}} \right\rceil_{MAX} = \left\lceil \frac{\partial (0.5 \Delta v_I \sin 2\pi f_I t) / \partial t}{\Delta v_O / t_{CLK}} \right\rceil_{MAX} = \left\lceil \frac{\pi \Delta v_I f_I}{\Delta v_O f_{CLK}} \right\rceil, \quad (37)$$

and shown in Figure 19, it translates to a v_O''' variation $\Delta v_O'''$:

$$\Delta v_O''' = \Delta d_{ADC}''' A_{DAC0} R_O = \Delta d_{ADC}''' \Delta v_O = \left\lceil \frac{\pi \Delta v_I f_I}{f_{CLK}} \right\rceil \quad (38)$$

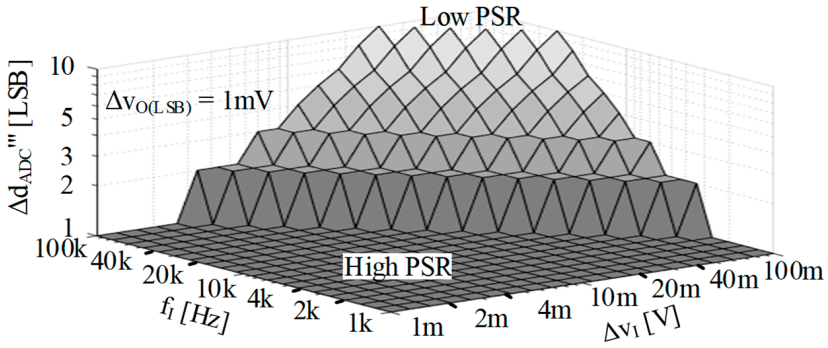

Figure 19. Simulated slew rate thresholds for PSR.

To ensure one-LSB regulation, the maximum slope in v_I, $\partial v_I/\partial t$, must not exceed the maximum slew rate of the LDO, $\Delta v_O f_{CLK}$. In other words, if the input voltage is expected to have slewing larger than this, f_{CLK} may need to be increased or a DLDO may not fit the PSR needs of that application. Here, Δv_I is v_I's ripple amplitude, and f_I is the input voltage ripple frequency.

6.2. Design

To achieve good regulation at the operating frequency of interest, negative feedback must dominate over positive feedback. Traditional analog techniques that enhance loop stability can also be extended to DLDOs. For instance, adding a bypass capacitor across R_{FB1} introduces an in-phase zero to the loop, preserving gain and phase that might otherwise be lost to other poles. Bypassing the DAC with a feed-forward capacitor or creating an in-phase zero within the ADC in the digital domain will have a similar effect.

Finally, DLDOs offer an advantage in terms of efficiency control. When CMOS loads enter sleep mode, they typically lower f_{CLK} and reduce their current i_{LD}. At lower i_{LD}, DLDO loop gain increases, and p_O drops in frequency, reducing PM, making it preferable to operate at a lower bandwidth with a lower clock for lower sub-clock oscillation amplitude. Coincidentally, the load's clock is also decreased and can directly (or a fractional frequency derivative) be used with the DLDO when operating in DVFS mode. This eliminates the need for a separate clock source for the DLDO and significantly reduces the latter term of the power loss P_{LOSS}, thus improving efficiency at low i_{LD}:

$$P_{LOSS} \approx i_Q v_I + f_{CLK} C_{G(EQ)} v_I^2. \quad (39)$$

Here, i_Q is the quiescent current used by the DLDO feedback control, and $C_{G(EQ)}$ is the equivalent capacitance that it presents to the input. Further loss reduction is obtained by clock-gating inactive sections of CNTR and decoder [13,30] to reduce the clock activity factor and $C_{G(EQ)}$, which is typically the bottleneck in these designs.

7. Conclusions

This paper proposes digital LDOs for highly integrated applications that operate over wide current and voltage ranges to drive CMOS SoC blocks. A simple model is presented to analyze any DLDO. The shortcomings in stability analyses in prior art are bridged with new and more accurate models of feedback effects such as counter-pole, sampling pole, and loop gain response. Intuitive guidelines are provided to keep parasitic effects from affecting the system. Further, the oscillatory behavior of DLDOs is explained. A novel block, the error-subtracting counter, is proposed to enforce one-LSB regulation that

can make the system all-stable while exponentially improving response time, reducing output noise, and improving PSR of DLDOs by canceling all undesired oscillations in the output voltage. With a simple addition to the control scheme, any prior-art DLDO can be made exponentially faster while maintaining low design complexity with low power and low area to fit the solution on-chip. Additionally, based on the need, the designer may choose a smaller LSB power device to improve DC regulation accuracy by trading with speed. Finally, well-known techniques are reviewed that help with system-level design for improving stability. Higher speed requires higher operating power. A few counting schemes are outlined for the counter-based integrator, aiding the designer to pick the one that suits the application the best. Additionally, DVFS may be employed to trade speed with efficiency. Future work will explore how the system may adaptively switch between counting schemes for even faster response or lower power and will also look at improving PSR at higher frequencies and slew rates.

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