Designing Compact & Efficient Switched-Capacitor DC–DC Converters

Xi Li, *Graduate Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Fellow, IEEE*
School of Electrical and Computer Engineering, *Georgia Institute of Technology*, Atlanta, GA, U.S.A.
xli832@gatech.edu and rincon-mora@gatech.edu

***Abstract*—Switched-capacitor DC–DC converters are widely used for fully integrated on-chip power supplies due to their high efficiency and compact footprint. Existing design approaches provide effective circuit analysis but limited guidance for systematic circuit-level design. This work presents a topology-independent design methodology based on a static ohmic-loss model and the boundary between full and partial transfer. By using the boundary as the design target, capacitance allocation, MOSFET sizing, and clock period are jointly optimized while ensuring simultaneous boundary operation of all flying capacitors. The resulting design flow is demonstrated on a telescoping-stage converter. Simulation results closely match theoretical predictions and confirm minimum-loss operation, providing a practical and systematic framework for SC converter design.**

***Index Terms*—Switched-capacitor dc–dc converters, charge pump, power supplies, boost, optimization, design, sizing, low-loss, capacitance allocation, clock frequency, low-power, on-chip.**

I. Compact & Efficient On-Chip Power Supplies

With rising demand for compact, low-power devices, system-on-chip solutions are increasingly used. Switched-capacitor (SC) converters outperform switched-inductor ones due to less nonideal on-chip capacitors and higher energy density [1], [2]. In Fig. 1, SC converters can harvest energy from batteries or transducers to power sensors, transmitters, and DSPs [3]–[25].

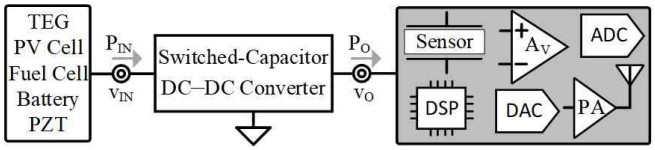

Fig. 1. Switched capacitor dc-dc converter for low power IoT systems.

Existing SC analyses have established transfer regimes and loss mechanisms [26]–[33]. Building on these analytical foundations, this work develops a topology-independent design methodology that uses the boundary as the design target to jointly determine capacitance allocation, clock period, and MOSFET sizing through closed-form equations. The resulting methodology provides a complete design flow rather than heuristic parameter selection.

This paper is organized as follows: Section II presents SC topologies. Section III shows the output resistance derivation. Section IV explores capacitance allocation. Section V discusses the clock:switch design of the SC converter, and Section VI provides a design example. Section VII concludes the paper.

II. Switched-Capacitor Power Supplies

Over the years, many SC topologies have been proposed for various applications. Existing literature typically classifies them based on operating principles rather than circuit structure. This work focuses on voltage-boosting topologies for IoT systems.

A. Single Stage

A single stage converter transfers energy from input to output in one step. All flying capacitors C_F are first charged in parallel, then connected in series to boost the voltage, as shown in Fig. 2, with no intermediate stages or cascaded redistribution.

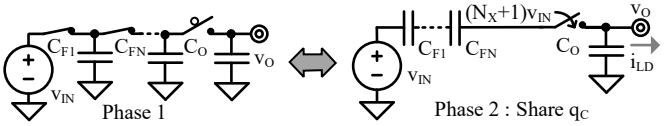

Fig. 2. Single stage (parallel–series) topology.

The nominal voltage boosting gain A_V depends on the number of C_F, N_X.

$$A_V \equiv \frac{v_O}{v_{IN}} = \frac{v_{O(S)}}{v_{IN}} = \frac{N_X v_{IN} + v_{IN}}{v_{IN}} = N_X + 1, \qquad (1)$$

where v_O and v_{IN} are the output voltage and input voltage respectively. The "+1" accounts for the v_{IN} itself. This corresponds to the ideal, unloaded voltage gain of the converter.

B. Multi-Stage

Multi-stage converters extend the single stage by dividing energy transfer into multiple sequential stages. Intermediate nodes incrementally boost the voltage to v_O, as shown in Fig. 3. Its A_V matches the single stage case for the same N_X.

$$v_{O(M)} = v_N + v_{IN} = N_X v_{IN} + v_{IN}. \qquad (2)$$

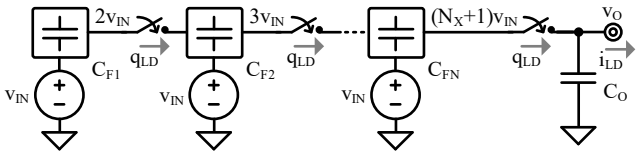

Fig. 3. Multi-stage topology.

C. Telescoping

Telescoping topology further extends the multi-stage approach, with sequential charge transfer through cascaded intermediate stages. This allows higher voltage gains with fewer C_F. For instance, the topology in Fig. 4 follows a Fibonacci-like pattern.

$$v_{O(T)} = v_N + v_{N-1}. \qquad (3)$$

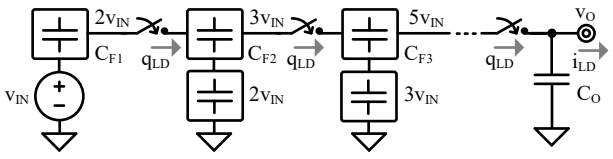

Fig. 4. Telescoping topology.

D. Reconfigurable

Reconfigurable stages further extend SC topologies by allowing C_F to be connected in series or parallel, with stages bypassed or merged as needed, as shown in Fig. 5. Unlike fixed-stage topologies, they do not increase the maximum conversion ratio but enable near-optimal ratio selection over a wide load range.

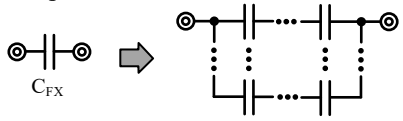

Fig. 5. A reconfigurable flying capacitor.

E. Optimization

A_V is achieved under no-load conditions, when all C_F are fully charged with no charge flow through intermediate stages. Under load i_{LD}', v_O drops as each C_F charges and discharges, causing ohmic loss. Thus, optimal design depends on a fixed i_{LD}'.

$$\text{Optimization} = f(i_{LD}'). \tag{4}$$

III. Output Resistance

A. Static Ohmic Model

As shown in Fig. 6, a static ohmic model characterizes the SC converter in steady state. It is modeled as an ideal transformer with gain A_V and output resistance R_O capturing conduction loss P_R from i_{LD}, appearing as a voltage drop v_R. R_B denotes bottom-plate capacitors, is omitted for illustration purposes.

$$P_R = {i_{LD}}^2 R_O = i_{LD} v_R. \tag{5}$$

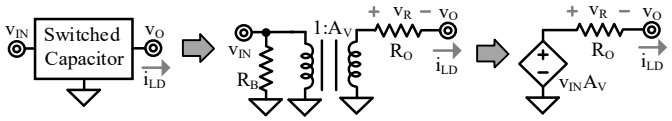

Fig. 6. Static ohmic model of switched-capacitor converter.

As illustrated in Fig. 7, the simulated output voltage v_O of the SC converter does not reach the ideal value $A_V v_{IN}$ under a finite load i_{LD}. Instead, a voltage difference v_R always exists.

$$v_R = v_{IN}A_V - v_{O(AVG)} = i_{LD}R_O. \tag{6}$$

v_O exhibits small oscillations due to the combined effects of the i_{LD} and charge redistribution from the preceding stage.

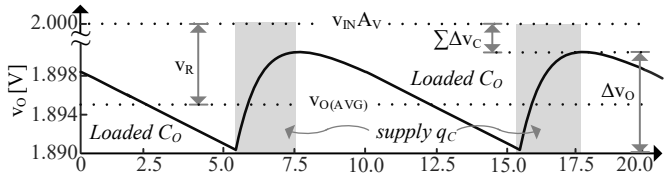

Fig. 7. Simulated v_O with corresponding v_R compared against $v_{IN}A_V$.

B. Transfer Loss

Transfer Regimes: The SC converter operates differently under full transfer (FT) and partial transfer (PT) conditions. FT occurs when the C_F voltage v_C reaches its target voltage v_T within the charging portion of the clock period t_{CLK}, assumed here as 50% of t_{CLK} for illustration in Fig. 8. In contrast, PT occurs when v_C fails to reach v_T during this interval. v_H is the peak voltage of v_C during t_{CLK}, and PT occurs when v_H is less than v_T.

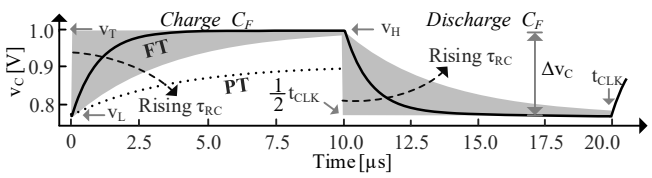

Fig. 8. Simulated voltage changes on a C_F at full transfer or partial transfer.

In PT, C_F is not fully charged, leading to lower transfer currents. This reduces P_R as explained in [31]–[33]. However, decreasing t_{CLK} rapidly increases switching-related losses.

Regime Boundary: As established in [26], operation deep in FT region increases P_R. Therefore, the FT/PT boundary provides the optimal operating point and is adopted as the design target. Accordingly, t_{CLK} is chosen such that v_H reaches approximately 99.5% of v_T within the charging half-cycle.

$$\text{Err} \equiv \frac{v_T - v_H}{v_T} = \left(\frac{\Delta v_C}{v_T}\right)\left(\frac{e^{-\frac{t_{CLK}}{2\tau_{RC}}}}{1-e^{-\frac{t_{CLK}}{2\tau_{RC}}}}\right) \equiv 0.5\%. \tag{7}$$

Beyond this point, further settling only increases transferred charge and reduces efficiency. Under this condition,

$$t_{CLK} \approx 4.34\tau_{RC} = 4.34 C_{EQ} R_{EQ}, \tag{8}$$

where C_{EQ} and R_{EQ} are effective capacitance and resistance.

Charge-Sharing Model: The 99.5% criterion approximates the boundary with negligible deviation from FT, allowing P_R to be modeled using FT model. To evaluate it, the charge-sharing between C_1 and C_2, as shown in Fig. 9, is modeled using C_{EQ},

$$C_{EQ} = C_{SER} = C_1 \oplus C_2 = \frac{C_2 C_1}{C_1 + C_2}. \tag{9}$$

The symbol $\oplus$ denotes a parallel-resistor-like operation.

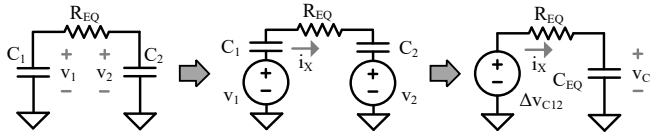

Fig. 9. Equivalent loss model for charge sharing.

When C_1 and C_2, initially charged to v_1 and v_2, are connected, charge redistributes and part of the stored energy is dissipated through resistive paths. The resulting ohmic loss equals the difference E_R between the initial and final stored energies.

$$E_{R1,2} = E_I - E_F = \left(\frac{1}{2}\right) C_1 {v_1}^2 + \left(\frac{1}{2}\right) C_2 {v_2}^2 - \frac{(C_1 v_1 + C_2 v_2)^2}{2(C_1 + C_2)}$$
$$= \left(\frac{1}{2}\right)(C_1 \oplus C_2)(v_1 - v_2)^2 = \left(\frac{1}{2}\right) C_{EQ} {\Delta v_{C1,2}}^2. \tag{10}$$

This loss can be modeled by charging C_{EQ} with $v_1 - v_2$, as shown in Fig. 9, and i_X is the transient current. P_R of this transfer is,

$$P_{RX} = \frac{E_{RX}}{t_{CLK}} = k_R t_{CLK}. \tag{11}$$

Voltage swing: After i_{LD} discharges C_O, preceding stages replenish it in cascade. Each C_F shows a voltage change Δv_C set by i_X, an integer multiple, N_{LD}, of i_{LD} set by the topology.

$$\Delta v_{C(X)} = \frac{q_X}{C_{FX}} = \frac{i_X t_{CLK}}{C_{FX}} = \frac{N_{LD} i_{LD} t_{CLK}}{C_{FX}}. \tag{12}$$

As shown in Fig. 10, Δv_C increases with longer t_{CLK} due to increased charge transfer per period, leading to higher P_R.

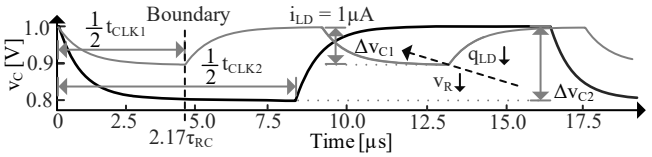

Fig. 10. Simulated Δv_C with different t_{CLK} with full transfer.

C. FT Output Resistance:

R_O, which characterizes the total P_R, can be extracted using static ohmic model by factoring out the i_{LD}^2 term.

$$R_O = \frac{P_R}{i_{LD}^2} = \frac{\sum_{X=1}^{N_X} P_{RX}}{i_{LD}^2}. \quad (13)$$

For an SC converter, the total P_R is given by the sum of P_{RX}, which corresponds to an individual transfer. Each P_{RX} can be calculated as given by (11).

IV. Optimal Capacitance Allocation

A. Limited Total Capacitance

Using very large capacitors reduces ohmic loss by lowering the voltage drop Δv_C on each capacitor. In practice, the total on-chip capacitance C_{TOT} is limited and shared between C_F and C_O.

$$C_{TOT} = C_O + \sum_{X=1}^{N_X} C_F. \quad (14)$$

Therefore, increasing C_O inevitably reduces the budget for C_F, requiring an optimal allocation between C_O and C_F.

B. Flying Capacitance

Since the last C_F, C_{FN}, directly replenishes C_O, it has a reference $\Delta v_C'$ within one clock cycle. All C_F must operate at the FT/PT boundary. Thus, each stage is sized to experience the same $\Delta v_C'$, and each C_F is scaled based on C_{FN} and i_X based on i_{LD},

$$C_{FX} = C_{F(MIN)}\left(\frac{i_X}{i_{LD}}\right) = C_{FN}N_{LD}, \quad (15)$$

where C_{FX} is the capacitance of the C_F at that stage.

C. Low Loss

v_R, defined in (6), has two components: v_{RO} and v_{RC}. v_{RO} comes from the output voltage ripple Δv_O, while v_{RC} is the sum of Δv_C across all preceding C_F, as shown in Fig. 7.

$$v_R = v_{RO} + v_{RC} \approx \frac{1}{2}\Delta v_O + \sum_{X=1}^{N_X} \Delta v_{C(X)}$$
$$= \frac{1}{2}\left(\frac{0.5q_{LD}}{C_O + C_{OEQ}} + \frac{0.5q_{LD}}{C_O}\right) + N_X{}^2\left(\frac{q_{LD}}{C_{TOT} - C_O}\right). \quad (16)$$

Only about half of Δv_O contributes since charge sharing occurs only when C_O is replenished by the preceding stage. Since v_R reflects P_R, capacitance allocation aims to minimize v_R, i.e., minimize P_R. C_{OEQ} is the equivalent capacitance of the C_F group that directly replenishes C_O, and is the only topology-dependent parameter in the proposed methodology. For a single stage, all C_F are connected in series, yielding the minimum C_{OEQ}. For a multi-stage, a single C_F replenishes C_O, giving the maximum C_{OEQ}. Telescoping converters lie between these two limits,

$$C_{OEQ(S)} = \frac{C_{TOT} - C_O}{N_X{}^2} < C_{OEQ(T)} < C_{OEQ(M)} = \frac{C_{TOT} - C_O}{N_X}. \quad (17)$$

D. Ohmic Loss Minimization

Increasing C_O reduces v_{RO} but, under a limited C_{TOT}, leaves less budget for C_F, increasing v_{RC}. As a result, C_O can be increased until the additional v_{RC} cancels the reduction in v_{RO}, yielding a minimum v_R. With C_{OEQ} determined for a given topology and C_{FX} scaled by (15), (17) reduces v_R to a function of the single variable C_O. The optimal C_O is then obtained from,

$$\left.\frac{\partial v_R}{\partial C_O}\right|_{C_O'} = \left.\frac{\partial v_{RO}}{\partial C_O}\right|_{C_O'} + \left.\frac{\partial v_{RC}}{\partial C_O}\right|_{C_O'} \equiv 0. \quad (18)$$

V. Low-Loss Clock:Switch Design

A. Boundary Clock:Width Relationship

After capacitance allocation, given C_{FX} and the resulting C_{EQ}, each t_{CLK} uniquely determines R_{EQ}, and the MOSFET switch width W_{MOS} required based on (8)

$$W_{MOS} = \frac{k_\Omega}{N_S R_{SW}} \equiv \frac{k_\Omega}{R_{EQ}} = \frac{k_\Omega C_{EQ}}{\tau_{RC}} = \frac{4.34 k_\Omega C_{EQ}}{t_{CLK}}, \quad (19)$$

where N_S is number of switches, and k_Ω includes all terms independent of t_{CLK} and W_{MOS}. This forms the basis for systematically minimizing total MOSFET loss P_{MOS}.

B. Boundary MOS Loss

P_{MOS} includes the gate-drive loss P_G, originating from charging and discharging the MOSFET gate capacitances every t_{CLK}. The P_G of a transfer event, P_{GX}, is,

$$P_{GX} = v_{DD}\left(\frac{q_G}{t_{CLK}}\right)N_S = \frac{W_{MOS}k_G{}'}{t_{CLK}} = \frac{k_G}{t_{CLK}{}^2}. \quad (20)$$

Both k_R and k_G are defined similarly to k_Ω.

C. Optimal Boundary Clock & Width

To find the optimal W_{MOS} and t_{CLK} that minimize P_{MOSX}, the derivative of P_{MOSX} with respect to t_{CLK} is set to zero.

$$\left.\frac{\partial P_{MOSX}}{\partial t_{CLK}}\right|_{t_{CLK}'} = \left.\frac{\partial P_{GX}}{\partial t_{CLK}}\right|_{t_{CLK}'} + \left.\frac{\partial P_{RX}}{\partial t_{CLK}}\right|_{t_{CLK}'} \equiv 0. \quad (21)$$

Solving (21) gives the optimal clock t_{CLK}', which increases with N_S and C_{EQ}, and decreases with i_{LD}.

$$t_{CLK}' = \sqrt[3]{\frac{2k_G}{k_R}} \propto \frac{N_S C_{EQ}}{i_{LD}}. \quad (22)$$

The corresponding optimal MOS transistor width W_{MOS}' is

$$W_{MOS}' = \frac{4.34 k_\Omega C_{EQ}}{t_{CLK}'} \propto i_{LD}. \quad (23)$$

This only illustrates the optimization for a single transfer event. In practice, each transfer in the SC topology must be optimized individually using the same method.

VI. Telescoping 1 : 5 V Boosting Example

A. Architecture and Design Flow

A telescoping topology is used as a representative SC converter with nonuniform C_F allocation. The proposed methodology consists of five steps: allocate C_F ratios, determine C_{TOT},

optimize the C_O–C_F allocation, determine t_{CLK} from the boundary, and size the MOSFET by solving k_Ω, k_R, and k_G. Fig. 11 shows a 1:5 telescoping converter with three C_F. Odd and even switches operate on non-overlapping clock phases.

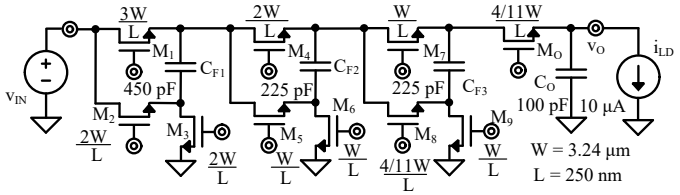

Fig. 11. Telescoping stage with boosting ratio of 1 to 5.

B. Capacitors

In this topology, shown in Fig. 12, C_{F1} charges C_{F2} and C_{F3} simultaneously. As a result, its current i_X is twice i_{LD}. To reach the same $\Delta v_C'$, C_F is scaled as,

$$C_{F1} = 2C_{F2} = 2C_{F3}. \tag{24}$$

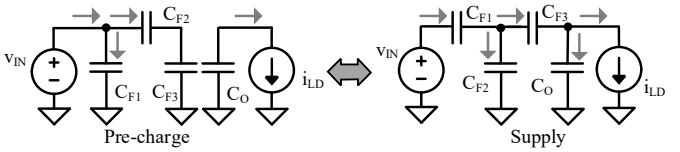

Fig. 12. Pre-charge and supply phases for charging cycles.

With C_{TOT} of 1 nF, C_O' is 100 pF verified by simulation, as shown in Fig. 13, to minimize v_R. This results in C_{F1} being 450 pF and C_{F2} and C_{F3} being 225 pF each.

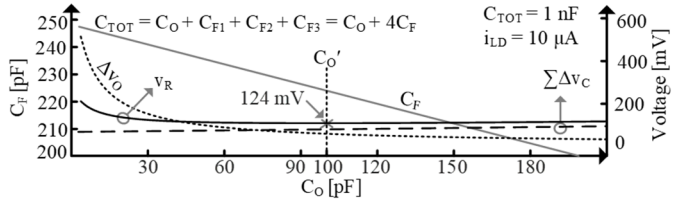

Fig. 13. Δv_O, v_R, $\sum\Delta v_C$, and C_F across C_O at FT showing $v_{R(MIN)}$.

C. Clock

With the capacitors set, each transfer can be optimized at the boundary. As an example, consider the transfer where v_{IN} charges cascaded C_{F2} and C_{F3}. C_{EQ} of this transfer event is

$$C_{EQ} = C_{F2} \oplus C_{F3} = \frac{C_{F3}}{2} = 113\ \text{pF}. \tag{25}$$

Four switches are used, so N_S is 4 and corresponding k_Ω is,

$$k_\Omega = L_{CH}\left[\frac{1}{K_N'(v_{DD}-v_{TH})}\right]N_S = 2.36\ \text{m}\frac{\Omega}{\text{m}}. \tag{26}$$

Then k_R derived from (10) and (12) is

$$k_R \approx \left(\frac{1}{2}\right)C_{EQ}\left(\frac{2i_{LD}}{C_{F3}}\right)^2 = 444\ \text{m}\frac{A^2}{F}. \tag{27}$$

q_G' indicate amount of charge needed per width, and k_G is,

$$k_G = 4.34 v_{DD} q_G' N_S k_\Omega C_{EQ} = 9.95\text{x}10^{-21}\ F^2v^2\Omega. \tag{28}$$

Using k_R and k_G, t_{CLK}' is 355 ns and W_{MOS}' is 3.24 µm.

D. MOS

After the optimal t_{CLK}' and W_{MOS}' are determined for one transfer, to ensure all transfers operate at the FT/PT boundary simultaneously, the remaining transfer paths are designed to have the same τ_{RC}. Therefore, the MOSFET widths of the remaining switches are selected such that,

$$\tau_{RC} = C_{EQA}R_{EQA} = C_{EQB}R_{EQB}. \tag{29}$$

For example, M_1 drives two transfers, the one discussed above and the recharge of C_{F1}. Since C_{F1} is twice C_{F2}, the width of M_1 is scaled by a factor of three.

E. Power Consumption

Fig. 14 shows P_{LOSS} versus W_{MOS} and t_{CLK} without boundary constraints. The analytical design achieves near-minimum loss, with ~3% deviation due to slight inaccuracy in the FT expression. This leads to less than 0.1% efficiency η_C impact, and a local sweep readily identifies the true minimum.

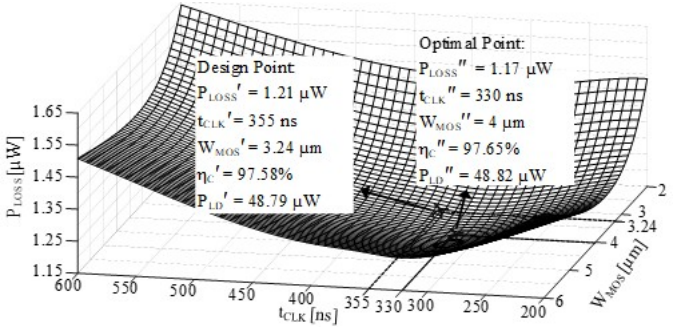

Fig. 14. P_{LOSS} changes with t_{CLK} and W_{MOS}.

Fig. 15 compares η_C of a fixed-width design η_C' with the optimized case η_I across i_{LD}, along with relative difference. Both decrease with increasing i_{LD} due to the quadratic rise in P_R. η_I exceeds η_C' except at 10 µA. The gap reaches ~2% as i_{LD} doubles, indicating low efficiency loss for the fixed-width design.

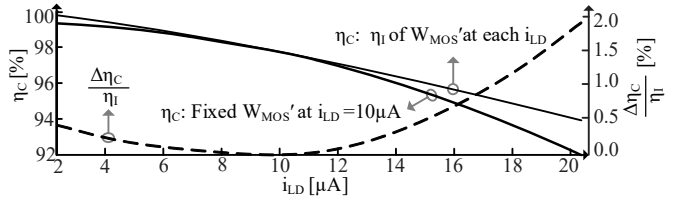

Fig. 15. η_C falls with i_{LD} of fixed W_{MOS}' and optimized W_{MOS}' of changing i_{LD}.

VII. Conclusions

This work presents a topology-independent design methodology for switched-capacitor DC–DC converters based on a static ohmic-loss model and the FT/PT boundary. By using the FT/PT boundary as the design target, the proposed method jointly determines capacitance allocation, clock period, and MOSFET sizing through a unified design flow. Validation on a telescoping 1-V-to-5-V boost converter shows close agreement between analytical predictions and circuit simulations, with less than 0.1% efficiency difference, demonstrating the effectiveness of the proposed methodology.

Acknowledgment

The authors would like to thank Dr. O. Lazaro, Dr. T. Chang, Dr. Joshi, and Texas Instruments for their sponsorship and support.

REFERENCES

[1] A. Meshkat, R. Dehghani, H. Farzanehfard and S. A. Khajehoddin, "Improved On-Chip Inductor Design for Fully Integrated Voltage Regulators," in *IEEE J. of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 6, pp. 7397-7409, Dec. 2022.

[2] G. Kiran Kumar, T. Kobaku, S. Sahoo, B. Subudhi, D. Elangovan, and F. Blaabjerg, "An Overview of Fully Integrated Switching Power Converters Based on Switched-Capacitor versus Inductive Approach and Their Advanced Control Aspects," *Energies*, vol. 14, no. 11, p. 3250, Jan. 2021.

[3] T. M. Andersen *et al*., "A 10 W On-Chip Switched Capacitor Voltage Regulator With Feedforward Regulation Capability for Granular Microprocessor Power Delivery," in *IEEE Trans. on Power Electronics*, vol. 32, no. 1, pp. 378-393, Jan. 2017,

[4] J. Kim, P. K. T. Mok, and C. Kim, "A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 414–425, Feb. 2014.

[5] D. Kilani, B. Mohammad, H. Saleh and M. Ismail, "Switched capacitor DC-DC converter for ultra-low power applications," *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Marseille, France, 2014, pp. 463-466.

[6] D. Newell and M. Duffy, "Review of Power Conversion and Energy Management for Low-Power, Low-Voltage Energy Harvesting Powered Wireless Sensors," in *IEEE Trans. on Power Electronics*, vol. 34, no. 10, pp. 9794-9805, Oct. 2019.

[7] J. Kim, P. K. T. Mok and C. Kim, "A 0.15 V Input Energy Harvesting Charge Pump With Dynamic Body Biasing and Adaptive Dead-Time for Efficiency Improvement," in *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 414-425, Feb. 2015,

[8] A. Stillwell and R. C. N. Pilawa-Podgurski, "A Resonant Switched-Capacitor Converter With GaN Transistors for High-Efficiency Power Delivery to Series-Stacked Processors," in *IEEE J. Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 3139-3150, Sept. 2020,

[9] L. G. Salem, "A Recursive N-Path Switched-Capacitor Rectifier for Piezoelectric Energy Harvesting," in *IEEE J. Solid-State Circuits*, vol. 60, no. 4, pp. 1461-1473, April 2025.

[10] G. W. den Besten and B. Nauta, "Embedded 5 V-to-3.3 V voltage regulator for supplying digital IC's in 3.3 V CMOS technology," in *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 956-962, July 1998,

[11] K. K. Pakkirisami Churchill, G. Chong, H. Ramiah, M. Y. Ahmad and J. Rajendran, "Low-Voltage Capacitive-Based Step-Up DC-DC Converters for RF Energy Harvesting System: A Review," in *IEEE Access*, vol. 8, pp. 186393-186407, 2020.

[12] S. Mondal and R. Paily, "An Efficient On-Chip Switched-Capacitor-Based Power Converter for a Microscale Energy Transducer," in *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 63, no. 3, pp. 254-258, March 2016,

[13] T. Ozaki, T. Hirose, H. Asano, N. Kuroki and M. Numa, "Fully-Integrated High-Conversion-Ratio Dual-Output Voltage Boost Converter With MPPT for Low-Voltage Energy Harvesting," in *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2398-2407, Oct. 2016.

[14] H. -C. Cheng, P. -H. Chen, Y. -T. Su and P. -H. Chen, "A Reconfigurable Capacitive Power Converter With Capacitance Redistribution for Indoor Light-Powered Batteryless Internet-of-Things Devices," in *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 2934-2942, Oct. 2021.

[15]]A. Cabrini, L. Gobbi, and G. Torelli, "Voltage gain analysis of integrated Fibonacci-like charge pumps for low power applications," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 11, pp. 929–933, Nov. 2007.

[16] N. Butzen and M. Steyaert, "A Single-Topology Continuously-Scalable-Conversion-Ratio Fully Integrated Switched-Capacitor DC-DC Converter with 0-to-2.22V Output and 93% Peak-Efficiency," *2018 IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, 2018, pp. 103-104.

[17] N. Butzen *et al*., "14.4 A Monolithic 26A/mm2Imax, 88.5% Peak-Efficiency Continuously Scalable Conversion-Ratio Switched-Capacitor DC-DC Converter," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 232-234.

[18] N. Butzen and M. Steyaert, "Design of Single-Topology Continuously Scalable-Conversion-Ratio Switched- Capacitor DC–DC Converters," in *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1039-1047, April 2019.

[19] C. Hardy *et al*., "11.1 A Scalable Heterogeneous Integrated Two-Stage Vertical Power-Delivery Architecture for High-Performance Computing," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 182-184.

[20] N. Butzen and M. Steyaert, "10.1 A 1.1W/mm2-power-density 82%-efficiency fully integrated 3:1 Switched-Capacitor DC-DC converter in baseline 28nm CMOS using Stage Outphasing and Multiphase Soft-Charging," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2017, pp. 178-179.

[21] T. M. Andersen *et al*., "4.7 A sub-ns response on-chip switched-capacitor DC-DC voltage regulator delivering 3.7W/mm2 at 90% efficiency using deep-trench capacitors in 32nm SOI CMOS," *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, San Francisco, CA, USA, 2014, pp. 90-91.

[22] N. Butzen and M. S. J. Steyaert, "MIMO Switched-Capacitor DC–DC Converters Using Only Parasitic Capacitances Through Scalable Parasitic Charge Redistribution," in *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1814-1824, July 2017.

[23] Y. Yoon *et al*., "A Continuously-Scalable-Conversion-Ratio Step-Up/Down SC Energy-Harvesting Interface With MPPT Enabled by Real-Time Power Monitoring With Frequency-Mapped Capacitor DAC," in *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 69, no. 4, pp. 1820-1831, April 2022.

[24] H. -P. Le, M. Seeman, S. R. Sanders, V. Sathe, S. Naffziger and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 81% efficiency," *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2010, pp. 210-211.

[25] Y. K. Ramadass, A. A. Fayed and A. P. Chandrakasan, "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS," in *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557-2565, Dec. 2010.

[26] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," in *IEEE Trans. on Power Electronics*, vol. 23, no. 2, pp. 841-851, March 2008.

[27] M. S. Makowski and D. Maksimovic, "Performance limits of switchedcapacitor dc–dc converters," in *IEEE Power Electron*. Spec. Conf., Jun. 18–22, 1995, pp. 1215–1221.

[28] T. S. Ho, H. Ramiah, K. K. P. Churchill, Y. Chen, P. -I. Mak and R. P. Martins, "Extended Power Dynamic Range and Enhanced Power Conversion Efficiency of a Switched-Capacitor DC–DC Converter: A Tutorial," in *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 71, no. 3, pp. 1606-1612, March 2024.

[29] G. Palumbo and D. Pappalardo, "Charge Pump Circuits: An Overview on Design Strategies and Topologies," in *IEEE Circuits and Systems Magazine*, vol. 10, no. 1, pp. 31-45, First Quarter 2010.

[30] Chi-Chang Wang and Jiin-Chuan Wu, "Efficiency improvement in charge pump circuits," in *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 852-860, June 1997.

[31] C. K. Tse, S. C. Wong and M. H. L. Chow, "On lossless switched-capacitor power converters," in *IEEE Trans. on Power Electronics*, vol. 10, no. 3, pp. 286-291, May 1995.

[32] G, Zhu et al., "Switched-capacitor power supplies: DC voltage ratio, efficiency, ripple, regulation," IEEE ISCAS, pp 553–556, May. 1996.

[33] Z, Pan et al., "Power losses and efficiency analysis of multilevel dc-dc converters," IEEE APEC, pp 1393–1398, Mar. 2005.