Switched-Inductor Multiple-I/O Power Supplies: MOSFET Selection and Cross Conduction

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***Abstract*—Switched-inductor power supplies are valued for their high efficiency despite the bulkiness of off-chip inductors. To enhance power density, single-inductor topologies are favored. However, single-inductor multiple-input/multiple-output power supplies (SL-MI/O) present unique design challenges that haven't been sufficiently explored. To assist designers with MOSFET selection, which is non-trivial in SL-MI/Os, an intuitive metric called the Favorability Index (F_{NP}) is introduced. The paper also discusses methods that can be employed to mitigate unwanted turn-on of switches shorting inputs/outputs (cross conduction). Furthermore, a two-transistor selector topology is recommended to block cross conduction with lower impact on efficiency.**

***Index Terms*—DC-DC, single inductor, multiple inputs, multiple outputs, efficiency, cross conduction, favorability index, CMOS.**

I. Switched-Inductor Multiple-I/O Power Supplies

Switched-inductor power supplies, widely used in electronics [1]–[3], offer high efficiency but require bulky inductors. The increasing prevalence of microelectronics, such as Internet-of-Things (IoT) devices [4], emphasizes the need for high power-density. Consequently, using only a single inductor is preferred.

As electronics grow in complexity, power supplies need to generate multiple voltages [5]–[7], requiring multiple outputs. Systems with diverse sources necessitate multiple inputs [8]–[10]. Some systems require both multiple inputs and outputs [11]–[13]. This paper refers to all of the above as Single-Inductor Multiple-Input/Multiple-Output (SL-MI/O) designs. A general SL-MI/O system diagram with input one v_{I1} to input N v_{IN} and output one v_{O1} to output N v_{ON} is depicted in Fig. 1.

In MI/O systems, power switches are connected to many different voltages. Selection between an NMOS or a PMOS for a particular power I/O switch becomes non-trivial, particularly at intermediate voltage levels. Furthermore, to provide power to and source power from multiple I/Os, the inductor in an SL-MI/O needs to cycle its current to and from multiple voltage levels. This results in complex switching voltages at inductor nodes that can cause unwanted turn-on of switches (cross conduction). Designs like hybrid/switched-capacitor power supplies or charge pumps may also experience similar cross conductions [14], making the insights discussed in this paper relevant for a broader range of power supply configurations.

In Sec. II, an analysis of MOSFET selection is presented. The Favorability Index (F_{NP}) is introduced as an intuitive metric to aid designers. Sec. III outlines the challenges of SL-MI/Os with cross conduction, and Sec. IV and Sec. V discuss common and proposed solutions for it. In Sec. VI, design methods presented are demonstrated through an example design flow.

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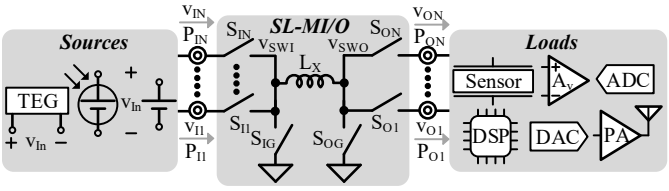

Fig. 1. SL-MI/O system diagram.

II. MOSFET Selection

A. Power Losses

Design of switches is usually governed by losses; control loops are usually ones that determine response time. When designing a power I/O switch, the first consideration is choosing between an NMOS and a PMOS. Intuitively, one can examine the gate drive (overdrive) voltage v_{GST}. It represents the ohmic loss P_R as current passes through the switch's on-resistance. But it constitutes only one part of a MOSFET switch's losses, with another significant part being the gate-charging loss P_G. For MOSFET selection, the total losses of N/PMOS should be compared. Because the type with lower P_R may exhibit higher P_G, and the sum of losses is not necessarily lower.

Note that $v_{DD/SS}$ variables in this paper refer to the gate drivers' high-side/low-side supply of each switch, and not global supply rails. The v_{SS}/v_{DD} of an N/PMOS switch is always connected to its source (v_S) unless otherwise specified. That is because NMOS's open with collapsed v_{GS}, the gate voltage v_G only needs to reach the source voltage v_S to open it. PMOS's open with collapsed v_{SG}, where v_G reaches v_S.

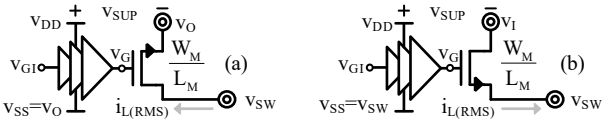

Fig. 2. Example NMOS I/O power switches.

P_{R0} and P_{G0} can be derived in (1)–(3) [15]. The subscript 0 differentiates (1)–(3) from modified equations introduced later. $i_{L(RMS)}$ is RMS inductor current, $K_{N/P}'$ is the transconductance parameter, W_{M0} is the channel width, and f_{SW} is the switching frequency. The on-resistance R_M is calculated in deep triode since that is the operating region of power switches. k_{R0} and k_{G0} are coefficients defined here to simplify presentations.

$$P_{R0} = i_{L(RMS)}{}^2 R_M d_{ON} \equiv \frac{k_{R0}}{K_{N/P}{}' \left| v_{GST} \right| W_{M0}}, \tag{1}$$

$$v_{SUP} = v_{DD} - v_{SS}, \tag{2}$$

$$P_{G0} = v_{SUP} q_G f_{SW} \equiv k_{G0} v_{SUP}{}^2 W_{M0}. \tag{3}$$

In (3), v_{SUP} is used instead of v_{DD} to account for the gate charge q_G sourced from v_{DD} being returned to v_{SS} during gate discharge. The overall MOSFET loss P_{M0} is approximately the sum of P_{R0} and P_{G0}. In consumer applications with 10 V or lower voltages, I-V overlap loss P_{IV} is usually lower than P_{R0} and P_{G0} by at least an order of magnitude. Thus, it is omitted here. P_{R0} is inversely proportional to W_{M0}, while P_{G0} is linearly proportional. Consequently, there is an optimal W_{M0}' at which point the sum is the lowest [15]. At W_{M0}', P_{M0} reaches the optimum at P_{M0}', shown in (4). P_{M0}' is the loss that should be compared between the N and PMOS to justify design choices.

$$P_{M0}' = P_{R0}' + P_{G0}' = 2P_{R0}' = 2P_{G0}' = 2\sqrt{\frac{k_{R0}k_{G0}v_{SUP}^{\ 2}}{K_{N/P}'v_{GST}}}. \quad (4)$$

B. Favorability Index

A favorability index F_{NP0} can be defined to help with MOSFET selection. F_{NP0} is the ratio of a switch's P_{M0}' when it is a PMOS to that of an NMOS. A value of F_{NP0} greater than one indicates lower power loss in NMOS, favoring its use. Conversely, a value smaller than one favors PMOS.

$$F_{NP0} \equiv \frac{P_{MP0}'}{P_{MN0}'} \approx \sqrt{\left(\frac{v_{SUPP}}{v_{SUPN}}\right)^2\left(\frac{K_N'}{K_P'}\right)\left(\frac{v_{GST}}{v_{SGT}}\right)}. \quad (5)$$

Many variables cancel for the same switch in F_{NP0}, and non-dominant terms are approximated away to get (5). If they're notably different, the accurate ratio equation defined in (5) must be used. If all conditions are equal, an NMOS is always better due to its higher carrier mobility. For switches connected to the lowest/highest voltage in the system, F_{NP0} is infinite/0. These are obvious, but F_{NP0} becomes useful for switches connected to intermediate voltages. F_{NP0} is plotted in Fig. 3 as a 3D surface across v_{SUP}'s and v_{GST}'s ratios, along with the boundary where F_{NP0} is equal to 1, to visualize the impact of F_{NP0} components.

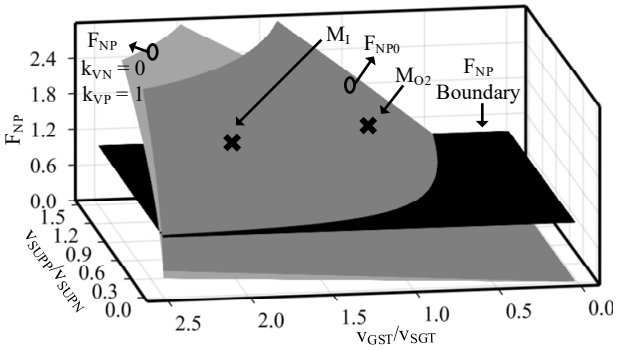

Fig. 3. Favorability Index.

III. Inaccessible Inputs/Outputs

A. Body Diodes

A MOSFET can unintentionally conduct through its body diodes, shown in Fig. 4. Using the NMOS as an example, if v_{NS} drops below v_{NB}, the body diode D_{NS} conducts. In this paper, arrows denote the NMOS source terminal as the terminal with lower potential during normal operation and, conversely, the terminal with higher potential for a PMOS. If the device is bidirectional, arrows are annotated on both terminals. D_{PD} is used to denote a PMOS's drain side body diode, etc.

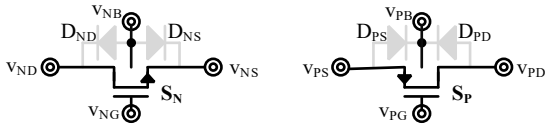

Fig. 4. Body diodes in a MOSFET.

B. MOS Diodes

The MOSFET itself can also act like a diode, most commonly when v_G is connected to v_D. But it can also act like a diode even when v_G is connected to a static rail. Using the NMOS shown in Fig. 5 as an example, it is opened by connecting v_G to v_{SS}. However, if v_{NS} drops below v_{SS} by more than a threshold v_T, a v_{GS} is still established, and the NMOS turns on, conducting like a diode. The MOS diode can turn on instead of or in parallel with the body diode, depending on the v_T vs. the diode drop.

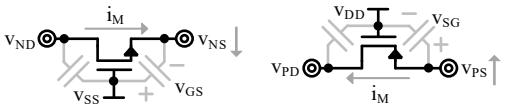

Fig. 5. MOSFETs as MOS diodes.

C. Cross Conduction

In a SL-MI/O, a single inductor is connected to multiple I/O voltages. Each or both nodes at the inductor, v_{SWI} and v_{SWO}, can swing across two or more voltages. Due to MOSFET diodes described above, v_{SW}'s may have two or more diodes connected to different voltages. One of the diodes would then conduct and clamp v_{SW}, causing reverse conduction and preventing the other voltage(s) from being accessible. This can cause significant issues such as device failures and power loss.

Consider Fig. 6's example system. Bodies are connected such that only one body diode on each side (M_{I1}'s and M_{O1}'s) conducts dead time current. M_{I1} and M_{O1} are turned on for intended conduction. However, as v_{O1} is higher than v_{ON}, M_{ON}'s MOS diode turns on. This shorts v_{ON} and v_{O1} and clamps v_{SWO}. M_{O2} to M_{ON-1} would also have diode conduction, regardless v_B connects v_S or v_D. Grey arrowed lines represent unwanted cross conduction that happens instead of the desired conduction path.

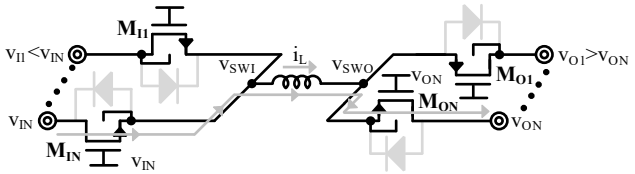

Fig. 6. Cross conduction at input and output.

Similarly on the input side, M_{I1}'s turn-on triggers diode conduction in M_{I2} to M_{IN}. Consequently, blocking both the body and MOS diodes of I/O switches is imperative. But designers should leave one switch unblocked to conduct dead time current. References [14], [16]–[24] all exhibited cross conduction with solutions categorized in the sections below.

IV. Blocking Body Diodes

A. Static Bias

The simplest way to block the conduction of body diodes is to bias the body to a static extreme voltage [19], [20] instead of

v_S, such that the body diodes are always reverse biased. An N/PMOS can bias its v_B with the most negative/positive voltage that can occur on its v_S. However, this requires body access, and the switch suffers from body effect during conduction. This can increase the ohmic loss drastically with high $v_{SB/BS}$.

B. Opposite Diodes

Body diode conduction can also be blocked by putting two MOSFETs in series with their bodies connected in different directions [16]–[18], as shown in Fig. 7. This way, even if one diode conducts, the other blocks it with its opposite orientation.

However, using series-connected switches results in a fourfold increase in resistance for the same area. This rise in resistance substantially increases overall loss, rendering this solution undesirable in many cases. However, this can be the only solution for devices where the body is tied to the source.

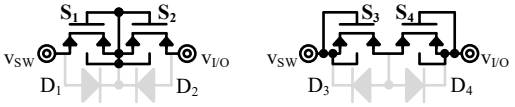

Fig. 7. Opposite diodes switches.

C. Body-Bias Selector

1) Operation: This paper recommends blocking body diodes with a selector depicted in Fig. 8a which dynamically selects the min/max voltage between v_S and v_D to bias v_B [14], [21]–[24]. Using M_{IN} in Fig. 6 as an example, the selector always selects the lower voltage between v_{SWI} and v_{IN}. It could select either during conduction, eliminating body effect. Cross conduction through body diodes is thus blocked without incurring excessive loss through body effect or series switches.

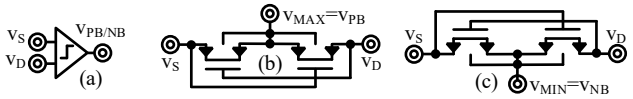

Fig. 8. Generic and two-transistor selector implementations.

2) Generic Selector: The selector can be implemented in various ways, but it must operate asynchronously; otherwise, cross conduction or voltage spikes would still happen during dead time. One implementation could be a hysteretic common gate comparator connected to two switches [21] that switches v_B between v_S and v_D. However, there can be many design challenges like quiescent power, ICMR, response time, etc.

3) Two-Transistor Selector: The simplest implementation with just two switches, depicted in Fig. 8b/c, is recommended. Comparison is achieved by cross-connecting v_G's and v_S's. The two input voltages are usually the v_S and v_D of the power switch in the context of this paper. When one input voltage is different from another, it causes one selector switch to be more on and the other one off. One selector switch is entirely on if the difference is more than V_{T0}, connecting the output to the correct voltage. This topology can select the lowest/highest voltage with just 2 N/PMOS's, and operate asynchronously and fast. v_T /V_{T0} stands for threshold voltage with/without body effect.

The downside of this implementation is that when v_S and v_D are too close to each other, with a difference $|v_{ID}|$ smaller than V_{T0}, neither of the switches is on. The output, therefore, becomes high-impedance until $|v_{ID}|$ rises above V_{T0}, shown below in a DC plot in Fig. 9. In practice, the selector output can take some time to reach its final state in the high-impedance region, due to low sub-v_T currents. Therefore, when using this selector, the switch could still have a $v_{SB/BS}$ of around V_{T0} during conduction, resulting in a small body effect. This can be alleviated with low-v_T devices in the selector.

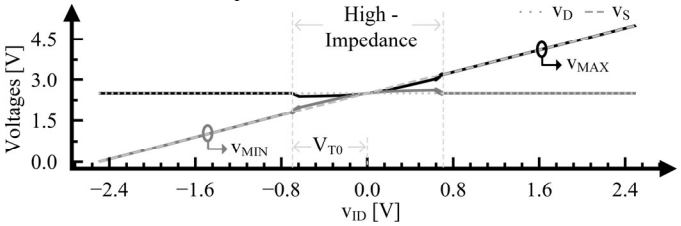

Fig. 9. Simulated two-transistor selector operation in DC.

V. Blocking MOS Diodes

A. Static Bias

MOS diodes can be blocked in the same way as body diodes described in Sec. IV.A. To prevent establishing v_{GST}, a static extreme voltage [24], [25] can be used to supply v_G's of N/PMOS's when opening them. Using M_{ON} in Fig. 6 as an example, it can be opened by supplying v_G with v_{O1} instead of v_{ON}. Then there's no v_{SGT} even when v_{SWO} rises to v_{O1}. However, q_G is now sourced from a higher supply voltage v_{O1} instead of v_{ON}, potentially increasing P_G significantly.

B. Opposite Diodes

Like the concept described in Sec. IV.B, the MOS diodes can be "pointed" at each other when the switches are supposed to be opened. By connecting the gate drivers' supplies when the switch is off in opposite directions, the MOS diodes are effectively pointed against each other. The correct connections are shown in Fig. 7, with the gate drivers abstracted away.

C. Gate-Supply Selector

1) Operation: The body-bias selector can simultaneously be used as the gate-supply selector. MOS diode conduction is blocked by selecting the min/max voltage between v_S and v_D to supply v_G. The selector should balance its switching loss against the P_{IV} of the I/O switch. Since P_{IV} is usually negligible in consumer applications, the switching loss of the selector is also minimal. Using a gate-supply selector provides many benefits compared to static biasing:

2) Reduced Supply Power: When charging a capacitor, it is more efficient to source the charge from the lowest supply voltage possible. Consider the turn-off of a PMOS shown in Fig. 10. Suppose after the PMOS is opened with $v_{I/O}$, v_{SW} is switched to a $v_{SW(HI)}$ higher than $v_{I/O}$. Cross conduction happens if it is not addressed. If we address it by statically supplying v_G with $v_{SW(HI)}$, then P_{G0} is (3), with v_{SUP} being $v_{SW(HI)}$ minus v_{SS}.

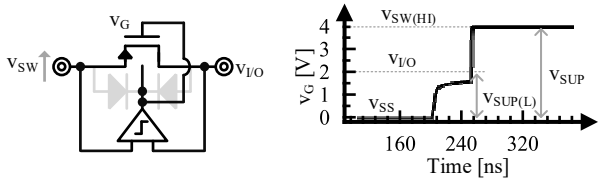

Fig. 10. Gate supply selector operation.

If v_G is connected to a maximum selector, however, it goes through a two-step charging. First, v_G is charged to $v_{I/O,}$ which opens the switch. Then, as v_{SW} rises, v_G follows it to $v_{SW(HI)}$ as the selector selects v_{SW}. The gate capacitance is first charged from v_{SS} to $v_{I/O}$ with $v_{I/O}$ supplying q_{G1}, then from $v_{I/O}$ to $v_{SW(HI)}$ with $v_{SW(HI)}$ supplying q_{G2}, instead of directly from v_{SS} to $v_{SW(HI)}$ with $v_{SW(HI)}$ supplying $q_{G1} + q_{G2}$. The resulting P_G is lowered compared to P_{G0} in (3) due to $v_{SUP(L)}$ being lower than v_{SUP}.

$$\begin{aligned} P_G &= \left(v_{SUP(L)} q_{G1} + v_{SUP} q_{G2}\right) f_{SW} \\ &\equiv k_{G0}\left(1 + k_V\right) {v_{SUP(L)}}^2 f_{SW} \equiv k_G {v_{SUP(L)}}^2 f_{SW} < P_{G0}. \end{aligned} \tag{6}$$

3) Reduced Gate Charge: If v_G and v_B are connected to the selector, as shown in Fig. 10, then in the second step, when both v_G and v_B are rising from $v_{I/O}$ to $v_{SW\,(HI)}$, Δv_{GB} is negligible and C_{GB} is not charged. Similarly, with the selector selecting v_S to supply v_G, Δv_{GS} is negligible and C_{GS} is not charged.

Therefore, the C_{CH} in C_{GB} and one C_{OL} in C_{GS}, after the switch is already opened with $v_{I/O}$, aren't charged. Only one C_{OL} in C_{GD} is charged in the second step, and the gate charge q_{G2} needed for the second step is significantly reduced, as expressed in (7). Note that the reduced supply power and gate charge also roughly apply to the opposite diode method described in Sec. V.B, but it won't be expanded on in this paper.

$$q_{G2} = \left(v_{SUP} - v_{SUP(L)}\right) C_{OL} << q_{G1}. \tag{7}$$

4) Modified F_{NP}: Since P_G for switches using selectors in (6) is different from (3), the F_{NP0} in (5) needs to be updated. The new k_G can be expressed as a modified k_{G0} in (3) with a modifier k_V expressed in (8). k_V can then be applied on the denominator or numerator of $F_{NP0,}$ depending on whether the N or PMOS version of the switch would require the selector. If both versions require blocking with the selector, F_{NP} becomes (9).

$$k_V = \frac{v_{SUP} q_{G2}}{v_{SUP(L)} q_{G1}} = \left(\frac{v_{SUP}}{v_{SUP(L)}}\right)\left(\frac{v_{SUP} - v_{SUP(L)}}{v_{SUP(L)}}\right)\left(\frac{L_{OL}}{L_{EQ}}\right). \tag{8}$$

$$F_{NP} \equiv \frac{{P_{MP}}'}{{P_{MN}}'} = F_{NP0}\sqrt{\frac{1 + k_{VP}}{1 + k_{VN}}}. \tag{9}$$

VI. Validation

A. SL-SIMO Buck–Boost Example

To illustrate the design methods outlined in the paper, a typical buck–boost system which Fig. 1 shows and Fig. 11 embodies is chosen. The system has a v_I of 4 V, a v_{O1} of 6 V, and a v_{O2} of 3 V. The voltages and parameters are selected for easier demonstration of MOSFET selection and cross conduction without otherwise additional significance. $K_{N/P}{}'$ is 150 μ/50 μ, V_{T0} is 0.7 V, f_{SW} is 1 MHz, and i_O is up to 2A.

B. Favorability Index

M_{IG} and M_{OG}, connected to the lowest voltage in the system, are selected as NMOS's. M_{O1}, connected to the highest voltage, is selected as a PMOS. F_{NP0} needs to be consulted for M_I and M_{O2}. F_{NP0} can be calculated as 2.17 for M_I and 1.73 for M_{O2}, ignoring cross conduction. NMOS is superior in both cases because it is assumed that both have equal access to the body, and therefore neither suffers body effect. If the NMOS body is substrate at ground, v_T needs to be adjusted for body effect, and F_{NP0} becomes 0.5 for M_I and 1.29 for M_{O2}.

C. Cross Conduction

Cross conduction does not happen for switches connected to highest and lowest voltages, which are M_{IG}, M_{OG}, and M_{O1}. With $v_{SS/DD}$ correctly connected to v_S, N/PMOS M_{O1} also does not have cross conduction unless another input voltage higher than v_I is added. N/PMOS M_{O2}, with its $v_{SS/DD}$ connected to v_{O2}/v_{SWO}, must block cross conduction due to M_{OG} connecting v_{SWO} to ground, establishing a $|v_{GST}|$. M_{O2}'s body diode would conduct no matter whether v_B is connected to v_D or v_S, since v_{SWO} can reach voltages both higher and lower than v_{O2}.

Since blocking with selector is required for both N/PMOS M_{O2}, F_{NP} can be calculated with (9) with both k_{VN} and k_{VP}. But k_V's cancel since $v_{SUP(L)}$ and v_{SUP} are the same for both N/PMOS M_{O2}, resulting in F_{NP} equal F_{NP0}. $F_{NP(0)}$ of M_{O2} and M_I are also annotated in Fig. 3. From the F_{NP} results the CMOS system can be implemented as shown in Fig. 11, the widths shown are the $W_M{}'$s at the annotated mid-range i_L.

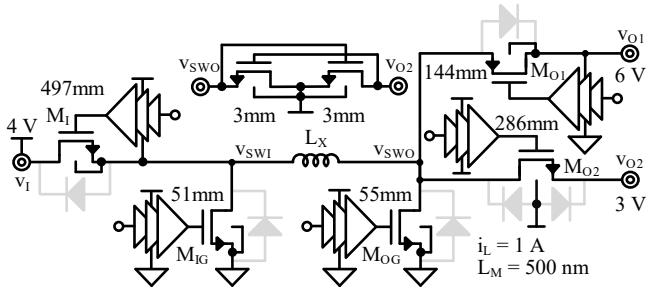

Fig. 11. Example SL-MI/O buck–boost.

Cross conduction is eliminated, and F_{NP} results is verified by measuring $P_M{}'$ of both N/PMOS M_{O2} across i_L, applying $W_M{}'$ at each point. Fig. 12 shows M_{O2}'s PMOS loss being higher than NMOS loss at all i_L, agreeing with its F_{NP} of 1.73.

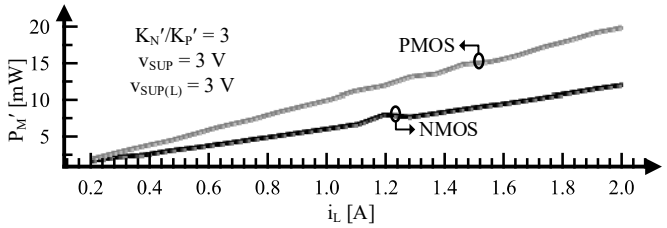

Fig. 12. Simulated M_{O2} loss as NMOS vs. PMOS.

VII. Conclusions

This paper presents design guidelines and insights concerning power switch design in SL-MI/Os. A brief analysis of optimal power MOSFET losses is presented, from which a Favorability Index (F_{NP}) is derived. This provides designers with an intuitive metric for choosing between an NMOS vs. a PMOS for a power I/O switch. Methodologies to block cross conduction are explored, and a solution with a simple two-transistor selector topology is recommended. Power savings from using a selector is presented. The favorability index is updated to apply to switches that block cross conduction with a selector. Finally, the theories are validated through simulations.

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