Maximum DC–DC Conversion in Switched-Inductor Power Supplies

Qiwei Chen, Graduate Student Member, IEEE, and Gabriel A. Rincón-Mora, Fellow, IEEE
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, U.S.A.
aren_chen@gatech.edu and rincon-mora@gatech.edu

Abstract—High DC–DC voltage conversion is crucial in many emerging fields. However, the maximum achievable voltage conversion of switched-inductor power supplies (SLPS) has been a lingering question. This paper first establishes the inversely proportional relationship between minimum duty cycle and maximum conversion ratio in ideal SLPS. Then, how propagation delays limit the minimum duty cycle is found. The difference between actual and ideal duty cycle, caused by losses in the power stages, is analyzed. By translating delay-limited minimum duty cycle and loss-induced duty cycle shift into ideal SLPS’s duty cycle, the maximum conversion of any actual SLPS can be determined.

In summary, this paper presents expressions and insights to analyze and understand maximum DC–DC conversion of SLPS.

Keywords—Propagation delay, power losses, maximum voltage gain, voltage translation, buck–boost, extreme duty ratio.

I. DC–DC CONVERSION IN POWER-SUPPLY SYSTEMS

Power supplies are essential for all systems that require external electrical power to operate. DC–DC power supplies are designed to sustain a constant voltage or current from a constant input voltage, examples of which are shown in Fig. 1.

Many emerging fields, such as USB power delivery, electric vehicle, and computation center, require power supplies to step-up or step-down voltages by high ratios. Most literatures on high DC–DC conversion power supplies utilized cascaded power stages, such as multiple switched-inductors [1]–[3], or switched-inductor/capacitor hybrid [4]–[12]. They all need additional components and usually more complex control schemes compared to standalone switched-inductor power supplies (SLPS) [13]–[19]. However, these costs for high DC–DC conversion applications remain unjustified unless the conversion exceeds the capability of SLPS. Past discussions have touched upon some factors’ impact on voltage conversion of certain SLPS [4], [20]–[24]. But the general conversion limit of SLPS is largely unexplored in the state-of-the-art.

In this paper, theory to find maximum DC–DC conversion ratio of SLPS is developed and validated with simulation. Section II introduces the operation and maximum conversion ratio of ideal SLPS, while Section III and IV explain how propagation delay and power losses impose limitation on real systems. Section V reveals the approach to find realistic maximum DC–DC conversion ratio and provides simulation validation of the theory, and Section VI concludes the paper.

II. SWITCHED-INDUCTOR DC–DC CONVERSION

A. Operation

In SLPS, the switched-inductor Lx serves as an energy storage device that receives and delivers energy in alternating energize and drain phases, as shown in Fig. 2. Across energize time tE, inductor voltage vL includes input voltage vi, and in drain time tD, it includes output voltage v0 to supply the load from source.

As Fig. 3 shows, in steady state, across conduction time tC, vL switches between ideal energize voltage vE during tE and ideal drain voltage vD during tD, keeping an average vL of 0 V. Meanwhile, inductor current IL rises and falls by the same ripple current ∆IL that can be calculated with:

$$\Delta I_L = t_E \frac{dI_L}{dt_E} = t_E \frac{v_E}{L_X} = t_D \frac{v_D}{L_X}$$

The ideal energize duty cycle dE, the tE fraction of tC, can also be represented by vE and vD, and it sums to 1 with the ideal drain duty cycle dD:

$$d_E \equiv \frac{t_E}{t_C} = \frac{v_E}{v_E + v_D} = 1 - d_D.$$  (2)

B. Conversion Ratio

As (2) shows, vD exceeds vE when dE is above 50 % and vice versa. An ideal buck-boost converter, shown in Fig. 4(a), can convert-up or convert-down vE to vD, which are vE and vD, as shown in Table I. Buck or boost converter in Fig. 4(b) or (c) are variations of buck-boost, with the absence of output or input switches. Their v0’s can only be lower or higher than v1.
The up or downward conversion ratio $K_{V(I)}$ from $V_i$ to $V_o$ is always larger than $1/V$. The input and output switching node voltages ($V_{SWI}$ and $V_{SWO}$) are duty-cycle fractions of $V_i$ and $V_o$. Since $V_{L( AVG) } = 0$, $V_{SWI}$ and $V_{SWO}$ have the same average value. $K_{V(I)}$ is then the ratio between $d_i'$ and $d_o'$, the duty cycles of $L_x$ connecting to $V_i$ and $V_o$ respectively:

$$K_{V(I)} = \frac{v_{i/o}}{v_{o/i}} = \left( \frac{v_{SWI/O(AVG)}}{d_{i/o}} \right) = \frac{d_{o/i}'}{d_{i/o}}.$$  

### C. Conversion Limit

The maximum conversion ratio $K_{MAX}$ would then be the ratio between maximum and minimum $d_i'$ or $d_o'$. By variable substitution, it can be expressed with only minimum $d_{MIN}$; or $d_{MIN}'$ in short, for buck–boost (BB), buck (BK), and boost (BS):

$$K_{MAX} = \frac{d_{o/i}(MAX)}{d_{i/o}(MIN)} = \frac{1}{d_{MIN}} \frac{d_{o/i}(MAX)}{d_{MIN}} = \frac{1}{d_{MIN}}.$$  

### III. DELAY LIMIT

It is now established that $d_{MIN}$ is the limiting factor for $K_{V(I)}$. Ideally, $d_{MIN}$ can approach 0 % and $K_{MAX}$ can approach $\infty$. However, in an actual system, there is a minimum energize or drain duty cycle provided to the switches, $d_{MIN}$.

#### A. Control Loop

Fig. 5 shows a simplified control loop diagram of SLPS, where the properties to be controlled, such as $V_o$ or $i_o$, are sensed and fed to the circuits that process the information into a control signal $V_{EO}$. The duty cycler then translates $V_{EO}$ into an alternating duty cycle command $V_G'$ that the driver uses to turn the switches on and off. In steady state, the feedback signal and $V_{EO}$ are constant, while the duty cycler and the driver operate switches at $d_{E/D}$, with $d_{MIN}$ possible.

#### B. Discontinuous-Conduction Mode

In Discontinuous-Conduction Mode (DCM), $t_c$ is a fraction of the switching period $t_{SW}$. After the drain phase, $i_r$ remains at 0 until the next $t_{SW}$ begins. As Fig. 6 shows, even with minimum energize time $t_{E(MIN)}$, $d_E$ can still decrease with $t_c$ extending into the zero-current period. The same applies to decreasing $d_D$.

In CCM, $t_c$ equals $t_{SW}$, and $d_{MIN}$ is dependent on $t_{SW(MAX)}$ and $t_{E/D(MIN)}$. For a component with propagation delay $t_p$, it can only reproduce inputs no shorter than $t_p$, as Fig. 7 shows.

---

<table>
<thead>
<tr>
<th>Table I: Ideal Voltages and Duty Ratios</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_i$</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>Buck-Boost</td>
</tr>
<tr>
<td>Buck</td>
</tr>
<tr>
<td>Boost</td>
</tr>
</tbody>
</table>

---

**PWM Loop:** In Pulse-Width Modulation (PWM) control, the duty cycler has a fixed $t_{SW}$ in this scheme, $d_{MIN}$ is determined solely by $t_{E/D(MIN)}$, or the delays. The expression for $d_{MIN}$ would be (6) with a constant denominator $t_{SW}$.

**Valley/Peak Loop:** $t_c$ or $t_p$ can be designed to be constant in valley or peak loop. Such, $d_{E(MIN)}$ in valley loop and $d_{D(MIN)}$ in peak loop are limited by $t_{SW(MAX)}$, or the lowest switching frequency $f_{SW}$ allowed before the control loop’s response time.
and stability is impacted by \( f_{SW} \) approaching the unity gain frequency. In this case, the numerator in (6) should be constant \( t_{E/D} \). In the alternative case that variable \( t_p \) or \( t_g \) is very short and \( f_{SW} \) is close to the preset \( t_p \) or \( t_g \), (6) shows approximate expression of \( d_{MIN} \) when the denominator is constant \( t_{E/D} \).

**Hysteretic Loop:** The power supplies can also be controlled by limiting \( i_L \) within a window. Since the energize or drain actions are administered whenever \( i_L \) reaches the boundaries, there is no preset \( t_{E/D} \) or \( t_{SW} \). Hence, (6) is accurate.

### IV. Power-Loss Duty Cycle Shift

Though \( d_{MIN} \) can be found with delays, (4) cannot be directly applied to a real, lossy system in which \( v_L \) is altered. This section analyzes the effects of power losses on a synchronous buck–boost shown in Fig. 9. Since buck and boost are buck–boost without certain components, their losses are naturally included in this analysis. Output capacitor \( C_0 \) and its series resistance \( R_C \) may not always be present in all SLPS.

**Fig. 9.** Power stage of buck–boost converter.

### A. Conduction-Path Losses

Across \( t_{E/D} \), current losses in the direction of \( v_L' \). Losses along the conduction path reduces \( v_L' \) into \( v_L \), the actual \( v_L \) during \( t_{E/D} \):

\[
v_L \approx v_L' - i_{L(AVG)} R_E - v_{IV(E)} \tag{7}
\]

where \( R_E \) is the resistance in energize path and \( v_{IV(E)} \) is the average energize voltage reduced by switches’ current-voltage (IV) overlap transient. As left of Fig. 10 shows, when \( v_{DS} \) rises to \( v_{TH} \) and \( v_{GS} \) falls below approximately as linearly as the switch closes. Across interval \( t_{V(E)} \), \( v_L \) is reduced by the average voltage \( v_{DS} \) traverses, \( 0.5(v_0 + v_{DS}) \). Similarly, \( v_{DS} \) of \( M_E \) traversing through \( v_1 + v_{DC} \) contribute to a lower \( v_L \). We can then derive:

\[
v_{IV(E)} = \left(\frac{v_{V(E)/D}}{v_{E/D}}\right) \left(\frac{v_1 + v_{DS}}{2}\right) + \left(\frac{v_{V(E)/D}}{t_{E/D}}\right) \left(\frac{v_0 + v_{DS}}{2}\right) \tag{8}
\]

where \( v_{DS} \) and \( v_{DS} \) are diode voltages of \( D_0 \) and \( D_0 \), which can have different values for Silicon, Schottky, or MOS diode. The IV overlap effects of \( M_{DG} \) and \( M_{DO} \) are negligible as their \( v_L \)’s traverse only \( v_{DS} \) and \( v_{DS} \) across short \( t_{V(E)} \’s \).

**Fig. 10.** Simulated transitions of \( M_{EG} \).

### B. Energize Duty-Cycle Shift

The energize duty cycle in a lossy system can then be expressed in terms of the actual \( v_L \) and \( v_L \) applied on \( L_x \):

\[
d_E = \frac{v_{D} + v_{D} \cdot i_{L(AVG)} R_E + v_{DT(D)} - v_{IV(D)}}{v_{D} + v_{D} \cdot i_{L(AVG)} (R_{D} - R_{E}) + v_{DT(D)} - v_{IV(D)} - v_{IV(E)}}, \tag{9}
\]

and the shift in energize duty cycle between lossy and lossless system, under identical conditions, is altered. This effect of \( \Delta d_E \) in (10) shows the average effect of diode drops on \( v_L \) during \( t_{DT(D)} \). In the case of an asynchronous system, \( R_D \) contains no resistance of \( M_{DG} \) and \( M_{DO} \), and \( 2t_{DT} \) equals \( t_0 \) in:

\[
v_{DT(D)/SW} = \left(\frac{2t_{DT}}{t_{SW}}\right) (v_{DG} + v_{DO}). \tag{10}
\]

As right of Fig. 10 shows, after \( M_{EG} \)’s \( v_{GS} \) drops to \( v_{TH} \), \( v_{DS} \) does not rise instantaneously but linearly across \( v_{IV(D)} \), reducing \( v_L \). This effect of \( M_{EG} \) and \( M_{EG} \)’s IV overlap is \( v_{IV(D)} \) in (8).

### C. Loading Effect

Previous subsections only considered the losses that alter \( v_L \). Some losses do not change \( v_L \), but effectively diverge current away from the output node or the load:

\[
i_{LD(\text{EFF})} = i_{LD} + i_{LG} + i_{G} + i_{DG} = t_{DT} + i_{LV} \tag{11}
\]

\[
i_{LG} = \frac{t_{DG}}{v_{D} \cdot v_{O}}, \tag{12}
\]

\[
i_{LD} = \frac{v_{D} \cdot v_{G}}{t_{SW}} \tag{13}
\]

For boost and buck–boost, whose \( i_0 \) is a \( 1 - d_E \) fraction of \( i_{L(AVG)} \), a higher \( d_E \) would result in a decrease in available \( i_{DG} \).
\[ i_{d_0} = i_{L(AVG)}(d'_0 - d_0) = \Delta d_E i_{L(AVG)} |_{\text{BS,BB}} \]  
\[ (17) \]

Additionally, in each \( t_{MT} \), some forward recovery charge \( q_{FR} \), which is proportional to forward transit time \( t_F \), is trapped in \( D_0 \) that could have been supplied to the load:

\[ i_{d_T} = \frac{2q_{FR}}{t_{SW}} |_{\text{BS,BB}} \approx \frac{2\tau i_{L(AVG)}}{t_{SW}} |_{\text{BS,BB}} \]  
\[ (18) \]

Referring to Fig. 11, it can also be seen that \( M_{EG} \) starts steering current away from the output \( t_{v(E)} \) before it closes and starts feeding the output \( t_{v(D)} + t_{i(D)} \) later than it is supposed to. Across \( t_1 \)'s, \( i_{BS} \) rises or falls roughly quadratically. The output current taken during IV overlap is then:

\[ i_{IV} = \frac{4E_{EG(V)}}{t_{SW}} \approx \left( \frac{t_{v,EG(D)}}{3} + \frac{t_{v,EG(U)}}{3} \right) \left( \frac{i_{L(AVG)}}{t_{SW}} \right). \]  
\[ (19) \]

Fig. 11 shows the trend of individual contribution and the total loading current \( i_{LOSS} \) across \( i_{L(AVG)} \). Both \( i_{d_T} \) and \( i_{IV} \) increase linearly with \( i_{L(AVG)} \), while \( i_{d_0} \) has both linear and quadratic components since \( \Delta d_E \) also increases with \( i_{L(AVG)} \).

![Fig. 11. Calculated loading effects.](image)

**V. MAXIMUM DC–DC CONVERSION**

As discussed, \( d_E' \) is a relationship between \( v_E \) and \( v_D' \), and can be derived from \( d_E \) and \( \Delta d_E \). In other words, a lossy SLPS operating at \( d_E \) can be reflected into an ideal SLPS operating at \( d_E' \) with the same \( v_E \) and \( v_D' \), or \( v_1 \) and \( v_0 \) as Table I shows. When the actual system operates at its delay-limited \( d_{MIN} \), the imaginary ideal system has:

\[ d_{MIN}' = \frac{d_E}{d_{MIN}} - \Delta d_E/d_D = d_{MIN} \mp \Delta d_E. \]  
\[ (20) \]

From (4), \( K_{V_{U/T}}^{MAX} \) can be found and it is also the maximum conversion ratio of the actual, lossy system between identical \( v_1 \) and \( v_0 \) as the equivalent ideal system. It is worth noting that higher delay-limited \( d_{MIN} \) always lowers \( K_{V_{U/T}}^{MAX} \). Fig. 12 shows the trend of decreasing \( K_{V_{U/T}}^{MAX} \) with higher \( t_{P(MAX)} \) and \( d_{MIN} \).

![Fig. 12. Simulated maximum conversion ratio respect to delay.](image)

**A. Buck Example**

The buck converter example in Fig. 14 is supplied by a USB and operates at a \( f_{SW} \) of 1 MHz with a 10 ns \( t_{DT} \). Its duty cycle has \( t_p^+ \) of 100 ns and \( t_p^- \) of 110 ns, while the drivers have a \( t_{PD} \) of 5 ns. At conversion limit, \( d_{E(MIN)} \) is 10.5 %, and \( R_{EQ} \) exhibited is 56.7 m\( \Omega \). Simulated with SPICE, \( K_{V_{B(max)}}^{MAX} \) rises from 9.6 to 17.5 V/V across 0.1 – 4 V of \( i_{L(AVG)} \) as Fig.13 shows. When the power stage is replaced with lossless components and duty cycle’s \( t_p \) varies, Fig. 12 shows simulated \( K_{V_{B(max)}}^{MAX} \).

![Fig. 14. Implementation of a buck example.](image)

**B. Boost Example**

The boost example in Fig. 15 supplies a USB load and operates with the same \( f_{SW} \), \( t_{DT} \), and delays. At conversion limit, \( d_{E(MIN)} \) is 10.5 % and \( R_{EQ} \) is 57.7 m\( \Omega \). \( K_{V_{B(max)}}^{MAX} \) falls from 9.4 to 6.5 V/V across \( i_{L(AVG)} \) as Fig.13 shows. Fig. 12 shows \( K_{V_{B(max)}}^{MAX} \) when the power stage is lossless and duty cycle’s \( t_p \) varies.

![Fig. 15. Implementation of a boost example.](image)

**VI. CONCLUSIONS**

This paper comprehensively analyzes the factors affecting the maximum DC–DC conversion in SLPS. By lumping the impact of losses into a shift from delay-limited minimum duty cycle, an actual system can be reflected into an ideal equivalence, where the maximum conversion can be easily determined. The minimum duty cycle is largely set by the longest single-component delay, higher of which lowers achievable conversion ratio. Resistance, dead time, and IV overlap cause the duty cycle shift, which extends the maximum conversion in voltage step-down applications but reduces it in step-up. With the derivations and insights presented, designers can now assess the feasibility of using SLPS in high conversion applications.

**ACKNOWLEDGMENT**

The authors thank Analog Devices, Inc. (ADI) for sponsoring this research and Dr. Hua Chen for his support and advice.


