A High Bandwidth, Bypass, Transient-Mode Sigma–Delta DC–DC Switching Boost Regulator with Wide LC Compliance

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***Abstract* – DC-DC switching regulators are critical building blocks in electronic systems and integrating them on chip affords numerous savings in system size, cost, and design complexity. A key portion of these regulators is the frequency compensation circuit and, because of its dependence to the passive LC filter parameters in the power stage, it resists integration. This hindrance to system-on-chip (SoC) integration can be overcome by adopting a sliding-mode control scheme, which, in implementing a variation of a sigma-delta (ΣΔ) converter, gives stable operation for a wide range of LC filter values, without the need for a frequency compensation circuit. However, sliding-mode boost DC-DC converters designed to tolerate wide LC variations exhibit a slow transient response because the bandwidth of the feedback circuit is necessarily low, significantly lower than the main power path's bandwidth, which is a requirement for stability. This paper proposes a switching boost converter with a high bandwidth, bypass, ΣΔ path that yields fast transient response (up to 50 % ΔV reduction) – limited only by slew-rate conditions. The proposed converter achieves this fast response without a degradation in LC filter compliance, steady-state voltage ripple (± 0.2 %), or efficiency. In effect, the presented strategy decouples the conflicting design requirements of high relative stability and fast transient response without requiring compensation circuits and therefore offering integrated, user-friendly solutions.**

I. INTRODUCTION

With an ever-increasing demand for compact and portable electronics with high-functionality, CMOS circuit integration has become a key trend in the semiconductor industry. From a power management standpoint, one of the critical blocks that hinder the complete integration of switching DC-DC converters is the frequency compensation circuit, whose design is based on the values of off-chip LC filter components [1]. Since these LC filter values vary, because of various design requirements, manufacturer tolerances, and/or parameter drifts, integration of a compensation circuit implies a non-optimal control design and a lower bandwidth solution.

The direct impact of a non-optimal compensation circuit is reflected in the transient response performance of the regulator, which is critical for voltage accuracy and stability in portable applications when driving switching loads like processors, motors, etc. The poor transient response can be offset by increasing the size of the output capacitor, requiring more PCB real estate and cost. Because of the right-half plane (RHP) zero in the loop gain of boost converters [2] and the resulting instability, the above requirement is more pronounced, as will be discussed here.

Pulse-width modulated (PWM) current-mode control in boost converters eases the converter stability requirements by regulating the filter inductor current with an additional, high bandwidth control loop, thereby reducing the converter small-signal transfer function to single-pole characteristics for frequencies of interest [3]. However, the main control loop (output voltage loop) requires a frequency compensation circuit, which is designed according to the output RC pole. As a result, the LC filter compliance of this converter is severely restricted by the designed compensation circuit.

Sliding-mode control [4-6] senses and mixes the inductor current and output voltage information in a single loop, thereby effectively implementing a variation of sigma-delta (ΣΔ) control [7] and current-mode control, and eliminating the need for a frequency compensation circuit. Consequently, converters based on this *single ΣΔ loop* technique are inherently stable [4-6], tolerating wide LC variations. However, the feedback path that determines the inductor current reference has a bandwidth necessarily lower than that of the power path [5], thereby limiting the transient response. As a result, when designed to tolerate wide LC variations, the bandwidth of the feedback path determining the inductor current reference has to be at its lowest value, which is set by the worst-case LC filter values (highest L and C). The overall result is significantly slow transient response, i.e., degraded transient voltage accuracy is obtained for other choices of LC filter values.

Controling the inductor current and output voltage using independent sigma-delta (ΣΔ) loops is a viable option [8]. Besides having wide LC filter compliance, this *dual ΣΔ* technique achieves a fast load transient response. However, these benefits were obtained at the cost of a higher switching voltage ripple (degraded accuracy) and reduced high-load efficiency.

This paper proposes a converter with a high-bandwidth, bypass transient-mode sigma-delta (ΣΔ) path around a conventional ΣΔ-based converter. The combined strategy responds in a fast single switching cycle, irrespective of the

LC filter. Concurrently, it achieves wide LC compliance, low steady-state ripple (high accuracy), and high efficiency.

The rest of the paper is organized as follows. Section II presents a background of the aforementioned single and dual ΣΔ loop control techniques and Section III describes the proposed technique and circuit. Comparative system simulation results are described and discussed in section IV, followed by key conclusions in Section V.

II. BACKGROUND

Output voltage based ΣΔ control in buck converters is known to enjoy wide LC filter compliance and fast transient response [9-11]. However, this control strategy is not prevalent in boost converters, where the output voltage does not yield complete inductor current information, which is required for stability. Below is a discussion on the reported sigma-delta boost converters.

A. Single ΣΔ Loop

Sliding-mode control is known to yield stable converter operation for wide variations in LC filter values. In its most commonly used and practical implementation in boost converters (Fig. 1), the sensed and scaled *ripples* in the inductor current and the output voltage are mixed to generate a new control variable σ, which is regulated to zero through a ΣΔ loop, as shown in Fig. 2. The inductor current reference I_{REF} is obtained as the average value of the sensed current itself, so that the difference between the two is only the ac current ripple. To achieve stable operation, an important requirement is that the bandwidth of the low-pass filter generating I_{REF} be less than the non-dominant pole, which is the larger of the inductor and output poles.

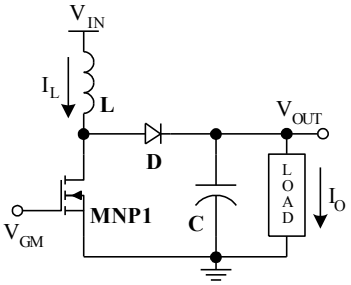

Fig. 1. Circuit schematic of a boost converter power stage.

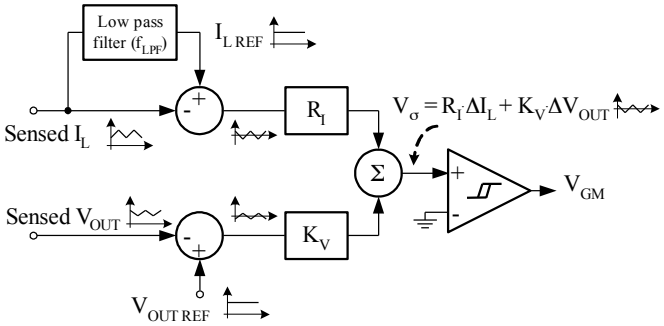

Fig. 2. Schematic representation of single ΣΔ loop control.

This condition is given in [5] as

$$f_{LPF} < \frac{1}{2\pi}\left(\frac{R_{LOAD}}{L_{EQ}} + \frac{2}{R_{LOAD}C}\right), \qquad (1)$$

where R_{LOAD} is the equivalent load resistance, L_{EQ} is the equivalent boost inductance ($L/[1-D]^2$) [5], and D is the duty-cycle of switch MNP1.

It is seen from Equation (1) that, for a converter designed to tolerate wide LC filter variations, filter frequency f_{LPF} has to be determined for the worst-case condition, i.e., largest L, largest C, and $R_{LOAD} = (2 \cdot L_{EQ}/C)^{1/2}$, *giving the lowest value of* f_{LPF}. Since f_{LPF} determines the bandwidth of the converter, a slow load transient response is obtained for a any LC filter combination that is not the aforementioned extreme. Furthermore, for small-signal stability, the ratio of the current and voltage scaling gains R_I and K_V needs to be greater than a critical value G_{CRIT} given in [5] as

$$G \equiv \frac{R_I}{K_V} > G_{CRIT} = \frac{L}{R_{LOAD}C(1-D)}. \qquad (2)$$

For higher values of G, the inductor current takes multiple switching cycles to increase, leading to an even slower transient response. In other words, the transient response of the converter is limited by the bandwidth of the feedback circuit, rather than the slew-rate limit of the converter's power stage.

B. Dual ΣΔ Loop

This technique, first proposed in [8], uses separate ΣΔ loops to control the inductor current and output voltage, adding a current-mode loop and responding quickly to transient load events. The current loop is regulated to its reference I_{REF} in a separate high frequency loop such that it appears as a current source in the voltage control loop (Fig. 3). The output voltage is regulated by a low frequency loop containing auxiliary switch S_A. Regulated current I_{REG}, flowing through the diode when switch MPP3 is open, is kept at a higher level than load current I_O. By sensing the output voltage, comparator Q_1 controls the duty-cycle of switch S_A, thus controlling the average current flowing to the load and hence the average output voltage. In response to a load transient step, the inductor current is increased in a single step, limited only by the its slew rate, thus giving a stable and fast transient response, without needing any frequency compensation circuit.

Dual-loop sigma-delta control and its advantages, viz., fast transient response and wide LC filter compliance, are achieved at the cost of a higher steady-state output voltage ripple (by up to ± 2 %) and increased inductor current (by up to 5 % above the nominal value in typical boost converters). This increased current leads to reduced high-load efficiency (by up to 2.5 %) [8].

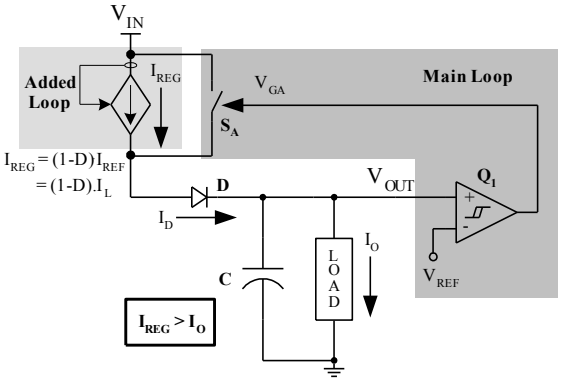

Fig. 3. Simplified schematic of a dual ΣΔ loop control.

III. PROPOSED TECHNIQUE

The proposed strategy incorporates the benefits of both the single and dual ΣΔ loop control techniques described earlier, while simultaneously eliminating their drawbacks. Simplistically and qualitatively stated, it consists of two parallel paths in the control loop, viz., a high gain, low frequency path that operates in steady state and a low gain, high frequency threshold-based path that operates only during transients. The proposed solution effectively functions as a single ΣΔ loop controller during steady state, yielding low output voltage ripple and high efficiency. During high-frequency transient events, however, the circuit functions as a dual ΣΔ loop controller, giving fast transient response.

The main ΣΔ path (with transfer function M(s) in Figs. 4(a) and (b)) has a high DC gain and a low frequency pole p_1.

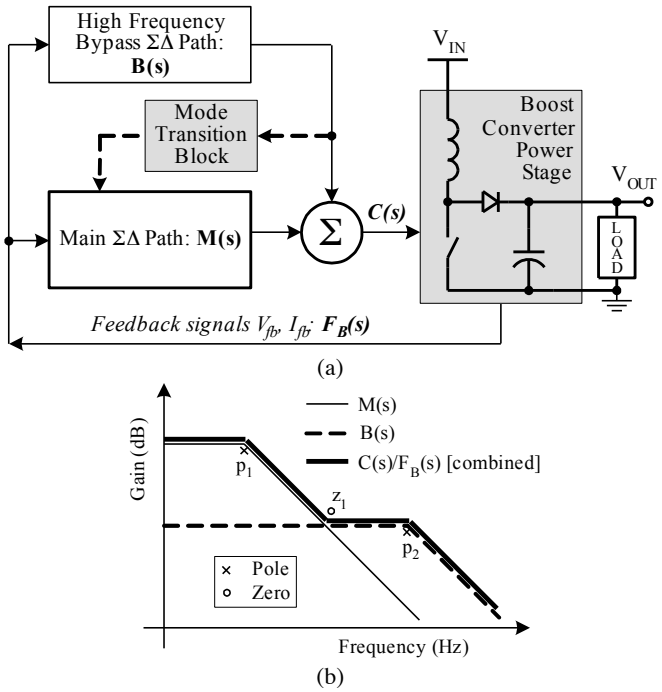

Fig. 4. Proposed transient bypass control strategy: (a) block-level schematic and (b) overall Bode plot response.

On the other hand, the bypass ΣΔ block with transfer function B(s) has a low DC gain and a high frequency pole p_2. The combined transfer function $C(s)/F_B(s)$ therefore has the effect of having, in addition to these two poles, a feedforward zero z_1. Consequently, the main ΣΔ block dominates at frequencies below the location of zero z_1, including DC. For higher frequencies, the bypass ΣΔ path dominates, giving a fast transient response. The mode transition block functionally transfers control between the main and bypass ΣΔ loops.

A. Detailed Circuit Description

The main ΣΔ loop implements single ΣΔ loop control in steady state. As shown in Fig. 5, it is comprised of summing comparator Q_2 with different gains K_I and K_V for scaling the inductor current and output voltage ripples, respectively. While the output voltage is sensed through resistive divider R_1-R_2, the inductor current is sensed through sense resistor R_S. Resistive current sensing is used here for simplicity but other more power efficient sensing techniques as described in [12] may be implemented. Inductor current reference V_{IREF} is the output of the low-pass filter (LPF) – filtered sense current. The output of comparator Q_2 (V_{G1}) is used to control switch MNP1 in the main ΣΔ path, thus controlling both the inductor current and output voltage simultaneously.

The bypass ΣΔ block implements dual ΣΔ loop control and is comprised of hysteretic comparator Q_1, which senses the output voltage, and auxiliary switch MPP3 connected across the inductor. Gate signal V_{GA} for switch MPP3 is derived from the output of comparator Q_1 and is an input to the mode transition block (Fig. 6) along with sensed voltage V_s and reference voltage V_{REF}.

The mode transition block outputs signals to the main ΣΔ loop during modal transitions. Comparator Q_3 compares the sensed voltage V_S with voltage V_R in Fig. 6, which is stepped down to 98 % of V_{REF}, and triggers switch MPC1. Output V_{C1} of the mode transition block, when low, disables voltage gain K_V of comparator Q_2, reducing it to zero and enabling the use of comparator Q_2 in a current regulating loop.

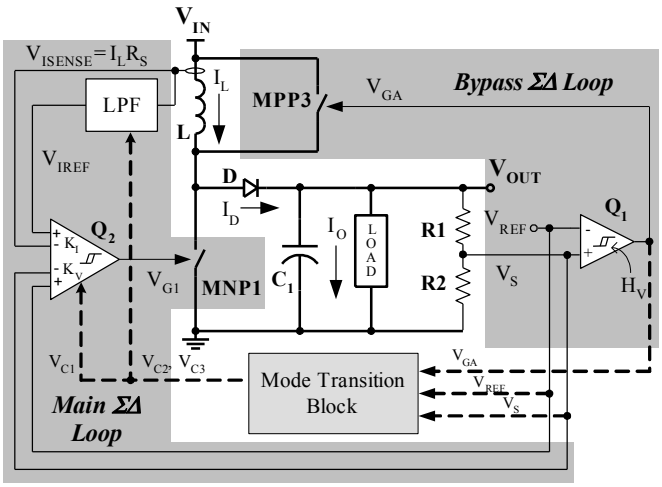

Fig. 5. Schematic of the proposed boost converter control strategy.

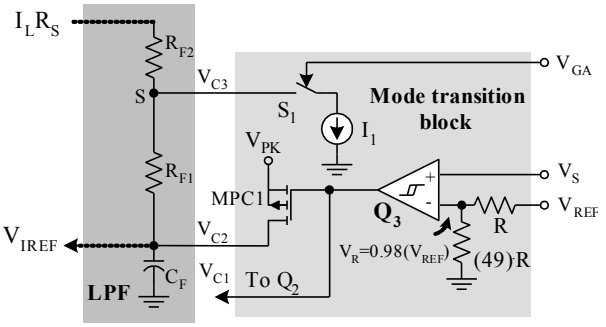

Fig. 6. Schematic of the mode transition block and low pass filter LPF.

B. Circuit Operation

Functionally, the proposed circuit effectively operates in two modes, namely, single ΣΔ loop via the main ΣΔ path and dual ΣΔ loop through the bypass ΣΔ block. The mode transition circuit manages the transition from one mode to the other. The detailed operation of these three blocks is described below.

1) Main ΣΔ loop: The main ΣΔ loop, which operates in steady state, is fully controlled by summing comparator Q_2, which amplifies the *ripples* of the sensed inductor current and output voltage by gains K_I and K_V, respectively, to generate an internal variable σ, which is regulated to zero by the feedback control action of Q_2. The cut-off frequency of low pass filter LPF (f_{LPF}) and gains K_I and K_V are designed to satisfy Equations (1) and (2) with worst-case LC filter design values. The control action of comparator Q_2 is given by the following relation:

$$K_I\left(V_{IREF} - I_L R_S\right) + K_V\left(V_{REF} - V_S\right) = 0 \,. \qquad (3)$$

Inductor current reference V_{IREF}, being the averaged value of the sensed inductor current $I_L R_S$, equals $I_L R_S$ at DC. Hence, at DC, Equation (3) reduces to

$$K_V\left(V_{REF} - V_S\right) = 0 \,, \qquad (4)$$

implying that the sensed DC voltage (V_S) is regulated to its reference (V_{REF}), thus performing the desired output voltage regulation. Auxiliary switch MPP3 is always open and the bypass ΣΔ block containing comparator Q_1 is inactive.

This loop gives wide LC filter compliance and low output voltage ripple. However, the transient response is slow due to non-optimal control (designed to meet the worst-case LC specifications). This slow response is corrected using the fast bypass ΣΔ loop during transient conditions.

2) Bypass ΣΔ loop: The bypass ΣΔ loop, operating during transient events only, is controlled by comparator Q_1, which senses and controls the output voltage through the duty-cycle of switch S_A. During bypass loop operating conditions, the average inductor current is higher than its minimum value I_{LMIN}, which is required to support load current I_O [3],

$$I_L = \frac{I_D}{(1-D)} > I_{LMIN} = \frac{I_O}{(1-D)} = \frac{I_{DMIN}}{(1-D)} \,, \qquad (5)$$

where D is the duty cycle of switch MNP1, I_D is the average current through diode D, and I_{DMIN} is the value of I_D corresponding to I_{LMIN}. The currents in Equation (5) indicate averaged values over one switching cycle of switch MNP1. As a side note, inductor current I_L equals I_{LMIN} during steady state conditions, i.e., main loop operation.

With switch MPP3 open, the difference between diode current I_D and load current I_O flows into capacitor C, thus charging it linearly. An increase in the sensed capacitor voltage (V_S) above its reference (V_{REF}) is monitored by comparator Q_1, which closes auxiliary switch S_A. The closed MPP3 switch shorts inductor L, thereby freewheeling the inductor current and reverse-biasing diode D, which cuts off current flow into capacitor C. Consequently, load current I_O discharges capacitor C. When sense voltage V_S falls below V_{REF}, comparator Q_1 opens switch S_A, repeating the cycle. Consequently, comparator Q_1 regulates the average output voltage at its desired value by controlling the duty cycle of switch S_A.

As long as inductor current I_L is greater than its minimum value (I_{LMIN}), the bypass loop regulates the average sensed voltage (V_S) to V_{REF}, *irrespective of the inductor current*. Therefore, the second term in Equation (3) reduces to zero, giving the control equation of comparator Q_2 as

$$K_I\left(V_{IREF} - I_L R_S\right) = 0 \,. \qquad (6)$$

In other words, comparator Q_2 simply regulates the sensed inductor current to its reference value, which is the DC value of the sensed current itself. This current loop is therefore self-sustaining and the inductor current, as it is, remains constant. The higher-than-minimum inductor current leads to slightly increased power losses and output voltage ripple, which is why the inductor current has to be reduced to I_{LMIN}, a task managed by the mode transition block with the introduction of an offset *within the current loop*.

3) Mode transition: The mode transition block manages the transitions between the two operating modes described earlier. It senses the excess inductor current (I_L–I_{LMIN}) when the circuit operates in the bypass ΣΔ mode and gradually reduces the reference (V_{IREF}) until the inductor current equals its minimum value. Since switch MPP3 switches only in the bypass ΣΔ mode, its gate signal V_{GA} is used as an indicator and measure of excess inductor current. From Fig. 6, a current I_1 is pulled out of node S whenever switch MPP3 is closed. With resistor R_{F2} in the low-pass filter designed to be much smaller than R_{F1}, most of current I_1 flows through resistor R_{F2}, creating a voltage offset $I_1 R_{F2}$ between the sensed inductor current ($I_L R_S$) and its reference (V_{IREF}). This offset causes a reduction in the duty cycle of switch MNP1 and therefore a reduction in inductor current I_L until switch MPP3 stops switching, i.e., inductor current I_L equals I_{LMIN}. As a result, the circuit naturally and smoothly transitions from the bypass mode to the main ΣΔ steady state mode.

In case of sustained load transitions, comparator Q_3 from Fig. 6 senses a drop in the sensed output voltage V_S. When V_S falls below V_R, which is 98 % of V_{REF}, the output of comparator Q_3 goes low, turning on switch MPC1 and raising the inductor current reference V_{IREF} (and hence the sensed

inductor current $I_L R_S$) to V_{PK} in a single step. Voltage V_{PK} is set such that the peak sensed inductor current $I_{LPK}R_S$ is greater than minimum inductor current I_{LMIN}, which corresponds to maximum load current $I_{O(MAX)}$,

$$I_{LPK} = \frac{V_{PK}}{R_S} > \frac{I_{O(MAX)}}{(1-D)}. \quad (7)$$

Simultaneously, gain K_V is reduced to zero by the mode transition block through V_{C1}. Then, the control action of comparator Q_2 is again governed by Equation (6). Therefore, comparator Q_2 regulates the inductor current to I_{LPK}. The choice of I_{LPK} in Equation (7) ensures that the conditions of Equation (5) are always satisfied; hence, the circuit naturally transitions to the bypass ΣΔ mode. Since the inductor current increases to its final value in a single step, fast transient response is achieved.

IV. SIMULATION RESULTS AND DISCUSSION

To validate the operation of the proposed technique and to compare its performance under identical operating conditions with state-of-the-art sigma-delta boost converters, circuit simulations were performed using the simulator Spectre™, which is a part of the Cadence suite. The general operating conditions of the testing environment included a V_{IN} of 3.3 V, V_{OUT} of 5 V, and I_{OUT} from 0.1 to 1 A, and the other parameters given in Table I.

Steady-state waveforms of the proposed circuit where L is 5 μH, C is 47 μF, and I_O is 0.1 A, are shown in Fig. 7. It is seen that the circuit starts as a dual ΣΔ loop converter with an output voltage ripple of ± 100 mV (±2 % of V_{OUT}). As the excess inductor current gradually decreases and finally disappears, the circuit transitions to single ΣΔ loop control. Switch MPP3's gate voltage V_{GA} (active low) stops pulsing as the circuit enters single ΣΔ loop mode. The steady-state voltage ripple is approximately ± 0.2 %.

Load transient waveforms for the proposed circuit with the above LC values and a load step from 0.1 to 1 A are shown in Fig. 8. In response to the load step, the inductor current rises in a single switching cycle, limited only by its slew rate until it reaches 1.7 A. A fast voltage transient with a voltage drop ΔV of 250 mV and a short transient time of 83 μs is observed.

For comparison, a state-of-the-art single ΣΔ loop controller was designed to operate within the LC filter range specified in Table I. Load step response for the single ΣΔ loop converter under identical conditions is shown in Fig. 9. As was mentioned earlier, a single ΣΔ loop controller has the highest bandwidth and therefore the fastest response for the lowest stable value of the current/voltage gain ratio K_I/K_V. For the waveforms in Fig. 9, the gain ratio was adjusted to 0.22, which was the lowest ratio guaranteeing stability at L = 30 μH, C = 30 μF, and R_{LOAD} = 5 Ω. Furthermore, the value of the low-pass filter frequency f_{LPF} was designed (2.7 kHz) to give an optimally damped response with the smallest voltage transient. Under these conditions, the voltage transient for a load step of 0.1 to 1 A was observed to be 396 mV with a transient time of 175 μs. Thus, the proposed converter shows an improvement of 146 mV (36 %) in the voltage transient, i.e., transient accuracy.

Table I. Switching regulator parameters and operating conditions.

Parameter	Value	Parameter	Value
V_{IN}	3.3 V	V_O	5 ±5%
I_O	0.1-1 A	L	1-30 μH
C	20-350 μF	D (P-ch) R_{ON}	0.15 Ω
MNP1 (N-ch) R_{ON}	0.1 Ω	MPP3 (P-ch) R_{ON}	0.5 Ω
K_I	4	K_V	1
C_1	200 pF	I_1	5 μA
Q_1, Q_3 hysteresis H_V	24 mV	Q_2 hysteresis H_S	100 mV
M	0.24	R_S	0.5 Ω
Simulator	Spectre	Technology	0.5μ CMOS

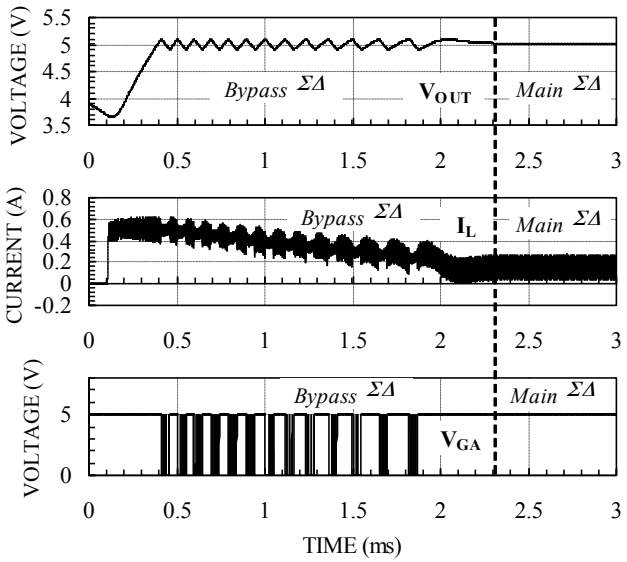

Fig. 7. Steady-state waveforms of the proposed bypass ΣΔ converter solution for L = 5 μH, C = 47 μF, and I_O = 0.1 A.

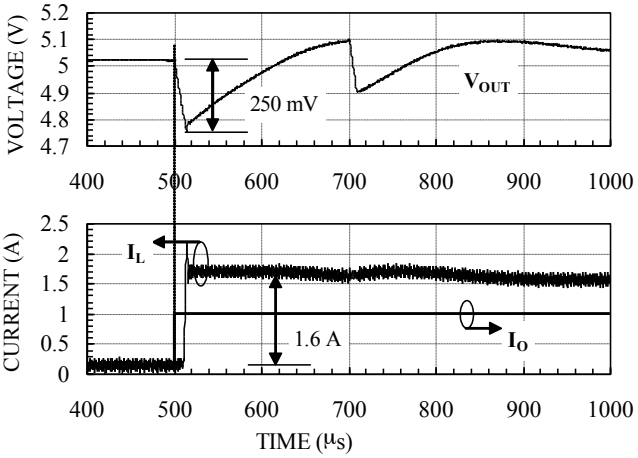

Fig. 8. Load-step transient waveforms of the proposed circuit for L = 5 μH, C = 47 μF, and I_O = 0.1 - 1 A.

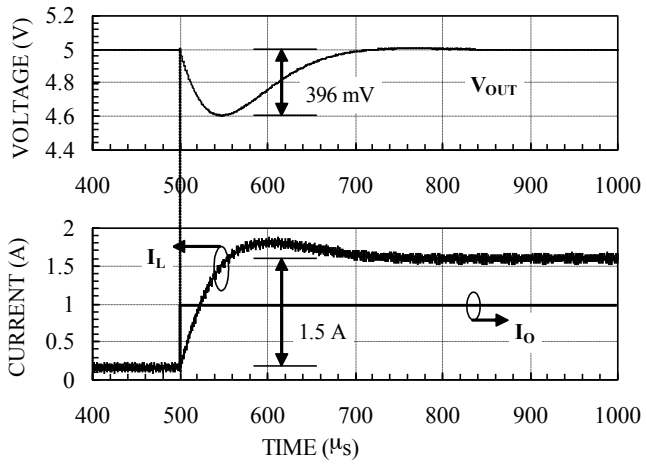

Fig. 9. Load-step transient waveforms of the single ΣΔ loop converter for L = 5 μH, C = 47 μF, and I_O = 0.1 - 1 A.

For a complete analysis, the voltage transient for the same load step was determined for the two converters as a function of filter inductance L, keeping every other parameter the same as before. The results of this analysis are shown in the plot shown in Fig. 10. The improvement in the voltage transient response is evident (up to 50 % at 1 μH), especially at lower inductance values. As the inductor and the LPF poles approach each other close to the maximum designed value (30 μH), the ΣΔ converter response approaches that of the proposed technique. Maximum improvement (50 %) in the proposed technique is seen at inductor values (1 μH) away from the highest designed filter inductor value.

Table II compares the three ΣΔ control schemes discussed in this paper, based on load transient response, LC filter compliance, output voltage ripple, power efficiency, and circuit complexity. While the proposed strategy has similar LC filter compliance as the other two techniques, it has lower output voltage ripple and higher power efficiency than the dual ΣΔ loop circuit. Concurrently, its transient response is significantly faster than that of the single ΣΔ loop technique designed for wide LC filter compliance. These benefits are achieved at the cost of system complexity.

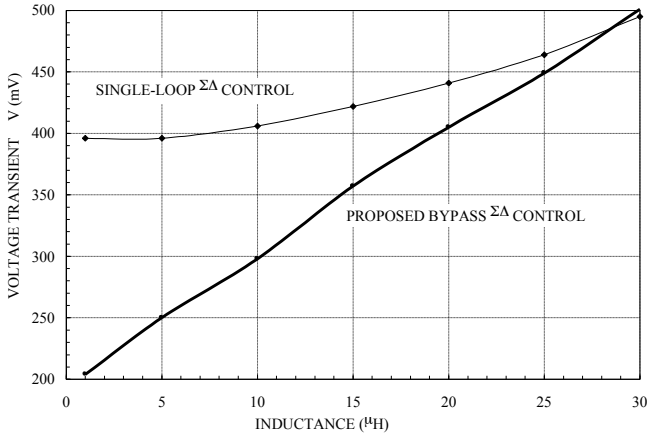

Fig. 10. Transient output voltage variation as a function of filter L in response to a load-current step for the single ΣΔ loop and the proposed bypass scheme with C = 47 uF and I_O = 0.1 to 1 A.

Table II. Comparative evaluation of fast LC compliant converters.

Parameter	Single ΣΔ Loop	Dual ΣΔ Loop	Proposed Bypass ΣΔ Loop
Transient Response (Voltage Variation)	Slow (396 mV)	Fast (250 mV)	**Fast (250 mV)**
LC Filter Compliance (see Table I)	High	High	**High**
Steady-State Output Voltage Ripple	± 0.2 %	± 2 %	**± 0.2 %**
Efficiency	High	Medium	**High**
Complexity	**Low**	Medium	High

V. CONCLUSION

A new control scheme was proposed for boost DC-DC converters, which, while giving stable response without using a frequency compensation circuit, displays significant advantages over current state-of-the-art techniques, viz., single ΣΔ loop (sliding-mode) control in terms of load transient response (up to 50 % improvement in ΔV transient). Simultaneously, low output voltage ripple (± 0.2 %) was achieved without any undue reduction in power efficiency or LC compliance, unlike other techniques reported in literature. The proposed technique thus decouples the conflicting requirements of high relative stability and fast transient response in boost DC-DC converters, enabling an optimal, almost fully integrated solution, except the passive LC filter.

V. REFERENCES

[1] B. Schaffer, "Internal compensation – boon or bane?," *Unitrode Design Seminar SEM 1400*, Texas Instruments, Dallas, TX, 2001.

[2] P. Krein (1998), *Elements of Power Electronics*, ISBN: 0195117018, Oxford University Press.

[3] R. Erickson (1997), *Fundamentals of Power Electronics*, 1st ed., New York: Chapman & Hall.

[4] R. Venkataramanan, A. Sabanovic and S. Cuk, "Sliding mode control of DC-to-DC converters," *IEEE International Conference on Industrial Electronics, Control and Instrumentation,* vol. 1, 1985, pp. 251-258.

[5] P. Mattavelli, L. Rossetto, G. Spiazzi, "Small-signal analysis of DC-DC converters with sliding mode control," *IEEE Transactions on Power Electronics*, vol. 12, No. 1, 1997, pp. 96-102.

[6] D. Biel, F. Guinjoan, E. Fossas, and J. Chavarria, "Sliding-Mode control design of a boost–buck switching converter for AC signal generation," *IEEE Transactions on Circuits and Systems-I*, vol. 51, No. 8, 2004, pp. 1539-1531.

[7] H. Sira-Ramírez, "Sliding mode-Δ modulation control of a buck converter," *IEEE Conference on Decision and Control*, vol. 3, 2003, pp. 2999-3004.

[8] N. Keskar and G.A. Rincón-Mora, "Self-Stabilizing, hysteretic, boost DC-DC converter," *The 30th Annual Conference of the IEEE Industrial Electronics Society, IECON 2004*, Nov 2004, TA3-4.

[9] G.A. Rincón-Mora, "Self-Oscillating DC-DC converters: From the Ground up," *IEEE Power Electronics Specialists Conference Tutorial*, 2001.

[10] R. Miftakhutdinov, "Analysis of synchronous buck converter with hysteretic controller at high slew-rate load current transients," *High Frequency Power Conversion Conference*, 1999, pp. 55-69.

[11] B.P. Schweitzer and A.B. Rosenstein, "Free running - switching mode regulator: analysis and design," *IEEE Transactions on Aerospace*, vol. AS-2, 1964, pp. 1171-1180.

[12] H.P. Forghani-zadeh and G.A. Rincón-Mora, "Current-sensing techniques for DC-DC converters," *Midwest Symposium on Circuits and Systems*, 2002, vol. 2, pp. II-577-II-580.