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1.4. Stability

A. Gain Objective

The principal aim of a feedback loop is to set an s_0 that is a reverse β_{FB} translation of s_i 's mirrored reflection. For A_{CL} to follow this translation, $1/\beta_{FB}$ should be lower than A_{FW} . But since gain is another goal, $1/\beta_{FB}$ should be one or greater. So in practice, A_{FW} is usually higher than $1/\beta_{FB}$ across frequencies of interest and β_{FB} is lower than or equal to 1 or 0 dB.

B. Stability Criterion

High A_{LG} is desirable in feedback systems because amplifying s_E reduces the mismatch between s_I and s_{FB} . Translating s_0 to s_{FB} , comparing s_{FB} to s_I , and amplifying the resulting s_E so this A_{LG} is high and s_0 is accurate usually requires two or more stages. Since each stage incorporates one or more poles, finding two or more poles in A_{LG} is not uncommon.

In Fig. 5, to cite an example, A_{LG} 's zero- or low-frequency gain A_{LG0} is well above 0 dB. A_{LG} falls 20 dB per decade after p_1 and another 20 dB per decade after p_2 . A_{LG} crosses 0 dB at a unity-gain frequency f_{0dB} that is higher than p_1 and p_2 . Since each pole reduces phase shift up to 90° , $\angle A_{LG}$ reaches -180° (at the inversion frequency f_{180°) before A_{LG} crosses 0 dB.

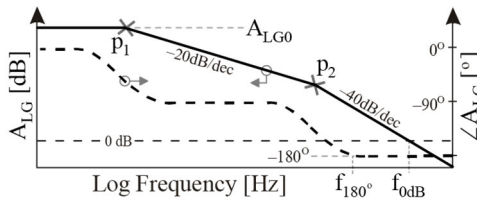


Fig. 5. Unstable loop-gain response.

Since A_{LG} inverts with -180° past f_{180° , A_{LG} is -1 at f_{0dB} . With this much phase shift, positive feedback peaks A_{CL} at f_{0dB} towards infinity:

$$A_{CL} = A_{FW} \parallel \frac{1}{\beta_{FB}} = \frac{A_{FW}}{1 + A_{LG}} \Big|_{A_{LG} = -1 \angle 180^\circ} = \frac{A_{FW}}{1 - 1} \rightarrow \infty. \quad (8)$$

Since A_V 's R_{IN} is very high, β_{FB} is the v_O fraction that R_2 sets across R_1 :

$$\beta_{FB} \equiv \frac{v_{FB}}{v_O} \approx \frac{R_1}{R_1 + R_2}. \quad (20)$$

So A_{LG} is $A_{FW}\beta_{FB}$ and A_{LG} reaches 0 dB at $A_{LG0}p_A$ or $A_{FW0}\beta_{FB}p_A$:

$$A_{LG} = A_{FW}\beta_{FB} \approx \left(\frac{A_{V0}}{1 + s/2\pi p_A} \right) \left(\frac{R_1}{R_1 + R_2} \right) \quad (21)$$

$$f_{0dB} \approx A_{LG0}p_A = A_{FW0}\beta_{FB}p_A \approx A_{V0} \left(\frac{R_1}{R_1 + R_2} \right) p_A. \quad (22)$$

And the voltage gain A_{VO} to v_O is A_{CL} 's $A_{V0} \parallel 1/\beta_{FB}$ up to f_{0dB} :

$$A_{VO} \equiv \frac{v_O}{v_{IN}} = A_{FW} \parallel \frac{1}{\beta_{FB}} \approx \left(A_{V0} \parallel \frac{R_1 + R_2}{R_1} \right) \left(\frac{1}{1 + s/2\pi f_{0dB}} \right), \quad (23)$$

which reduces to $1/\beta_{FB}$'s $(R_1 + R_2)/R_1$ up to f_{0dB} when A_{FW} 's A_{V0} is much greater than this $1/\beta_{FB}$.

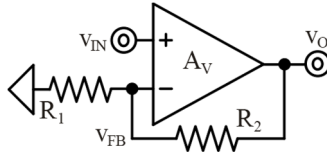


Fig. 15. Non-inverting (voltage-mixed) op amp.

Example 1: Determine A_{FW0} , β_{FB} , A_{LG0} , f_{0dB} , A_{VO0} , and $f_{CL(BW)}$ when A_{V0} is 100 V/V, p_A is 10 kHz, R_1 is 10 k Ω , and R_2 is 90 k Ω .

Solution:

$$A_{FW0} \approx A_{V0} = 100 \text{ V/V}$$

$$\beta_{FB} \approx \frac{R_1}{R_1 + R_2} = \frac{10k}{10k + 90k} = 100 \text{ mV/V}$$

$$A_{LG0} = A_{FW0}\beta_{FB} \approx (100)(100m) = 10 \text{ V/V}$$

$$f_{0dB} \approx A_{LG0}p_A \approx (10)(10k) = 100 \text{ kHz}$$

phase from shifting 180°. This way, A_{LG} follows A_S up to p_1 and continues to fall after z_{S1} and z_{S2} in A_S counter the effects of p_1 and p_2 in A_{LG} .

Parasitic poles in A_S eventually limit A_S 's bandwidth. So after z_{S1} and z_{S2} , A_S flattens with p_{S2} and falls with p_{S3} . Although p_{S2} and p_{S3} are not always apart, only one of these poles can be close to f_{0dB} for stability.

3.2. Amplifier Translations

An op amp can add p_{S1} . This op amp, however, cannot be *any* op amp. This is because the low-frequency gain A_{S0} and p_{S1} that A_{V0} and p_A set should establish an f_{0dB} that keeps the feedback system stable:

$$A_S \approx \frac{A_{V0}}{1 + s/2\pi p_A}. \quad (36)$$

The OTAs in Fig. 22 can also add p_{S1} . A_{S0} is the gain that A_G sets across R_F . In the first implementation, A_S falls past p_F when C_F shunts R_F :

$$A_S \approx A_G \left(R_F \parallel \frac{1}{sC_F} \right) = \frac{A_G R_F}{1 + sR_F C_F} = \frac{A_G R_F}{1 + s/2\pi p_F}. \quad (37)$$

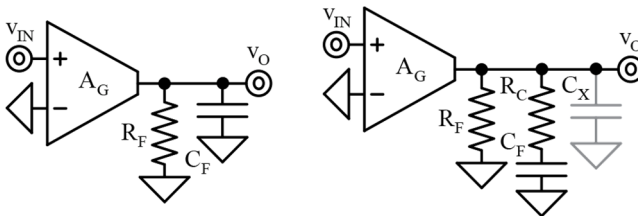


Fig. 22. Dominant-pole and pole-zero OTAs.

Current-limiting C_F with R_C adds z_{S1} . With R_C , A_S falls past p_C when C_F shunts R_C and R_F before parasitic capacitance C_X at v_O shunts R_F . p_C eventually fades past z_{CX} when C_F shorts with respect to R_C . Once shorted, A_S flattens to $A_G(R_F \parallel R_C)$ and later falls past p_O when C_X shunts $R_F \parallel R_C$:

$$\begin{aligned} A_S &= A_G \left[R_F \parallel (Z_F + R_C) \parallel Z_X \right] \\ &= \frac{A_G R_F (1 + sC_F R_C)}{s^2 R_C C_F R_F C_X + s \left[(R_F + R_C) C_F + R_F C_X \right] + 1} \end{aligned}$$

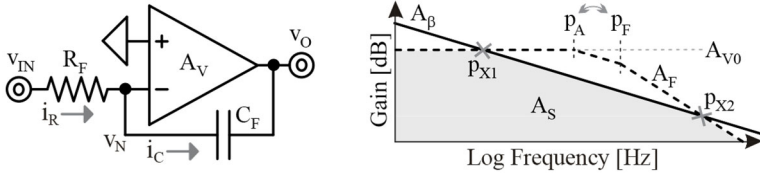


Fig. 31. Dominant-pole inverting mixed translation.

A_S follows A_F 's A_{V0} until A_β drops below A_{V0} at p_{X1} . With two poles in A_F and one in A_β , A_F falls faster than A_β . As a result, A_S falls with A_β past p_{X1} until A_F falls below A_β at p_{X2} . This way, A_{S0} is $-A_{V0}$, p_{S1} is p_{X1} , and p_{S2} is p_{X2} , but only when A_β 's projection to p_{X1} precedes p_A and p_F and A_F 's projection to p_{X2} exceeds p_{X1} :

$$|A_\beta| \approx \frac{1}{sR_F C_F} \Big|_{f_o \geq \frac{1}{2\pi A_{V0} R_F C_F} = \frac{p_F}{A_{V0}} \approx p_{X1}} \leq |A_F|_{f_o < p_A} \approx A_{V0}, \quad (65)$$

$$|A_F|_{f_o > p_A, p_F} \approx \frac{A_{V0} p_A p_F}{f_o^2} \Big|_{f_o \geq A_{V0} p_A \approx p_{X2}} \leq |A_\beta| = \frac{p_F}{f_o}, \quad (66)$$

$$A_S = A_F \parallel A_\beta \approx \frac{-A_{V0}}{(1 + s/2\pi p_{X1})(1 + s/2\pi p_{X2})}. \quad (67)$$

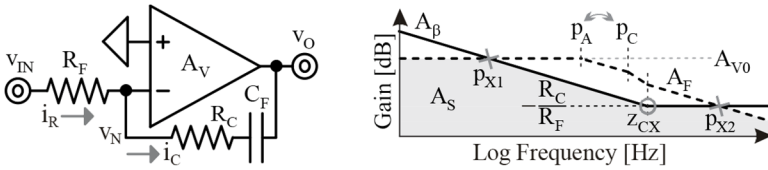


Fig. 32. Pole-zero inverting mixed translation.

Current-limiting C_F with R_C in Fig. 32 reverses C_F 's pole in A_F and A_β . So A_F starts with $-A_{V0}$, A_F falls past A_V 's p_A and p_C when C_F shunts R_C and R_F , and z_{CX} reverses p_C when R_C current-limits C_F . A_β falls as C_F shorts and flattens to $-R_C/R_F$ past z_{CX} when C_F shorts with respect to R_C :

$$A_F \approx \left(\frac{R_C + Z_C}{R_F + R_C + Z_C} \right) (-A_V) = \frac{-A_{V0} (1 + s/2\pi z_{CX})}{(1 + s/2\pi p_A)(1 + s/2\pi p_C)} \quad (68)$$

energize and drain L_X . The *duty-cycled inductance* L_{DO} is a d_{DO} translation of L_X with an R_L/D_{DO} that is usually negligible in light of R_{LD} . So the static components of d_{DO} , v_E , and v_D set L_{DO} in Fig. 36 to L_X/D_{DO}^2 and A_{SL} to

$$A_{SL(\text{CCM})} \equiv \frac{v_o}{d_e'} \approx \frac{(V_E + V_D)(1 + s/2\pi z_C)(1 - s/2\pi z_{DO})}{D_{DO} \left[(s/2\pi p_{LC})^2 + s/2\pi p_{LC} Q_{LC} + 1 \right] (1 + s/2\pi p_{SW})}. \quad (81)$$

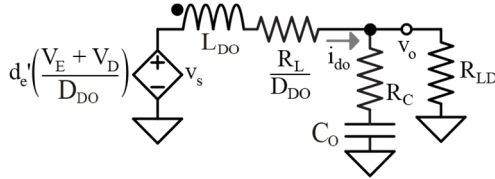


Fig. 36. Small-signal model of the switched inductor in CCM.

This gain drops as L_X opens with frequency because L_X feeds v_o less current. A_{SL} also falls as C_o shorts and steers current away from v_o . The resulting *inductor* and *capacitor poles* p_L and p_C appear together as a double pole p_{LC} at the *transitional LC frequency* f_{LC} when L_{DO} 's impedance sL_{DO} overcomes C_o 's $1/sC_o$. p_C eventually fades past z_C when the *capacitor resistance* R_C current-limits C_o .

Duty-cycled outputs connect L_X to v_o only when draining L_X . So when the *switching frequency* f_{SW} is constant, extending t_E shortens L_X 's *drain time* t_D . Reducing drain current this way produces an inverting (out-of-phase) zero when the loss outpaces the gain. This *duty-cycled zero* z_{DO} normally appears above p_{LC} , but not by far. When present, z_{DO} is usually below p_{SW} .

p_{LC} is challenging because it shifts phase 180° and peaks the gain. Since L_{DO} 's and C_o 's impedances cancel at f_{LC} , *inductor resistance* R_L and R_C impose a *series resistance* R_S that current-limits this peak. R_{LD} dampens it below this level because R_{LD} adds to the resistance that limits the LC current. But since R_L and R_C are usually low and R_{LD} is variable,

4.4. Current Mode

One way of eliminating p_{LC} is by regulating i_L . This way, the feedback translation that determines i_L is largely independent of sL_X . Removing this dependence to sL_X eliminates the LC interaction that produces p_{LC} .

A. Current Loop

A_{IE} , the PWM, the switched inductor, and β_{IFB} in Fig. 39 close an inverting feedback loop that sets i_L . A_{IE} senses and amplifies the error that adjusts d_E' and i_L so v_{IFB} nears v_{EO} . This way, i_L is a reverse β_{IFB} translation of v_{EO} 's mirrored reflection, which is independent of L_X 's impedance sL_X :

$$i_L = \frac{v_{IFB}}{\beta_{IFB}} \approx \frac{v_{EO}}{\beta_{IFB}}. \quad (85)$$

This is like removing L_X from the circuit.

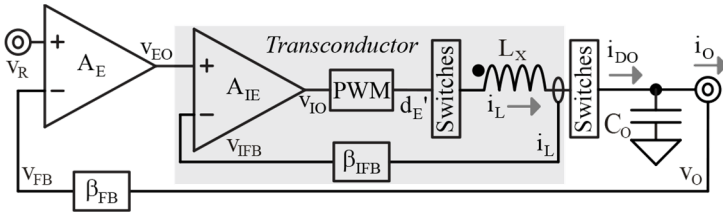


Fig. 39. Current-mode voltage controller.

B. Loop Gain

When the forward gain A_{IF} surpasses the feedback translation $A_{I\beta}$, the gain A_G to i_L follows $A_{I\beta}$'s $1/\beta_{IFB}$ up to the p_G that the loop's f_{i0dB} sets:

$$A_G \equiv \frac{i_L}{v_{EO}} = A_{IF} \parallel A_{I\beta} \approx \frac{1/\beta_{IFB}}{(1 + s/2\pi p_G)(1 + s/2\pi p_{SW})}. \quad (86)$$

A_G drops faster past p_{SW} when f_o surpasses f_{SW} . This β_{IFB} is usually constant. So the loop that sets i_L in Fig. 39 is basically a bandwidth-limited transconductor that d_{DO} in Fig. 40 duty-cycles.

A_{LG} is the gain across β_{FB} , A_E , A_G , and d_{DO} into C_O with R_C and R_{LD} . A_{LG} starts with $A_{E0}A_{G0}D_{DO}R_{LD}\beta_{FB}$. A_{LG} falls past p_G , p_{CP} , and p_{SW} when

$A_{IF}A_{PWM}A_{IL}$ is the part of A_{ILG} that determines feedback accuracy. This is because A_G follows $A_{I\beta}$ to the extent A_{IF} 's $A_{IE}A_{PWM}A_{IL}$ exceeds $A_{I\beta}$, which is to say, A_G approaches $1/\beta_{IFB}$ when A_{IF} increases. In other words, regulation accuracy scales with A_{IF} .

5.3. Inherent Stability

As a stabilizer, the aim of A_{IE} is to ensure A_{ILG} reaches f_{10dB} with less than 180° of phase shift. But since A_{IL} 's z_{CP} already recovers 90° of the 180° that p_{LC} loses, A_{IE} 's role can be to increase gain, and that way, extend f_{10dB} . But for f_{10dB} to add no more than one pole p_G , f_{10dB} should be a decade or more below A_{IE} 's bandwidth p_{IE1} and f_{SW} :

$$A_{ILG}|_{f_o > p_{LC}} \approx \frac{A_{ILG0} p_{LC}^2}{z_{CP} f_o} \Big|_{f_o = A_{ILG0} \left(\frac{p_{LC}^2}{z_{CP}} \right) \approx f_{10dB} = p_G \leq \frac{p_{IE1}}{10}, \frac{f_{SW}}{10}} = 1. \quad (96)$$

Since A_{ILG} rises and falls to 0 dB, A_{ILG} usually starts low, which means A_{IF0} is also low. So A_{IF} in Fig. 44 starts low, climbs past z_{CP} , falls past p_{LC} , and falls faster past p_{SW} . Although not always, A_{IF0} 's $A_{IE0}A_{PWM0}A_{IL0}$ is often lower than $A_{I\beta}$'s $1/\beta_{IFB}$. So A_G often starts with A_{IF0} .

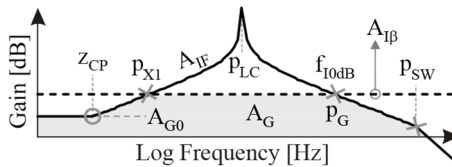


Fig. 44. Inherent transconductance in CCM.

A_G climbs with A_{IF} past z_{CP} until A_{IF} surpasses $A_{I\beta}$. This z_{CP} is usually low because C_O is high and R_{LD} is moderate. Since A_{IF} is the part of A_{ILG} that excludes β_{IFB} , A_{ILG0} is below 1 when A_{IF0} surpasses $1/\beta_{IFB}$. So A_{IF} crosses $A_{I\beta}$ at a p_{X1} that is $1/A_{ILG0}$ times greater than z_{CP} :

$$A_{IF}|_{f_o < p_{LC}} = A_{IE0}A_{PWM0}A_{IL0} \left(\frac{f_o}{z_{CP}} \right) \Big|_{f_o \geq \frac{z_{CP}}{A_{ILG0}} \approx p_{X1} > z_{CP}} \geq A_{I\beta} \approx \frac{1}{\beta_{IFB}}. \quad (97)$$

$$f_{10dB} \approx A_{ILG0} \left(\frac{p_{CS}}{z_{CP}} \right) p_{IE1} = (100) \left(\frac{120}{64} \right) p_{IE1} \equiv \frac{f_{SW}}{10} = 100 \text{ kHz}$$

$$\therefore p_{IE1} = 530 \text{ Hz} \quad \text{and} \quad p_{IE2} \geq f_{10dB} = 100 \text{ kHz}$$

$$A_{G0} = (A_{IE0} A_{PWM0} A_{IL0}) \parallel \frac{1}{\beta_{IFB}}$$

$$\approx [(190)(2)(140m)] \parallel 1 = 980 \text{ mA/V}$$

6. Digital Control

Feedback controllers use the voltage or current they sense to generate a pulsing command. From this perspective, feedback controllers are *analog-digital converters* (ADC). Mostly *analog controllers* mix, amplify, and stabilize the feedback system in the analog domain and mostly *digital controllers* in the digital domain.

Conventional ADCs digitize the voltage or current that digital controllers sense. Clocked *digital-signal processors* (DSP) use this digital word to mix, amplify, stabilize, and drive the switched inductor. Like analog controllers, digital controllers set loop gains that reach 0 dB with less than 180° of phase, if possible, at the highest manageable f_{0dB} .

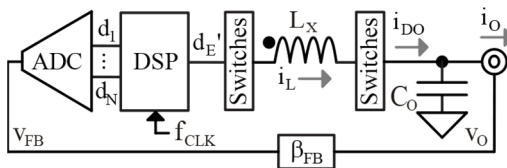


Fig. 47. Digital voltage-mode voltage controller.

6.1. Voltage Controller

Voltage-mode voltage controllers translate v_o in Fig. 47 to v_{FB} with β_{FB} and v_{FB} into an N-bit digital word d_{1-N} with ADCs. DSPs mix and compare this word d_{1-N} with a reference word d_R and use the difference to output the pulsing command $d_{E'}$ that adjusts i_L . This way, DSPs sense and amplify