Answers to End-of-Chapter Questions

from ***Analog IC Design with Low-Dropout Regulators***, 2nd Edition

By Gabriel Alfonso Rincón-Mora, Ph.D.

Chapter 1 Answers:

1. *Small signals only.*

2. *High power-conversion efficiency.*

3. *All of these (Noisier*, *slower*, and *more complex)*.

4. *Switched* and *linear.*

5. *Input voltage*, *output voltage*, *load current*, and *quiescent ground current.*

6. *Profound.*

7. *Nickel–cadmium* and *nickel–metal–hydride batteries.*

8. *Less.*

9. *Shorter* and *lower.*

10. *Solar light.*

11. *Validation only.*

12. *Unrealistically pessimistic.*

13. *All of these (wafer*, *wafers*, and *fabrication lots).*

Chapter 2 Answers:

1. *The reference voltage* v_{REF} *and the error amplifier's offset voltage* V_{OS} *across fabrication corners of the manufacturing process.*

2. *More accurate when loop gain is high.*

3. *The reference voltage* v_{REF} *and the error amplifier's offset voltage* V_{OS}.

4. *Steady-state variations.*

5. *Worse.*

6. *True.*

7. $\Delta v_{OUT} = \Delta v_{ESR} + \Delta v_C = \Delta i_{LOAD} R_{ESR} + \left(\frac{\Delta i_{LOAD}}{C_O}\right)\left(\frac{2.3}{2\pi f_{BW}}\right)$

$$= (15\ \text{mA})(250\ \text{m}\Omega) + \frac{(15\ \text{mA})(2.3)}{(1\ \mu\text{F})(2\pi)(0.5\ \text{MHz})} \approx 15\ \text{mV}$$

8. *Input and output voltages v_{IN} and v_{OUT}.*

9. $\eta_C = \frac{i_{LOAD} v_{OUT}}{i_{IN} v_{IN}} = \frac{(20\ \text{mA})(1.8\ \text{V})}{(20.4\ \text{mA})(3.6\ \text{V})} \approx 49\%$

10. $\eta_C = \frac{i_{LOAD} v_{OUT}}{i_{IN} v_{IN}} = \frac{(100\ \mu\text{A})(1.8\ \text{V})}{(140\ \mu\text{A})(3.6\ \text{V})} \approx 36\%$

11. *Switch-on resistance R_{ON}.*

12. *False, because board resistances are outside the regulating loop.*

13. *False, because the regulating effects of feedback diminish when the regulator is in the dropout region.*

14. *Low-power internally compensated low-dropout (LDO) regulators with no off-chip capacitors.*

15. *Low-power output-compensated low-dropout (LDO) regulators with an off-chip output capacitor.*

16. *Error amplifier, power transistor, feedback factor, reference voltage, and housekeeping functions like protection and bias blocks.*

Chapter 3 Answers:

1. *Width, length, and choice of material.*

2. *Contact resistances and a capacitor to the substrate.*

3. *Large resistor areas, close arrays, similarly oriented devices, common-centroid structures, interdigitation, cross-coupling, and dummy devices around the periphery of the array.*

4. *Top plate.*

5. *Contact and series resistances and a capacitor to the substrate.*

6. *Diffusion.*

7. *Lower voltages.*

8. *How much of the emitter current is the result of emitter carriers diffusing into the base.*

9. *How many of the emitter carriers diffused into the base reach the collector.*

10. *No.*

11. *No.*

12. *Extends depletion region, which ultimately shortens base width.*

13. *Magnifies base-width modulation.*

14. $g_m = \frac{I_C}{V_t} = \frac{10\ \mu A}{26\ mV} = 385\ \mu S$, $r_\pi = \frac{\beta_0}{g_m} = \frac{75\ A/A}{385\ \mu S} = 195\ k\Omega$, and $r_o = \frac{V_A}{I_C} = \frac{50\ V}{10\ \mu A} = 5\ M\Omega$.

15. *Accumulation, because a positive voltage accumulates electrons underneath the gate.*

16. *Negative.*

17. *Diffusion (i.e., concentration gradients).*

18. *Lowers.*

19. *Oxide capacitances from overlapping the gate over the source diffusion and across half the channel.*

20. *Oxide capacitances from overlapping the gate over the source diffusion and across the channel, which effectively extends two-thirds of the "drawn" channel length L.*

21. *No.*

22. *No.*

23. *Mega-ohms.*

24. *Negative.*

25. *Contact and diffusion resistances, gate–source and gate–drain capacitances, and maybe a diode to the substrate.*

26. *JFETs generate less 1/f noise.*

27. *±20%.*

28. *Resistors.*

29. *BJTs.*

Chapter 4 Answers:

1. *Short the output terminal to ground.*

2. *Establish poles that shunt energy away from propagating signals and therefore reduce gain.*

3. *To introduce right-half-plane zeros that invert the output, help establish poles at the input and output that shunt energy away from input and output signals and therefore reduce gain, and if across a voltage amplifier, introduce a Miller-multiplied capacitance to the input.*

4. *To introduce left-half-plane zeros that recover phase and gain lost by poles.*

5. *To limit capacitor current and therefore offset and cancel the effects of the pole that the capacitor created in the first place with what amounts to a left-half-plane zero.*

6. *No, because they invert the polarity of signals at higher operating frequencies.*

7. *The resistances they shunt.*

8. *Gate and source terminals.*

9. *Common-emitter and common-source transconductors.*

10. *To lower the effective transconductance and raise the output resistance of the transistor.*

11. *As current buffers because currents into their inputs flow almost entirely out of their outputs.*

12. *High frequencies because input source resistances are usually low.*

13. *To lower the transconductance and raise the input resistance of the transistor, and as a result of the latter, also lower the input pole.*

14. *Yes, because base–emitter capacitors C_π feed-forward in-phase currents from input to output.*

15. *Emitter and source resistances at nearly $1/g_m$.*

16. *Base–emitter and bulk-effect resistances r_π and $1/g_{mb}$.*

17. *Emitter/source-degenerated collector/drain resistances at $g_m r_\pi r_o$, $g_m R_{DEG} r_o$, or higher.*

18. *Base–emitter and gate–source capacitors C_π and C_{GS}, the capacitive loads they establish, and nonparasitic capacitors added intentionally to the circuit.*

Chapter 5 Answers:

1. $$A_I = \frac{i_O}{i_{IN}} = \frac{4i_C}{i_{IN}} \approx \frac{4\left(\frac{i_{IN}}{5}\right)}{i_{IN}} = \frac{4}{5}$$

2. $$i_B \approx \frac{i_{IN}}{\beta_0} + \frac{i_O}{\beta_0} = \frac{10\ \mu A}{50} + \frac{(10\ \mu A)\left(\frac{4}{5}\right)}{50} = 360\ nA$$

3. $$A_{ERR} = \frac{A_{IDEAL} - A_{ACTUAL}}{A_{IDEAL}} = \frac{\left(\frac{4}{5}\right) - \left(\frac{4}{5}\right)\frac{\left(1+\frac{v_O}{V_A}\right)}{\left(1+\frac{v_{BE}}{V_A}\right)}}{\left(\frac{4}{5}\right)} = 1 - \frac{\left(1+\frac{5\ V}{50\ V}\right)}{\left(1+\frac{0.7\ V}{50\ V}\right)} \approx 8.5\%$$

4. *Raise the base–emitter voltage of the output transistor with a resistor in series with the base of the input transistor or connect the collector of the input transistor to the common base via a common-collector BJT or common-drain MOSFET follower.*

5. *By inserting voltage-correcting cascodes in series with the mirroring transistors, so the drain voltages of the mirroring transistors match.*

6. $2V_t$.

7. $V_{DS(SAT)}$.

8. *When neglecting common-mode signals and applying the positive half of the differential signal to the base of one transistor and the negative half to the base of the other.*

9. *By reducing the transconductance of the pair with, for example, source-degenerating resistors between the source terminals of the transistors.*

10. *Tail-current and differential-pair transistors.*

11. *The input common-mode voltage* v_{IC}, *one P-type MOSFET threshold voltage* v_{TP}, *and two P-type saturation voltages* $2V_{SD(SAT)}$.

12. *Bandwidth and slew rate.*

13. *Balance bias currents, fold one differential current into the other, source the difference of the currents into one output, and load the resulting current so the current can establish a voltage, all of which convert a double-ended differential input voltage into a single-ended output voltage.*

14. *Output node.*

15. *Introduces a pole followed by an in-phase zero.*

16. *Introduces a zero followed by a pole.*

17. *Zero.*

18. *The zero and succeeding pole that the tail current produces, the zero that the mirror produces in the differential gain, and the zero that the mirror produces in the common-mode gain, the latter two of which do not match.*

19. *1/f and thermal noise.*

20. *Negative PSR is nearly 1 and positive PSR approaches infinity.*

21. *Current-folding and voltage-correcting cascodes* M_5, M_6, M_7, *and* M_8 *and tail-current transistor* M_T.

Chapter 6 Answers:

1. *Mixer, forward open-loop gain* A_{OL}, *sampler, and feedback factor* β_{FB}.

2. *In mirroring the mixed input, negative feedback opposes the effects of external forces.*

3. *To lower sensitivity.*

4. *To raise output impedance.*

5. *Voltage.*

6. *To raise input impedance.*

7. *Current.*

8. *To mask it.*

9. *Lower the corner frequency, which extends bandwidth.*

10. *Gain saturates near the extremes of the signal, when transistors approach their triode regions.*

11. *Drop a portion of the incoming voltage.*

12. *Steer output current away from the load.*

13. *Bases, emitters, gates, and sources when their opposing input terminals carry loop signals.*

14. *Bases, emitters, gates, and sources when their opposing input terminals do not carry loop signals.*

15. *Collectors, emitters, drains, and sources sample both small- and large-signal components of current.*

16. *By tracing the input terminal into the circuit and finding a T connection.*

17. *Ground input and output voltages.*

18. *Input and output currents should be zero, so the input current and the load should be absent.*

19. *Ground the input voltage being mixed.*

20. *Remove the input current.*

21.
$$A_{V.OL}\Big|_{i_o \equiv 0} \equiv \frac{v_{out}}{v_e} = A_V g_{m2}\left(R_{S1} \parallel r_{sd2}\right) \approx A_V g_{m2} R_{S1} \approx \frac{2A_V g_{m2}}{g_{m1}}$$

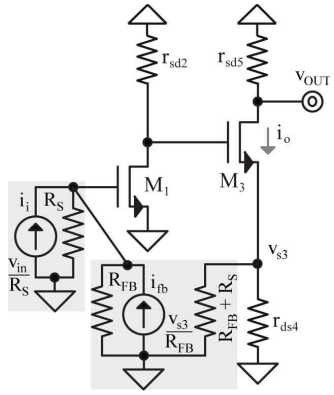
$$R_{S1} = \frac{r_{sd1} + r_{ds3}}{1 + g_{m1} r_{sd1}} \approx \frac{2}{g_{m1}}$$

$$\beta_{FB}\Big|_{v_{in} \equiv 0} \equiv \frac{v_{fb}}{v_{out}} = \frac{\left(\frac{v_{out}}{R_{S1}}\right) r_{sd3}}{v_{out}} \approx \frac{g_{m1} r_{sd3}}{2}$$

$$R_{I.OL} = R_{ID} + \left(r_{ds3} \parallel R_{D1}\right) \approx R_{ID} + r_{ds3} \to \infty$$

$$R_{O.OL}\Big|_{v_{in} \equiv 0} = R_{S1} \parallel r_{sd2} \approx R_{S1} \approx \frac{2}{g_{m1}}$$

22.



$$A_{I.OL}\big|_{v_{out}\equiv 0} \equiv \frac{i_o}{i_e} \approx \left(R_S \parallel R_{FB}\right)\left(-g_{m1}\right)\left(r_{ds1} \parallel r_{sd2}\right)\left\{\frac{g_{m3}}{1+g_{m3}\left[r_{ds4} \parallel \left(R_{FB}+R_S\right)\right]}\right\}$$

$$\beta_{FB}\big|_{i_i\equiv 0} \equiv \frac{i_{fb}}{i_o} = \left(\frac{v_{s3}}{i_o}\right)\left(\frac{i_{fb}}{v_{s3}}\right) = \left[r_{ds4} \parallel \left(R_{FB}+R_S\right)\right]\left(\frac{1}{R_{FB}}\right)$$

$$R_{I.OL} = R_S \parallel R_{FB}$$

$$R_{O.OL}\big|_{i_i\equiv 0} \approx r_{ds3} + \left[r_{ds4} \parallel \left(R_{FB}+R_S\right)\right] + g_{m3}r_{ds3}\left[r_{ds4} \parallel \left(R_{FB}+R_S\right)\right]$$

$$\frac{v_{out}}{v_{in}} = \left(\frac{i_i}{v_{in}}\right)\left(\frac{i_o}{i_i}\right)\left(\frac{v_{out}}{i_o}\right) = \left(\frac{1}{R_S}\right)A_{I.CL}\left(r_{sd5} \parallel R_{O.CL}\right) \approx \left(\frac{1}{R_S}\right)\left(\frac{1}{\beta_{FB}}\right)\left\{r_{sd5} \parallel \left[R_{O.OL}\left(1+A_{I.OL}\beta_{FB}\right)\right]\right\}$$

23. *The loop gain should reach the unity-gain frequency with less than 180° of phase shift.*

24. *Add capacitance to the node that establishes the pole.*

25. *Insert a Miller capacitor across the inverting gain stage that separates the two poles.*

26. *Current-limit a shunt capacitor with a series resistor or bypass a circuit with an in-phase capacitor or circuit.*

27. *Current-limit the capacitor with a series resistor.*

28. *Buffer the output voltage that feeds the capacitor or buffer the capacitor current that feeds the input.*

29. *True.*

Chapter 7 Answers:

1. *Diode voltages, breakdown voltages, and gate–source voltages*.

2. *Diode voltages*.

3. *PTAT refers to parameters that are proportional to absolute temperature.*

4. *Thermal voltage V_t.*

5. *The circuit generates a PTAT voltage that is largely independent of the supply without requiring a startup circuit.*

6. *The exponential dependence of MOS drain currents o gate–source voltages in subthreshold*.

7. *Base-current and collector- and drain-voltage mismatches between the diodes or transistors whose voltage difference establishes the circuit's PTAT current and between the transistors that mirror the current*.

8. *By inserting a feedback amplifier into the diode-connecting loop that balances base currents and series-mixes the voltages across the mirror to ensure the voltages are equal.*

9. *Diode and MOS threshold voltages (MOS transconductance parameters also incorporate a CTAT component)*.

10. *A multiplied version of the thermal voltage* V_t*, which is PTAT, and one diode voltage* v_D*, which is CTAT*.

11. *T ln T*.

12. *By injecting a current that ensures one of the diode-connected transistors in the noninverting feedback path is never off*.

13. *By comparing the PTAT current that the cell generates to that of a pinched-channel resistor or a long- and narrow-channel JFET or PMOSFET*.

14. *When a short circuit diode-connects the mirroring transistor*.

15. *Adding capacitance to the high-impedance node in the diode-connecting loop, placing the PTAT-generating resistor* R_P *on the side of the diode or BJT that boosts the inverting loop gain or degenerates the noninverting counterpart, and low-pass filtering components in the noninverting feedback path.*

16. *By coupling noise present in the emitter or source to the corresponding base or gate, or vice versa*.

17. *They steer PTAT currents into a resistor to generate a PTAT voltage that, when connected in series with a diode voltage, which is CTAT, produces a temperature-compensated sum.*

18. *Adding a shunt-feedback loop that regulates the output opposes the effects of coupled noise.*

19. *Mismatches between diodes, mirroring transistors, and resistors; the initial tolerance of the diode voltage and resistors; and the mismatches that package stresses produce.*

20. *Because surrounding one diode with eight others in a three-by-three array yields a layout that is compact, modular, and with a common center of mass*.

21. *Because, although trimming one parameter at one temperature limits the amount of correction possible, trimming more than one parameter at more than one temperature is prohibitively expensive in a mass-production environment.*

Plus, untrimmed package-induced offsets in plastic packages negate the benefits of curvature correction, and trimming after the IC is packaged is, again, prohibitively expensive in a mass-production environment.

Chapter 8 Answers:

1. *Output capacitor C_O, bypass capacitor C_B, load capacitor C_L, the coupling capacitor C_P across the power pass transistor, and the input capacitance of the error amplifier C_{IE}.*

2. *Output capacitor C_O.*

3. *Feedback resistances R_{FB1} and R_{FB2}, load resistance R_L, and the resistance of the power pass transistor R_P.*

4. *Feedback resistances R_{FB1} and R_{FB2}.*

5. *Output capacitor C_O, bypass capacitor C_B, load capacitor C_L, pass-transistor capacitance C_P, feedback resistors R_{FB1} and R_{FB2}, load resistance R_L, and pass-transistor resistance R_P.*

6. *Output capacitor C_O and C_O's equivalent series resistance R_{ESR}.*

7. *Bypass capacitor C_B, load capacitance C_L, pass-transistor capacitance C_P, and C_O's equivalent series resistance R_{ESR}.*

8. *A pole at the input of the error amplifier p_{FB}, a low- to moderate-frequency pole in the error amplifier p_E, and parasitic poles in the error amplifier.*

9. *Since f_{0dB} shifts with the gain–bandwidth product, f_{0dB} shifts with the square root of load current.*

10. *The ESR zero that R_{ESR} produces extends f_{0dB} to the extent that the output pole or the bypass pole that R_{ESR} also establishes allows.*

11. *Since high load current reduces output resistance and therefore raises the output pole, high gain, a low-frequency pole in the error amplifier, and no ESR zero, which results from low R_{ESR}, shift the phase across the loop the most before reaching f_{0dB}.*

12. *Achieving high loop gain and extending bandwidth when the output pole is low and the ESR zero is high, which results when R_{ESR} is low.*

13. *f_{0dB} shifts with the gain–bandwidth product, except gain variations cancel those of bandwidth, so f_{0dB} does not shift with load current in Miller-compensated circuits.*

14. *BJTs, because their transconductance changes linearly with load current.*

15. *The diode-connected resistance from Miller compensation, output resistance, coupling capacitance, and if not designed properly, the transconductance of the power pass device.*

16. *The shunting resistance that feedback establishes and output, bypass, and load capacitances*.

17. *Noise-free signals.*

18. *Gate signals that reproduce supply noise*.

19. *By loading the differential stage with a P-type current mirror*.

20. *N-type mirrors*.

21. *The Miller capacitor diode-connects the P-type power transistor, so the impedance falls from* r_{sd} *and flattens to diode resistance* $1/g_m$.

22. *Shunt feedback*.

23. *High loop gain*.

24. *The lowest-frequency pole in the error amplifier*.

25. *Near and past the system's bandwidth* f_{0dB}.

26. *Output, bypass, and load capacitances*.

27. *Equivalent series resistance* R_{ESR} *and the coupling resistance and capacitance across the power pass device*.

28. *Output compensation*.

Chapter 9 Answers:

1. *P-type BJTs and MOSFETs*.

2. *PNP BJTs*.

3. *N-type BJTs and MOSFETs*.

4. *The base current that the buffer must source or sink for a power BJT to satisfy the load.*

5. *The source–gate or gate–source voltage that the buffer must establish for a power MOSFET to satisfy the load.*

6. *P-type transistors drop the lowest voltage and MOSFETs do not require gate current, so PMOSFETs tend to dissipate the least power.*

7. *A reverse-biased diode from the collector to the substrate.*

8. *Vertical BJTs from the emitter and collector terminals to the substrate.*

9. *Reverse-biased diodes from the source and drain terminals to the substrate.*

10. *Vertical BJTs from the source and drain terminals to the substrate with a base that is highly resistive.*

11. *Because de-biasing the well with stray currents can activate the parasitic vertical BJT between the source and substrate, and injecting current into the substrate this way produces noise and establishes possible latch-up conditions*.

12. *Including as many well contacts as possible, integrating well contacts into the source fingers of the transistor, and overlapping the well with a highly doped buried layer, if available*.

13. *Triangular*.

14. *Metal, semiconductor, bond-wire, and board-trace resistances, the latter of which is normally less dominant*.

15. *Common-drain/collector voltage followers*.

16. *Because they raise the dropout voltage of the BJT*.

17. *Native NMOSFETs and P-type followers, because they can shut power PFETs*.

18. *A P-type follower looped with shunt feedback to help sink base current on demand*.

19. *Accelerates the response, load-tracks the pole, and offsets load-regulation effects*.

20. *Compromises the feedback stability of the system*.

21. *Because the output pole of many P-type regulators is dominant, so the load shifts the unity-gain frequency, and with it, its requirements for the buffer. And since a load-tracking pole is only high on demand, quiescent current is only high when needed, and low otherwise*.

22. *Because a 1.2-V reference and the positive input-common-mode range requirements of a P-type differential pair limit the minimum supply that the circuit can tolerate, and a lower reference reduces its signal-to-noise ratio*.

23. *By folding differential currents into the mirror load*.

24. *N-type mirrors, because they cancel power-supply noise*.

25. *P-type mirrors, because they reproduce power-supply noise that a PMOSFET can then cancel as common-mode noise*.

26. *Nondegenerated transistors (in the differential pair, mirror load, and bias-current pair)*.

27. *Mismatched voltages across the mirror load*.

28. *As a load-dependent mismatch in voltages across the mirror load.*

Chapter 10 Answers:

1. *Low-dropout voltage, high output capacitance for better load-dump response, and high power-supply-rejection bandwidth*.

2. *Two low- to moderate-frequency poles*.

3. *Low-dropout voltage and low on- and off-chip capacitance for higher integration*.

4. *Poor load-dump response and low power-supply-rejection bandwidth*.

5. *High loop bandwidth for better load-dump response*.

6. *High-dropout voltage and low power-supply-rejection bandwidth*.

7. *To establish a PTAT voltage that compensates the CTAT tendencies of a diode or base–emitter voltage*.

8. *Bandgap conversion uses an external PTAT current to produce a PTAT voltage in the loop and bandgap integration incorporates the PTAT generator into the regulating loop*.

9. *Forward-bias the bulk–source junction slightly when load current is high to reduce the effective threshold voltage of the PMOSFET, or add a linear or nonlinear slave transistor and an accompanying loop to control it*.

10. *Accelerate the falling rate of the loop gain with respect to frequency with a pole and recover the phase lost by that pole with an in-phase zero before the loop gain drops to and below 1*.

11. *Sense and mirror a diminutive fraction of the output current into a resistor that is in series with the reference so that higher load currents raise the effective voltage of the reference*.

12. *Filters power-supply noise at and above the regulator's bandwidth for higher power-supply rejection*.

13. *The series resistance is in the conduction path, so it dissipates power, and to accommodate a lower resistance, filter capacitance must be high*.

14. *Higher overall dropout voltage and low power-supply rejection at and above the preregulator's bandwidth*.

15. *Decouples power-supply noise from the output across frequency: below, at, and above the regulator's bandwidth, so power-supply rejection is higher across frequency*.

16. *Higher overall dropout voltage and circuit complexity*.

17. *Because the loop that regulates the cascode transistor raises output resistance*.

18. *No, because the output resistance of a nonregulated cascode circuit is already high, and inserting a regulating loop complicates the circuit (i.e., adds risk)*.

Chapter 11 Answers:

1. *The circuit should neither require quiescent current nor introduce voltage drops in the power-conduction path*.

2. *Maximum output current is higher because the limit while the output is near its target is higher than the highest short-circuit limit (when the output is near ground)*.

3. *The shutdown temperature should not exceed the melting point of the package, which in the case of plastic packages is normally around 170°C.*

4. *Mechanical guides, tracks, or stops that force batteries to fit only as prescribed.*

5. *Mechanical solutions usually occupy more space.*

6. *Human-body, machine, and charged-device models.*

7. *0.2–5 kV.*

8. *Forward-biasing and reverse-breakdown diodes, resistor- and capacitor-coupled BJTs, and latching complementary BJTs.*

9. *The diode connected to the input supply channels positive ESD energy through the input supply into ground, instead of directly to ground, which is a lower-impedance plane.*

10. *With a variable resistor or a programmable current-source circuit.*

11. *How much the output voltage changes with steady-state variations in load current.*

12. *Falls, to exclude the effects of startup.*

13. *The time one must wait to allow voltages and currents to settle before recording a measurement.*

14. *To lower the PTAT component of the reference, the result of which is to reduce the slope (i.e., temperature coefficient) of the reference with respect to temperature.*

15. *Halfway across the operating temperature range: at* T_{MID}.

16. *Load-dump response.*

17. *Power-supply ripple rejection.*

18. *Because a function generator usually cannot supply or sink the current that the linear regulator can.*

19. *Output voltage, load or output current, input voltage, and ground or quiescent current, and of these, only ground or quiescent current is an open design variable.*

20. *The circuit rails and pushes one or more transistors into triode, so the gain across the feedback loop drops.*

21. *Because base or gate drive normally falls with lower supply voltages.*

22. *At the edge of the linear region, where the regulator just enters dropout.*

23. *By raising the targeted output voltage well above the headroom limit of the regulator and sweeping the input supply from its maximum specified value down to ground.*

24. *By subjecting the system to the fastest and widest rising and falling load dumps possible and noting whether or not the regulator recovers and settles its output back within regulation limits*.

25. *Because systems engage components on demand to preserve energy, so startup time is part of the system's response time.*