Sub-mW, DCM Switched-inductor Converter-efficiency Performance across Process Nodes

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Abstract: Shorter minimum channel lengths (L_{MIN}) increase efficiency because, while conduction losses E_R change minimally (since a lower supply voltage V_{DD} opposes the effects of a lower L_{MIN} in channel resistance R_{SW}), switching gate-drive losses E_G decrease with the square of reductions in L_{MIN} (since energy decreases with the square of V_{DD} and a higher C_{OX} opposes a lower L_{MIN}). Ultimately, however, the power source limits the extent to which L_{MIN} can reduce, because a 2.7 – 4.2-V Li Ion, for example, requires 5-V (0.7-µm) switches.

Validation Example: Consider a 0.5 V-to-1 V, sub-mW boost converter in discontinuous-conduction mode (DCM) that outputs fixed packets of energy per cycle E_O/cycle with a 50-µH, 5-Ω inductor L_O peaking at 4 mA ($i_{L(PK)}$) and switching with a 1-ns dead time. The circuit raises output current I_O by increasing switching frequency f_{SW}, where f_{SW} is nominally at 100 kHz. The selected aspect ratios for the switches W_{OPT}/L_{MIN} ensure E_R and E_G's sum remains minimal for every sample case. Quiescent current I_Q includes analog ($I_{Q(BW)}$), duty-cycled ($I_{Q(D)}$), and bias ($I_{Q(B)}$) components. With V_{TH} independently adjusted, oxide capacitance per unit area C_{OX} and, therefore, transconductance parameter K' increase with reductions in L_{MIN}, as the table shows, and breakdown voltages decrease.

L_{MIN} (Process)	0.18 µm		0.35 µm		0.5 µm	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
Max. V_{GS}, V_{DS}	1.8 V	–1.8 V	3.3 V	–3.3 V	4.5 V	–4.5 V
V_{TH}	0.65 V	–0.58 V	0.5 V	–0.6 V	0.86 V	–0.8 V
C_{OX} (T_{OX})	7.7 fF/µm² (45 Å)		4.5 fF/µm² (74 Å)		2.3 fF/µm² (151 Å)	
K'	135 µA/V²	35 µA/V²	89 µA/V²	33 µA/V²	47 µA/V²	12.5 µA/V²

Table 1. Process nodes.

Losses: With fixed packets of energy per cycle, P_R ($\propto i_{RMS}^2 R_{EQ}$) increases with f_{SW} and R_{SW} so, since a rise in K' (i.e., C_{OX}) offsets a fall in V_{DD}, $\mathbf{P_R \propto L_{MIN} f_{SW}/W}$. Since P_G is $(C_{OX}WL_{MIN})V_{DD}^2 f_{SW}$ and C_{OX} ($\propto 1/L_{MIN}$) cancels L_{MIN}, $\mathbf{P_G \propto W L_{MIN}^2 f_{SW}}$. To maintain bandwidth g_m/C_{EQ}, $I_{Q(BW)}$ should increase with L_{MIN}^2 to track C_{EQ} so $\mathbf{P_{Q(BW)} = I_{Q(BW)} V_{DD} \propto L_{MIN}^3}$. To keep losses low, other circuit blocks should only operate on demand, irrespective of L_{MIN}, so duty-cycled blocks dissipate $\mathbf{P_{Q(D)} = I_{Q(D)} D_O V_{DD} \propto L_{MIN}}$, and similarly, the bias generator consumes $\mathbf{P_{Q(B)} = I_{Q(B)} V_{DD} \propto L_{MIN}}$. There is an optimum W_{OPT}/L_{MIN} that balances (and minimizes aggregate losses) E_R and E_G, as Fig. 1a shows, so when using W_{OPT}, total losses $E_R + E_G + E_Q$ or E_L (in Fig. 1b) $\propto L_{MIN}$, but because E_G decreases faster than E_R with lower L_{MIN}'s, E_R's effects magnify at lower L_{MIN}'s and E_L's falling rate, as a result, decreases at lower L_{MIN}'s.

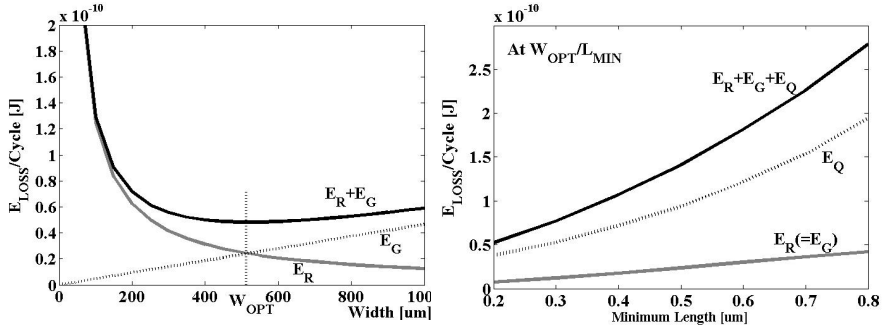

Fig. 1. Losses across (a) optimal channel width and (b) process node.

Simulation Results:

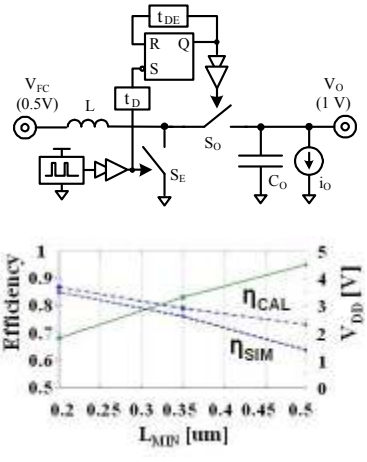

Fig. 2. (a) Circuit and (b) efficiency.

L_{MIN} (Process)		0.18 µm	0.35 µm	0.5 µm
Optimum Aspect Ratio W_{OPT}/L_{MIN}		3710	1250	1035
$E_{R(OPT)}$	R_{SW} (× 2 switches)	7.4 pJ with 1.7 Ω	15.0 pJ with 3.5 Ω	24.1 pJ with 5.6 Ω
	$R_{L(ESR)}$ (5 Ω)	21.3 pJ	21.3 pJ	21.3 pJ
$E_{G(OPT)}$	Gate Drive (× 2 switches)	7.4 pJ with 1.1 pF	15.0 pJ with 0.69 pF	24.1 pJ with 0.60 pF
	IV overlap	7.2 pJ	13.2 pJ	18 pJ
E_Q	t_{COND} (CMP_O & CMP_{AD} for 0.8 µs)	28.8 pJ	52.8 pJ	72 pJ
	t_{SW} (CMP_{MODE} & CLK_{GEN} for 10 µs)	36 pJ	66 pJ	90 pJ
Total Losses E_L		123 pJ	213.4 pJ	297.7 pJ
E_O/Cycle @ V_O = 1 V & $I_{L(PK)}$ = 4 mA		800 pJ	800 pJ	800 pJ
Efficiency	Calculated η_{CAL}	86.7 %	78.9 %	72.9 %
	Simulated η_{SIM}	**84.8 %**	**76.0 %**	**63.5 %**

Table 2. Efficiency performance.