CCM Switched-inductor Converter-efficiency Performance across Process Nodes

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Objective*:* To assess the impact of process technology on the (efficiency) performance of switched-inductor dc-dc converters.

Abstract*:* The table below compares the effects of decreasing L_{MIN} (i.e., increasing C_{OX} and therefore increasing K') on the loss mechanisms and resulting peak and full-load efficiencies η_P and η_{FL} of a 10-MHz buck converter in CCM. The comparison does not apply to (a) DCM because conduction losses P_C in DCM contribute less to the total losses and do not relate to I_{OUT} in the same way as in CCM or (b) speed because a lower L_{MIN} could increase f_{0dB} and f_{SW} (under hysteretic control) and therefore reduce output ripple.

Observations*:* P_C decreases with a lower L_{MIN} because a higher K' decreases R_{DSON}, but not as fast because the breakdown voltage V_{GSS} of a smaller L_{MIN} decreases gate-drive voltage V_{GST}, plus the total resistance includes the interconnecting metal and the inductor's ESR, which do not scale with L_{MIN}. Driver losses P_D decrease with a lower L_{MIN} because, while shoot-through losses P_{ST} increase because K' reduces R_{DSON}, larger gate-charge losses P_{GC} decrease more because reductions in L_{MIN} and transistor widths W overwhelm the rise in C_{OX}. Overlap and quiescent losses P_{OV} and P_Q do not scale with L_{MIN} (if f_{0dB} and f_{SW} remain unchanged).

Conclusions*:* With optimal W, because both P_C and P_D decrease with a lower L_{MIN}, η_P (which occurs at the edge of DCM) increases by roughly 1.32% for every 50% (i.e., 2×) reduction in L_{MIN} at 1.8 V, and less (by 0.85%) at higher voltages (at 3.6 V) because P_O is higher and losses therefore become a smaller fraction of η_P (which is why η_P is generally higher at higher voltages). A larger (non-optimal) W can improve η_{FL} (e.g., at 2 A), where P_C dominates, by 15% while lowering η_P by less than 2%. Interestingly, the optimal aspect ratio W/L used for each technology and output voltage combination resulted in nearly the same value in all cases.

Technology	0.18µm [1]		0.35µm [2]		0.6µm [3]	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
k' ($\mu C_{OX}/2$) ($\mu A/V^2$)	171	37	89	33	58	19
R_{DSON} (2.7V) (kΩ/sq.)	-	-	4.6	16	6.6	21
R_{DSON} (4.2V) (kΩ/sq.)	3.3 (@1.8V)	13 (@1.8V)	4.1 (@3.3V)	13 (@3.3V)	5.2	15
C_{OX} ($fF/\mu m^2$)	8.4	8.4	4.5	4.5	2.4	2.4
Nom. Voltage (Thick Ox.)	1.8V (3.3V)	1.8V (3.3V)	3.3V (5V)	3.3V (5V)	5V	5V

Technology		0.18µm (A) [1]		0.35µm (A) [2]		0.6µm (B) [3]	
Efficiency (E)	P_{OV}	100%		100%		100% (6.2mW at 0.22A)	
	P_C (D)	70%		83%		100% (23mW at 0.22A)	
	R_{SW} (C)	71%	77%	85%	86%	100% (259mΩ)	100% (559mΩ)
	P_D (F)	59%		77%		100% (15.3mW)	
	P_{ST} (G)	148%		121%		100% (2.9mW)	
	P_{GC}	38%		66%		100% (12.5mW)	
	P_Q	100%		100%		100% (4.2mW)	
	P_{LEAK}	Neglected		Neglected		Neglected	
	Peak (1.8V)	91.50%		90.43%		89.11%	
	(W/L)	3.97E+04		3.40E+04		3.27E+04	
	Peak (3.3V)	94.80%		94.13%		93.27%	
	(W/L)	4.34E+04		3.60E+04		3.40E+04	
Accuracy	Ripple	100%		100%		100%	
	Transient	100%		100%		100%	
		MM	MM-HV	MM	MM-HV	MM	
Price (H)	Die	$33,500	-	$8,500	$9,000	$2,000	
	Package	$2,600	-	$2,600	$2,600	$2,600	
	Total	$36,100	-	$11,100	$11,600	$4,600	

Assumptions:

(A) The battery voltage (V_{IN}) is assumed to be 4.2V in every case even though additional circuits are needed to protect transistors in the some technologies. R_{DSON} is calculated using realistic gate-drive (e.g. 1.8V for TSMC 0.18µm).

(B) Losses and resistance estimates are normalized to the values for 0.6µm.

(C) Includes 100mΩ for metal in addition to the resistance of the silicon.

(D) Given for the value of I_{OUT} where efficiency is maximum. (Not the same for every technology.)

(E) Switching frequency is 10MHz and converter always in continous-conduction mode.

(F) P_D (Driver Power) is sum of P_{GC} (Gate Charge) and P_{ST} (Shoot Through).

(G) No metal resistance is added to drivers, so P_{ST} scales slightly faster than R_{SW}.

(H) Based on $4mm^2$, except: TSMC 0.35µm HV minimum is $5mm^2$, and TSMC 0.18µm minimum is $25mm^2$.

References:

[1] TSMC 0.18µm (MOSIS: T92Y MM NON EPI THK-MTL)
[2] TSMC 0.35µm (MOSIS: V01C MM NON EPI)
[3] AMI 0.6µm (MOSIS: VO1W)