

Designing and Planning a Printed-Circuit Board (PCB) Prototype

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Evaluation Printed-circuit board (PCB) prototype design is a key step in evaluating, testing, and proving novel circuit concepts [1-2], especially when considering integrated circuit (IC) implementations are costly, time-consuming, and difficult to debug, which is why PCBs precede ICs in the experimental and developmental process, whenever possible. The popularity of PCB prototype design has therefore spread from industry to academia. However, evaluation time, measurements, and results, without a robust test plan, can be adversely affected, ultimately delaying the schedule and sacrificing reliability. Careful planning will avoid most of these drawbacks by addressing them early in the PCB design phase, by, for example, choosing the most appropriate equipment and test probes for the kinds of signals to be tested, by carefully placing additional test points, connectors, and circuits, and by other similar techniques, as shown in this document.

From a testing perspective, a robust test plan adds redundancy to the PCB prototype and thus enables signal extraction with minimal interference and maximum fidelity; in other words, the test plan ensures the signal measured is a true representation of its source signal and the extraction method is benign to the system. Moreover, a robust test plan is practical, simple, convenient, and cost-effective. Recognizing that various test signals and specifications require specific equipment, test probes, connectors, and circuits is important because they determine the validity of the experiments and respective results.

Equipment: Based on the type of signals to be tested (e.g., analog or digital, voltage or current, dc or ac, high or low frequency, large or small signal) and the specifications (e.g., unity-gain frequency, common-mode range, power supply rejection ratio, etc.), suitable equipment must be identified to reveal and measure these signals accurately and effectively. Power supplies, for example, provide dc and bias currents, and their accuracy will vary with vendor. Function and signal generators produce various types of waveforms and signals, but their output power is limited (i.e., driving current). Multi-meters measure dc and ac voltages, currents, and resistances, and like power supplies, their accuracy will vary with vendor. Oscilloscopes capture transient responses and ac signals, but they have finite input resistance and parasitic input capacitance, which will affect the signal measured and its degree of change will depend on the circuit being tested. Spectrum analyzers capture the frequency composition of a given signal, including distortion, system noise, and environmental noise, which is why low noise experiments may be warranted. Network/impedance analyzers extract S-parameters in amplitude and phase, which are useful for examining impedance-matching and loop-stability performance. Semiconductor parameter analyzers are versatile and programmable and capable of characterizing discrete

semiconductor devices and integrated circuits (ICs). Probe stations are very useful for debugging ICs, for accessing signals embedded in the die and exposing and severing metallic signal paths with a laser beam. The electrical characteristics of the probes used are critical, given that they have limited bandwidth, resistance, and physical resolution. As seen, the electrical characteristics of the equipment alter the signals being measured and it is up to the designer to appropriately choose the equipment so as to minimize these effects to acceptable and possibly negligible levels. More detailed equipment information about equipment can be found in [3-4].

Test Probes: Most equipment includes its own set of test probes, for a basic configuration, but their electrical characteristics, unfortunately, are not universally benign to a measurement, to the signal being tapped, especially for advanced measurements in electrically harsh environments. Common test probes include passive and active voltage, current, 50/75-Ohm coaxial, and differential probes [5], as shown in Figure 1. Passive voltage probes are inexpensive but usually have relatively high input capacitance, making them suitable only for low cost DC and low frequency measurements. Active voltage probes incorporate active components, like field-effect transistors (FETs), in addition to the passives to yield low input capacitance, high input resistance, and wide dynamic range characteristics. They are therefore suitable for a wide range of ac voltage measurements, including low and high frequency components, which could viably include undesired noise signals. Current probes can be the traditional ac-only or “hall wall” effect type. The former offers an accurate and low-cost measurement and the latter introduces lower loading effects, consequently making them more appropriate for high current measurements. 50/75-Ohm Coaxial probes have the lowest input capacitance and are therefore suited for RF and microwave frequency signals. Unfortunately, they are relative expensive and bulky. Differential probes are good for rejecting common-mode noise signals (i.e., high common-mode rejection ratio – CMRR) and suitable for floating measurements, like input offset voltages in differential operational amplifier applications. As noted, selecting the proper test probe for a given experiment is critical because its loading resistance and capacitance, bandwidth, and frequency response alter the fidelity of the signal and measurement.



Figure 1. Various test probes for a variety of applications.

Connectors and Sockets: The physical constraints of on-board connectors and chip sockets are many times important considerations in designing a PCB and testing a batch of silicon dies for convenience and, like test probes, their electrical characteristics also affect signal fidelity. Test-point connectors, like banana jacks, through-hole test points, surface mount technology (SMT) test-points, SMT ball and socket connectors, switches and jumpers, and so on (Figure 2), are selected to match the test probes and signal requirements of the experiment. Banana jacks, for instance, are bulky and typically used for high power supply paths. Through-hole test-points are for PCBs with through-hole chips, like single- and/or dual-in line packages (SIP and/or DIP). Multi-layer PCBs with SMT chips, like small-outline integrated circuit package (SOIC), exploit the benefits of SMT compatible test-points – SMT ball and socket connectors are good for high-speed digital signals because of their ease and bus-connecting capabilities. Switches and jumpers are convenient means of enabling and disabling parts of a system, which is especially useful in the debugging phase of a PCB design [6-7]. On the other hand, sockets as the ones shown in Figure 3 for chip-packaged prototypes (e.g., plastic leadless chip carrier (PLCC), quad flat no-lead (QFN), SOIC, small outline transistor (SOT), small shrink outline package (SSOP), thin small outline package (TSOP), and so on), are useful for easily testing several similar prototypes without having to solder or de-solder components on the board, which would otherwise damage the PCB. The incidental parasitic devices introduced by the socket affect signal fidelity, but the convenience of testing a batch of silicon on one PCB may sometimes merit its use, especially if the parasitic effects are negligible. In all, connectors and sockets not only extend but also define the physical constraints of a given test probe link and silicon chip prototype.

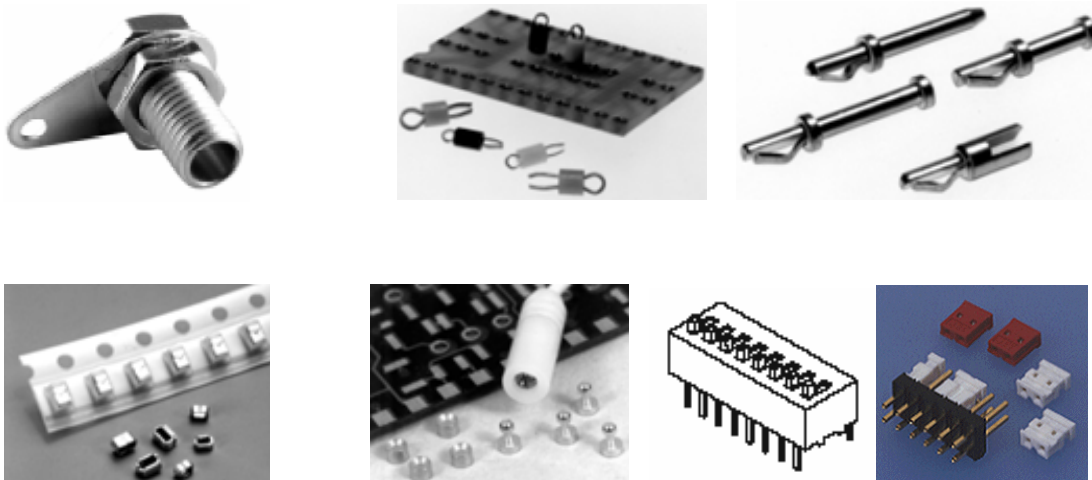


Figure 2. Test-point connectors.

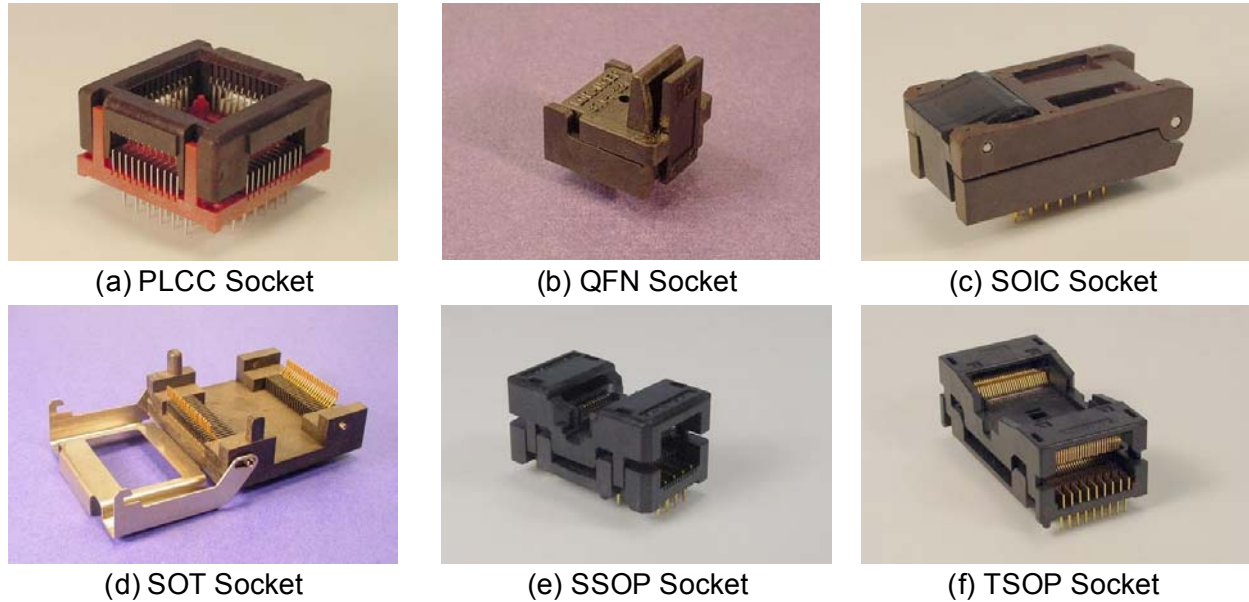


Figure 3. Chip Sockets.

Occasionally, for low cost, simplicity, and minimum real estate, two-dimensional test-points, like copper and metal test pads and vias (Figure 4), are fabricated directly on the PCB board, unlike connectors, which are appended to it. These pads and vias, as well as connector footprints, must be placed close to the signal being tested to reduce the parasitic resistance and capacitance associated with the connection and therefore minimize interference and maximize fidelity. The shape and design of these pads and vias can be customized to almost any application.

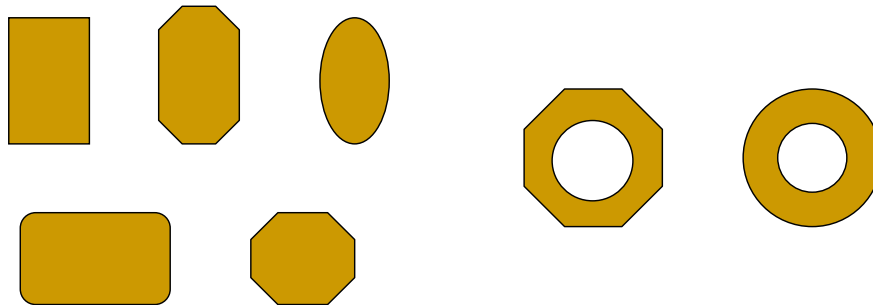


Figure 4. Two-dimensional test-points.

Circuits: Unfortunately, testing and measuring low power, low energy signals is difficult because any parasitic in the equipment, test probe, connector, and PCB will unavoidably affect it. Application-specific circuits like low noise and low input-offset amplifiers, drivers, and buffers can sometimes be used to isolate and contain these signals before exposing them to the parasitic elements just mentioned. Simply said, they sample and amplify signals with minimal distortion before making the first measurement but, like with anything else, tradeoffs like switching noise, cost, real-estate, etc. exist and must be comprehended into the design. Sometimes the sensitivity and vulnerability of a signal is too great for a circuit to sample without adversely affecting it,

which is why the designer/experimentalist must scrutinize the results, evaluate and re-evaluate assumptions, and carefully extrapolate conclusions.

Test Plan: Given the complexity and extensive set of considerations of designing a PCB (i.e., equipment, test probes, connectors, circuits, and measurement issues), the designer must carefully devise a test plan. The plan must therefore start with the circuit to be tested. One must ascertain the parameters and specifications first, followed by the electrical sensitivity of each signal to parasitic resistance, capacitance, and inductance. The signal’s accessibility must be defined and comprehended into the PCB. Once these constraints are defined and redundancy explored, equipment, test probes, connectors, and circuits for each signal can be identified, at which point the simulation process of the PCB schematic can commence.

PCB simulation must emulate and evaluate all the experimental procedure to be performed on the circuit. Only after carefully and fully simulating the projected PCB design and test plan can the layout process begin. Simulating the test procedure ensures that the proper nodes to be accessed are defined. Predicting problems before the layout process is important because redundancy and access to miscellaneous nodes in the system can potentially ease the debugging effort.

Finally, when testing a PCB, the procedure must start by testing the connectivity of the PCB, without the device under test (DUT), to ensure the PCB is operational. This should be followed by adding the DUT and testing only DC measurements to verify the device is properly biased. If problems exist, the debugging phase should start, before making any other measurements. If the system is properly biased, functional measurements should be performed to test the operational status of the various system blocks, possibly identifying problem areas. Once functionality is verified, specific ac and transient measurements can be performed, which would ultimately be followed by a full statistical evaluation, where several DUTs are tested and their statistical sigma performance is ascertained. Figure 5 illustrates a sample schedule, highlighting the major test plan issues discussed in this section.

ID	Task Name	Eight Weeks							
		W1	W2	W3	W4	W5	W6	W7	W8
1	Spec. and System Design	■							
2	Circuit Design & Simulation		■						
3	Equipment, Probes, Connectors, and Circuits Identification			■					
4	Test Plan				■				
5	PCB Design & Layout				■				
6	Experimental Evaluation (DC, functional, and statistical measurements)						■	■	■

Figure. 5. A sample schedule.

The goal of the entire research and development (R & D) cycle is to build a working prototype and every design activity, including circuit design and simulation, test plan, PCB design and layout, and experimental evaluation, must therefore be synchronized in harmony,

appropriately assigning tasks at suitable times in the schedule and interweaving them with synergy. The test plan, which is many times overlooked or undervalued, is a pivotal part of the project, especially when managing design risk and test time. With a robust test plan, evaluation time can be decreased, complex measurements eased, and accurate results verified, thereby increasing the chances of meeting project deadlines and shortening time-to-market cycles.

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