# Using a Circuit-Driven Approach to Teach Printed-Circuit Board (PCB) Layout Techniques for Switching Power Supply Circuits

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## Abstract

*Power supply circuits are critical components in all electrical systems. They not only supply power but must also do so without degrading system performance with noise and/or sagging supply voltages, which is why the layout of the printed-circuit board (PCB) is extremely important. Key power supply specifications like output voltage accuracy and power efficiency worsen when the layout of the PCB is less than optimal, since the effects of parasitic PCB resistances and inductances are considerably high for high-current, fast-switching traces. Most college-level power and analog courses, textbooks, and papers discuss the circuit design aspects of switching power supply systems but largely ignore the details of PCB layout design. This paper addresses this gap by exploring, explaining, and outlining how PCB layout can affect the power supply system, and devising a set of design guidelines and instructional material based on the circuit. This circuit-driven approach to PCB layout trains students, technicians, and young engineers in PCB layout for high performance circuit topologies by first focusing on the effects of layout-induced parasitic impedances on key circuit specifications, then addressing them with proper layout guidelines.*

**Keywords:** Switching Regulators, DC-DC converters, Power supply circuits, PCB layout, high-current nodes, fast-switching signals, EMI, ground loop, and PCB model.

## 1. Introduction

The demand for higher-performance switching regulators is relentless, requiring high power efficiency and accuracy, especially in battery-operated applications, such as laptops, cell phones, and personal digital assistants (PDAs). Efficiencies of more than 90% are required at both high and low loading conditions. Moreover, the output voltage ripple must be kept below tens of millivolts during all possible load transients. Significant effort has therefore been dedicated to devise techniques that improve power efficiency and accuracy of switching supply circuits [1-2], and the incremental power efficiency improvement of any one of these techniques is normally

less than 5%. However, these seemingly insignificant improvements are intrinsic and necessary to meet the stringent efficiency specifications of today's state-of-the-art applications.

The design of printed-circuit boards (PCBs) for high-current, fast-switching power converters requires more caution than ordinary PCBs, since the voltage drops caused by the parasitic impedances become significant in high current and fast-switching conditions. A PCB that is not well designed can degrade the power efficiency by up to 10% and increase the output ripple by tens of millivolts, thereby reducing accuracy performance. To compensate for a poorly designed PCB, design and application engineers must develop additional circuitry and/or upgrade their external components (e.g., low-resistance power switches, low ESR inductors, low ESR ceramic capacitors, etc.), which not only increases design time but also overall system cost.

There are many well-known references on the design and analysis of switching power supplies, but little [6-8] to no discussion [3-5] is offered on the design aspects of the printed-circuit boards (PCBs). Most of the literature on the design of PCBs for switching supplies is found in a few obscure application notes [9-16], and most of the guidelines are oriented specifically to a commercial product, outlining an application-specific layout plan, not general design guidelines.

The objective of this paper is to provide a tutorial and instructional material on PCB design of fast-switching, high-current power supplies for students, technicians, researchers, and engineers who are not experts in the field of power supplies. A sample switching power supply circuit is used to highlight and extrapolate the various design considerations of PCBs for high power circuits. The guidelines are derived from the circuit directly such that the techniques used to address them can be extended to other circuits under similar design constraints, in other words, high power circuits.

## 2. Modeling Connections

In practice, electrical nodes are not dimensionless, zero-impedance junctions. They are metal links with resistive, inductive, and capacitive properties that vary significantly with PCB layout. An area of metal used to connect two electrical points can be modeled with a simple impedance network consisting of a resitor, inductor, and capacitor combination, as shown in Figure 1. The parasitic capacitance to ground is normally negligable, when compared to the capacitors typically used in power supply circuits (e.g., 1 nF to 100 μF). An area of metal used to link three ports is similarly modeled with the triangular impedance network shown in Figure 2(a), where each impedance consists of a parasitic inductor in series with a parasitic resistor, neglecting the parasitic capacitors because of the aforementioned reason. Increasing the width of the links, as done in Figure 2(b), do not alter the circuit model, even when the width is large enough to eliminate the separation between the links (Figure 2(c)). The corresponding impedance values are the only ones that change. Generally, the connection can have any arbitrary shape, including an irregular chunk of solder, as illustrated in Figure 2(d).

The triangular model can always be mapped into an equivalent star network, and vice versa (Figure 3). The dimensionless, zero-impedance node in the middle of the star network is only conceptual and is not literally accessible on the PCB. An "n" port connection can be decomposed into two- and three-port sections, and a star model can be used for each of these segments, as shown in Figure 4.

To extract the pertinent star model parameters, the impedance between any two points is measured, while leaving the remaining terminals disconnected. Through inspection, the measured impedance between any two points in the triangular model (e.g., $Z_{12}$) is the parallel combination of the direct impedance between the two points (e.g., $Z_a$) and the series impedance

combination going through the third point in the triangle (e.g., $Z_b + Z_c$), which is how the triangle model maps into a star network:

$$Z_{12} = Z_a \,||\, (Z_b + Z_c) = \frac{Z_a Z_b + Z_a Z_b}{Z_a + Z_b + Z_c} = Z_1 + Z_2 \,. \tag{1}$$

Measuring the impedance between terminals one and two, two and three, and one and three yield $Z_1 + Z_2$, $Z_2 + Z_3$, and $Z_1 + Z_3$, respectively, which are readily solved (three equations and three unknowns).

The actual resistance and inductance of a PCB metal trace with length l, width w, and height h in meters are

$$R = \rho\left(\frac{l}{wh}\right) \tag{2}$$

and

$$L = 2l\left[\ln\left(\frac{2l}{w+h}\right) + 0.5\right]10^{-7}\,H\,, \tag{3}$$

where ρ is the metal line resistivity (1.724e-8Ω·m for copper) [17]. The inductance is an approximation because components in its proximity will also affect its value. As a rule of thumb, every 2.5cm (one inch) of 0.25mm (10mil) wide and 0.035mm (1.4mil) thick copper trace has 20mΩ of resistance and about 20nH of inductance [9]. Consequently, both a 1A per 1μs change in current and a 1A DC will independently cause a 20mV drop across the aforementioned trace ($V = Ldi/dt + I_{DC}R$). High current, fast-switching signals are therefore critical, not only do they incur the resistive but also the transient inductive voltage drop, which could be worse (e.g., 1A/10ns through a 20nH inductor incurs a 2V drop). The inductive voltage drop fades away after the transition is over, but its mere occurrence can still disturb the functionality of the system and damage various parts of the power supply, especially the sensitive ICs because of various failure mechanisms, such as minority carrier injection or latch up [18]. To reduce these ill-fated effects,

in other words, decrease the parasitic resistance and inductance of the trace, the trace should be short and wide (Equations 2 and 3). However, an increase in width is not as effective as a decrease in length because of the logarithmic term.

As an example, to illustrate how to model and ascertain the parasitic effects of any given connection on a PCB, the ideal buck-switching regulator illustrated in Figure 5(a) is used, but the process and procedure used here is naturally extended to any high power PCB application. The circuit consists of various power and control components, consisting of power MOSFET $M_p$, power diode $D_p$, output capacitor C, power inductor L, input capacitor $C_{in}$, and a controller IC. The battery and loading application are connected to the input and output of the regulator, respectively. Figure 5(b) illustrates how every connection in the converter shown in Figure 5(a) is modeled with a star network, where each impedance is a parasitic resistor-inductor combination. The electrical components of the circuit also have parasitic effects, most important of which are normally their equivalent series resistors (ESRs) (e.g., inductor and capacitor ESR).

Figure 5(a) also illustrates the high-current and fast-switching paths, which are of particular interest, given their significant parasitic effects. The MOSFET and diode currents, for instance, are pulsating in nature, as also shown in the figure, switching from zero to the inductor current level in a few nanoseconds. These currents are therefore both high current and fast switching, which is why reducing their pertinent parasitic resistance and inductance values is extremely important. The output capacitor, on the other hand, only carries the inductor current ripple, which is neither relatively high in value nor fast, and higher parasitic inductance is therefore tolerated in the metal link between the inductor and the output capacitor.

These parasitic impedances can severely affect the performance of a system, from a malfunction to degraded power efficiency and reduced accuracy. The large voltage spikes across

the parasitic inductors can potentially reverse-bias and damage internal silicon p-n junctions present in the control circuitry. What is more, the power losses associated with the parasitic resistors has a direct bearing in overall power efficiency, which is especially critical in portable electronics for extended battery life. The parasitic PCB resistance series with the output capacitor's ESR not only has this effect but also degraded accuracy and altered filtering characteristics, which of course affects feedback stability.

# 3. PCB Layout Guidelines

Layout techniques for switching power supplies are divided in two general categories: those that affect circuit performance and those related to electro-magnetic compliance (EMC). The former addresses the functionality, accuracy, and efficiency of the circuit and the latter is mostly targeted to ensure the circuit passes EMC tests. While the guidelines assume the power switches and diode are off-chip, the same rules apply to controller ICs with on-chip power components. What is more, these guidelines, at a smaller scale, also apply to the IC itself, to the "PCB" within the chip.

## A. Functionality

Parasitic resistors in high-current paths and parasitic inductances in fast switching signal traces can potentially upset the circuit operation of the system. Consequently, for the sample buck-supply circuit shown in Figure 5, the most important connection is the phase junction that connects the power inductor to the switches ($V_{phase}$), since it carries fast-switching currents in the order of amperes. The trace connecting the input capacitor, the input supply's positive terminal, and the power MOSFET's source as well as the connections from the diode to power ground carry high current and fast switching signals (Figure 5). As explained in Section 2, short and wide routing traces have lower parasitic resistances and inductances and therefore superimpose

less ill-fated effects to the system. As a result, to reduce parasitic resistance and inductance, the first rule in PCB layout is to place connected power components (i.e., $C_{in}$, $M_p$, $D_p$, L, and $C_{out}$) as close as possible, and in a way that their interconnection lengths are minimal [8]. The width of all high-current paths should be sufficiently wide to exhibit low resistive values, when compared to the power components. For example, if the power switch's resistance is 70mΩ, the PCB's trace resistance should be less than 10 mΩ so as not to incur significant additional power losses. Moderate current-carrying paths, like the path from the MOSFET's gate driver to the MOSFET's gate, also warrant some attention because of their peak switching current characteristics. The issues that apply to high current, fast-switching paths also apply to moderate current-carrying paths, but in a less critical fashion; in other words, they have lower priority. The width of PCB lines can therefore be somewhat smaller and their length longer, implying slightly higher resistance and inductance values and therefore giving the designer more flexibility to address fast-switching, high-current paths first.

Additional precautions should be employed in the design of evaluation boards (e.g., EVM). In these boards, which are many times used to test and gauge switching supply circuits, the power supply and the system load are not on the PCB. They are connected to the board via lead wires and connectors, which introduce series resistors and inductors. In a portable application, the power supply (e.g., battery) and the load may be on the same PCB, and no additional lead wires may be needed. In such cases, the parasitic components of the leads are not present.

Another important issue is to use separate, parallel connections for the supply ground, load ground, and measurement instrument's ground, instead of series connections. Series connections are unreliable and lossy, and they introduce additional undesired impedance between critical

nodes. Undesired noise and high temperature gradients across the PCB usually result when problems with supply ground connections exist.

**B. Accuracy**

Power supply circuits regulate the supply voltages of loading applications against variable input supply variations and across operating conditions, making accuracy a key performance parameter. For maximum accuracy, the feedback sense terminal should be connected as close to the load as possible, since the voltage across the load is the one requiring regulation (Figure 5). Although this connection of the feedback network ensures output dc accuracy, the output ripple during steady-state conditions and load transient events are functions of PCB parasitic impedances, as will be shown. During normal operation, the inductor current is the summation of load current $I_{DC1}$ and capacitor ripple current $I_c$ (Figure 6(a)). Since the rate of current change in steady state is relatively small (e.g., in the order of 1A per μsec), the voltage drops across the parasitic inductors are negligible. Moreover, the voltage drops across load connections ($R_{PCB\text{-}ld+}$ and $R_{PCB\text{-}ld-}$) are constant since the load current is constant in steady-state. Consequently, the voltage ripple across the load is

$$V_{out\text{-}AC}(t) = I_c(t)(R_{PCB\_C+} + R_{PCB\_C-} + R_{ESR\_C}) + \frac{1}{C_{out}}\int I_c(t)dt\,, \qquad (4)$$

where $R_{ESR\_C}$ is the output capacitor's ESR and $R_{PCB\_C+}$ and $R_{PCB\_C-}$ are the PCB parasitic resistors used to connect the capacitor to the circuit. Ripple current $I_c(t)$ is a function of input voltage $V_{in}$, output voltage $V_o$, inductor L, and the switching frequency of the supply circuit, and is independent of the output capacitor and load, since the output voltage is for all practical purposes constant in steady state. The ripple voltage across the output capacitor is usually small because of its high capacitance. The output voltage ripple is therefore mostly composed of the capacitor's ESR and the parasitic PCB resistances.

In constant frequency controllers such as pulse-width modulated (PWM) controllers [2-5], the inductor ripple current is fixed because the switching frequency is constant. As a result, inductor ripple current ($I_c$) is constant and the steady state output ripple voltage is increased if parasitic resistors are increased (Eq. (4)). However, in constant ripple voltage controllers like hysteretic converters [2], the change in parasitic resistances manifests itself in a variation of switching frequency, which results in lower overall efficiency (e.g., an increase in equivalent capacitor ESR from 10mΩ to 20mΩ doubles the swicthing frequency and switching losses). Hence, to increase both ac accuracy and power efficiency, both in the case of PWM and hysteretic power supply circuits, the PCB should be designed such that $R_{PCB\_C-}$ and $R_{PCB\_C+}$ are minimal.

The effect of PCB parasitic impedances becomes even more important during load transients. If the load current changes abruptly, from $I_{DC1}$ to $I_{DC2}$ in nano seconds, the inductor current and supply circuit cannot respond fast enough to fully comprehend the change. Thus, the output capacitor ($C_{out}$) supplies all the transient current, simplifying the output stage to just a passive LCR filter (Figure 4.b). The maximum instantaneous output voltage ripple happens at the end of a load-current change, when load current has just reached $I_{DC2}$. Since the output capacitor is large, its output voltage does not change significantly, and hence the transient ripple voltage mostly consists of the resistive voltage drops across the parasitic resistors ($V_{INST-R}$) and the inductive voltage spikes across the parasitic inductors ($V_{INST-L}$), which results in

$$V_{INST} = V_{INST\_L} + V_{INST\_R} = (L_{PCB\_C+} + L_{PCB\_C-} + L_{PCB\_ld+} + L_{PCB\_ld-})\frac{I_{DC2} - I_{DC1}}{t_r} + (R_{PCB\_C+} + R_{PCB\_C-} + R_{PCB\_ld+} + R_{PCB\_ld-})(I_{DC2} - I_{DC1}). \quad (5)$$

After the transient condition, the inductive drop is shunted by an LCR tank (i.e., parasitic L, parasitic R, and $C_{out}$), and the output voltage drop retains its $V_{INST-R}$ value (Figure 6(b)). After

the initial drop sequence, the output voltage continues to drop slowly because the output capacitor slews (i.e., discharges). After a delay time proportional to the inverse of controller bandwidth, the controller kicks in and starts to recharge the capacitor to reach the desired steady state operation. Although the drop due to the capacitor discharge can be limited by designing output capacitor value and the controller loop bandwidth, the instantaneous voltage drop ($V_{INST}$) is independent of DC-DC converter control circuitry and is strongly PCB design dependent. From Equation 4, the worst-case instantaneous ripple occurs when the output current changes abruptly from zero to full load or vice versa. To minimize the instantaneous drop, the output capacitor should be placed as close as possible to the load, and therefore for a specified transient accuracy, the designer should pay special attention in routing the trace that connects load to output capacitor.

### C. Noise

Switching nodes and traces of a DC-DC converter can inject noise to the analog and sensitive traces through capacitive coupling. The traces that are connected to high-impedance nodes are more sensitive to pickup environmental noise. To increase noise immunity, the traces connected to high impedance nodes should be routed as short as possible and placed as far as possible from noisy traces. For example in Figure 5(b), $V_{sense}$ voltage at the resistor dividers is connected to the high impedance input of error amplifier in the controller. Therefore, resistors $R_{f1}$ and $R_{f2}$ should be placed close to the chip and far from noisy phase node ($V_{phase}$) to increase noise immunity of sense voltage.

### D. Radiated Electro-Magnetic Interference (EMI)

Radiated electro-magnetic interference (EMI) is another important issue to consider in the layout design of power circuits. Due to industry standards, the amount of electro-magnetic power

propagated from a commercial circuit through radiation should be limited. This limitation minimizes the interference among electric systems when they are working in close proximity [19-20]. Nodes with fast switching voltages and/or currents generate radio-frequency (RF) noise (e.g., the $V_{phase}$ node in a buck converter has nano-second rise and fall times). In general, any trace containing an ac current generates time-varying magnetic fields around it, producing time-varying electric fields and consequently radiating EMI.

To limit the electro-magnetic radiation from the PCB, two important guidelines should be considered. First, high frequency switching nodes should be as short as possible. The metal paths act as antennas and their frequency range is directly proportional to their length (i.e., shorter paths cover lower frequency ranges). Second, high frequency signal-return paths should be as close as possible to their respective forward paths. The two traces will therefore generate equal but opposite magnetic fields, canceling each other and hence reducing radiated EMI.

Although a strong recommendation for using ground planes exists (i.e., filling every available space on the PCB with copper and connecting to ground), the use of a ground plane may not be effective in all instances [9]. Ground planes are effectively close high-speed return paths for average forward signal paths, but arbitrarily increasing the ground plane may not necessarily reach critical nodes. In PCB technologies with more than two layers, middle layers are normally dedicated to ground planes, thereby decreasing their distance to high-current forward switching paths. Large metal areas connected to the controller pins also help conduct thermal energy from the chip to the surrounding air, resulting in lower junction-to-ambient thermal impedance and consequently reducing power losses, decreasing operating temperatures, and increasing reliability. This is especially important with controller chips that use on-chip power switches [13-14]. In a buck converter, for instance, careful attention should be paid to the switching phase

node and other fast-switching traces carrying high MOSFET and diode currents to minimize EMI propagation.

The trace connecting a driver circuit to the gate of a power MOSFET switch also requires scrutiny [6, 19]. During the power MOSFET's off to on transition, the driver circuitry charges the gate of power MOSFET with more current than is usually necessary, which results in damped oscillations in the presence of a parasitic inductance in the gate trace. The damping frequency is usually an order of magnitude higher than the on/off transitional frequency ($1/t_{rise}$ and $1/t_{fall}$ where $t_{rise}$ and $t_{fall}$ are rise and fall times of the switch's controlling node, the gate in the case of MOSFETs). Since the power MOSFET is a large device, relatively high energy is involved in the on/off events, radiating EMI and possibly causing the power supply to fail EMC tests at high frequencies. To eliminate this effect, a series resistor can be placed in series with the power MOSFET's gate to limit the current during the on/off transitions.

# 4. Measurements

### A. Test Points

Caution must be exercised when connecting measurement instruments' leads to the PCB. In Figure 5(b), the proper measurement points to test a DC-DC converter circuit, not to a PCB, are labeled as $V_{in1}$, $V_{out1}$, and $V_{GND1}$. To measure the output voltage, the oscilloscope ground should be connected to the ground plane, as close as possible to the capacitor, feedback, and load ground. Similarly, the oscilloscope probe should be connected to the output node as close as possible to the filter capacitor, feedback resistor, and load nodes. To measure the input voltage level, the input node voltage in the PCB closest to the MOSFET source is preferred. The aforementioned technique eliminates the effect of lead parasitic resistances in computing the

efficiency. If the PCB is included in the test, the oscilloscope lead should be connected to the supply, ground, and output planes, which are illustrated by $V_{in2}$, $V_{out2}$, and $V_{GND2}$ in Figure 5(b).

**B. Ground Loops**

A potential measurement problem in the process of power supply measurements is the ground loop situation [8]. A ground loop occurs when there is more than one ground path from the supply ground to the load ground. Test and measurement equipments have a safety connection to "earth" ground by the bench, which may cause undesirable connections between various ground points in the circuit. The oscilloscope ground is usually connected to the workbench earth. The supply voltage ground and the load ground may or may not be connected to the earth ground. The effect of a ground loop in the behavior of the system is graphically illustrated in Figure 7. The oscilloscope and power supply are not isolated from the workbench "earth" in this scheme. The oscilloscope measures the voltage difference at its inputs ($V_{ch1}$ and $V_{GND}$), but the oscilloscope probe is connected to $V_{LGND}$ and $V_o$ at converter. Because of probe high impedance at $V_{ch1}$, there is no significant voltage drop between $V_{ch1}$ and $V_o$. Nevertheless, the load current ($I_{Load}$) can return to the battery negative terminal through both the designed ground plane or from the workbench earth through probe ground wire. As a result, current flowing through probe parasitic resistance and inductance ($R_{probe}$ and $L_{probe}$) generates a voltage drop between $V_{GND}$ and $V_{LGND}$, which distorts the measured waveform. Therefore, circuit performance is underrated.

There is a simple way to test if a ground loop problem exists in the measurement system. While the DC-DC converter is operational, if the oscilloscope probe lead and its ground are connected to the ground plane and the noisy spikes at the switching frequency of the converter are seen on the oscilloscope display, the ground connection is not good, and a ground loop problem exists. To prevent this ground loop problem, the oscilloscope should be isolated from

the bench. Either an isolation transformer can be applied to supply the oscilloscope or a differential probe can be used to isolate the probe ground from "earth." Another approach is to use floating supplies and loads.

## 5. Feedback from Students

This instructional material was first prepared as a tutorial for the graduate students in the Georgia Tech Analog and Power IC Laboratory, in the School of Electrical and Computer Engineering at Georgia Institute of Technology. These students' research is in integrated and discrete power supply circuits, from switching buck, boost, and buck-boost DC-DC converters to chargers and linear regulators. Since the projects are new designs for which there is no industry equivalent or corresponding layout guidelines, the instructional material was meant to apply to a wide range of circuits, thereby allowing the students to extrapolate and extend the general rules to their own designs. The feedback from these graduate students suggests that the instructional material not only guides the students through the design of PCB but it can also be applied to routing, floor planning, and package selection of power management integrated circuits.

Additionally, the instructional material was also presented to undergraduate students studying analog circuit design in the spring semester of 2005. The student evaluation forms (summarized in Table 1) indicate a mostly positive response. The majority of students felt the PCB design strategies taught enhanced their understanding of practical circuit design issues.

**Table 1. Student Evaluation Results.**

**(Key: A- Excellent, B- Very Good, C- Good, D- Poor, and F- Failure).**

| Questions * | A | B | C | D | F |
|---|---|---|---|---|---|
| How well this lecture introduced you to plan layout of PCBs? | 24% | 43% | 29% | 4% | 0% |
| How well did you understand the guidelines? | 24% | 48% | 19% | 9% | 0% |
| How well the guidelines are applicable to different circuit topologies? | 23% | 50% | 28% | 0% | 0% |
| How well theoretical backgrounds were provided to support the guidelines? | 10% | 48% | 38% | 4% | 0% |
| How is your overall rating of the lecture/instructional material? | 5% | 67% | 14% | 14% | 0% |

* 21 students participated in the survey.

# 6. Conclusions

This paper presented a new instructional material for PCB layout design of high-performance power supply circuits. Instead of describing a set of rules that are applicable only to a special circuit topology, the material provides general PCB layout design guidelines and how they address the various important performance parameters of high-current, fast-switching applications, using a switching power supply circuit as an example. The approach is to first model the parasitic trace impedance of connections and then study their effects on the functionality and key performance specifications, such as accuracy, efficiency, and electro magnetic compliance (EMC). After analyzing and prioritizing the various error sources, PCB layout guidelines for placing components and routing traces were derived, as summarized in Table 2.

The educational survey results from both graduate and undergraduate students were positive. The undergraduate students found it useful and enlightening, especially enhancing and applying the material from analog circuit design courses. Graduate students found the material useful for designing high performance power supply circuit PCBs. They also found the guidelines were compatible with the design of integrated circuits (IC), and more specifically in the floor-planning and layout phase of ICs, which refers to the "PCB within the chip."

**Table 2. Summary of circuit-driven PCB design approach.**

| | Culprit | Approach |
|---|---|---|
| Functionality | Parasitic L<br>Parasitic R | ▪ Reduce parasitic inductances in fast-switching current paths to suppress unwanted $L_{par}$di/dt voltage drops.<br>▪ Reduce parasitic resistances in high-current paths to eliminate unwanted $R_{par}$I voltage drops.<br>▪ Priority is with fast-switching connections since $L_{par}$di/dt dominates if switching frequency is high.<br>▪ Place power components as close as possible to each other.<br>▪ Reduce the parasitic inductances and resistances by routing them as short and wide as possible. |
| Efficiency | Parasitic R | ▪ Reduce parasitic resistances in high-current paths.<br>▪ Place power components as close as possible to each other to reduce the length of connections. Route their connections as wide as possible. |
| DC Accuracy | Parasitic R | ▪ Connect the Controller IC output voltage sense and analog ground pins as close as possible to the load.<br>▪ Place the output capacitor as close as possible to the load to suppress the parasitic resistances between load and output capacitor. As a result, the ac ripple is reduced. |
| Transient Accuracy | Parasitic R<br>Parasitic L | ▪ Reduce the parasitic resistance and inductance between output capacitor and the load to reduce voltage drops across parasitic inductors and resistors at load transients. |
| Switching Noise Injection | Parasitic C | ▪ Route sensitive connections connected to high impedance nodes as short as possible.<br>▪ Route them as far as possible from noisy signals to reduce capacitor coupling to noisy signals.<br>▪ The trace that connects the sensed output voltage from feedback resistors to the input of controller error amplifier is "the" sensitive connection in switching regulators. |
| EMI | | ▪ Route fast-switching connections as short as possible.<br>▪ Route return paths of fast switching connections close to their forward paths.<br>▪ Priority is with routing connections that their currents change suddenly (fast-switching currents).<br>▪ Fill empty spaces with ground plane. |
| Test & Measurement | | ▪ Beware of ground plane changes because of connecting test and measurement instruments to the converter circuitry. Avoid ground loops by:<br>- Floating supplies and loads<br>- An isolated oscilloscope |

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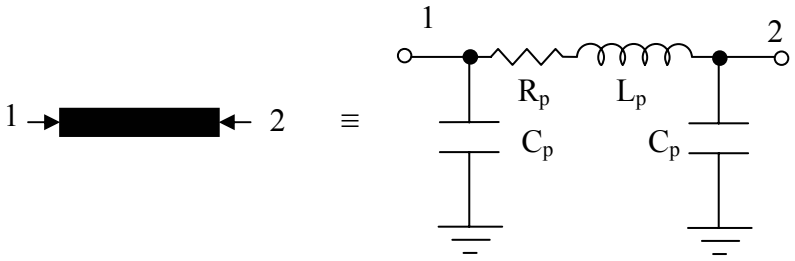



**Figure 1. Electrical modeling of a two-port connection.**

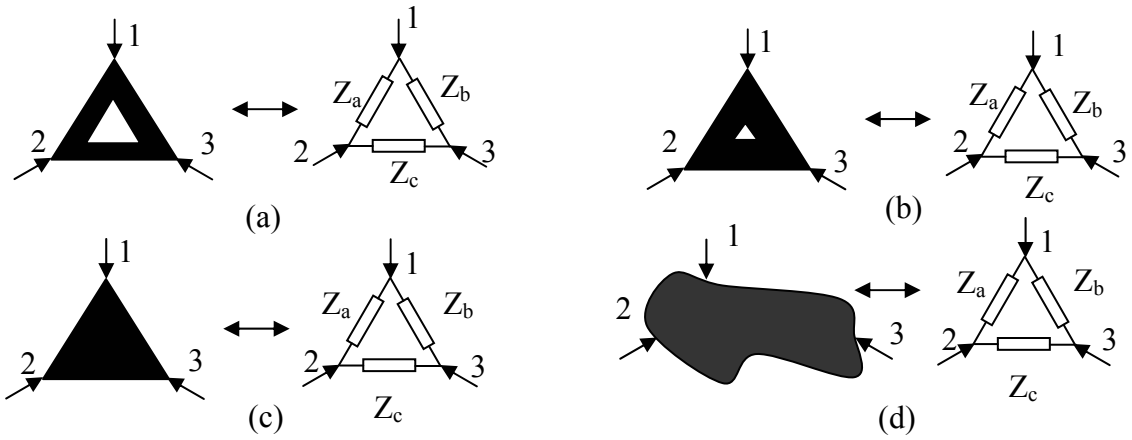
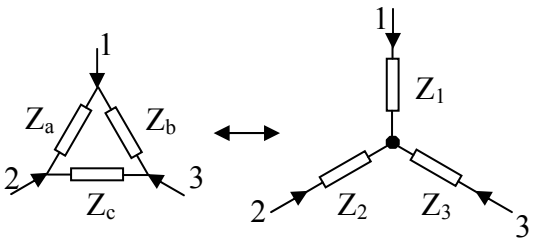



**Figure 2. Modeling high-current fast-switching connections: (a) model for a triangular three-port surface with a large opening in the middle, (b) model for a triangular three-port surface with a small opening, (c) model for a solid triangle, and (d) model for an arbitrary slab of solder.**

$$Z_{12} = Z_1 + Z_2$$
$$Z_{13} = Z_1 + Z_3$$
$$Z_{23} = Z_2 + Z_3$$




$$Z_1 = \frac{Z_a Z_b}{Z_a + Z_b + Z_c}$$
$$Z_2 = \frac{Z_a Z_c}{Z_a + Z_b + Z_c}$$
$$Z_3 = \frac{Z_b Z_c}{Z_a + Z_b + Z_c}$$

**Figure 3. Triangle-to-star impedance network conversion.**

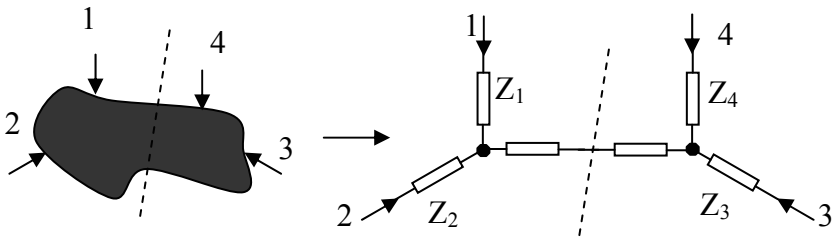



**Figure 4. An impedance model for a four-port connection.**

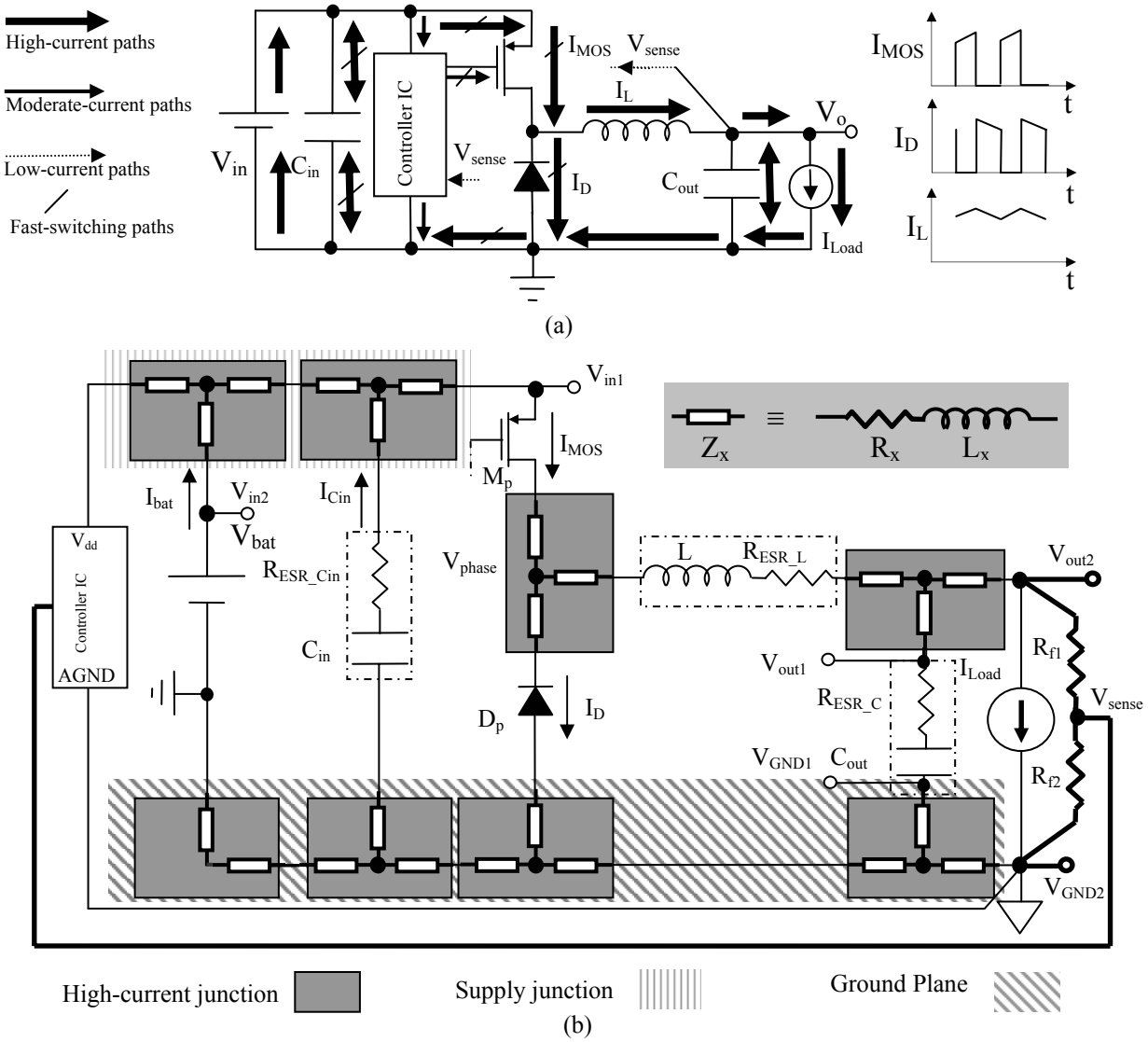



**Figure 5. (a) High-current and fast-switching paths and (b) parasitic resistors in a buck DC-DC converter circuit.**

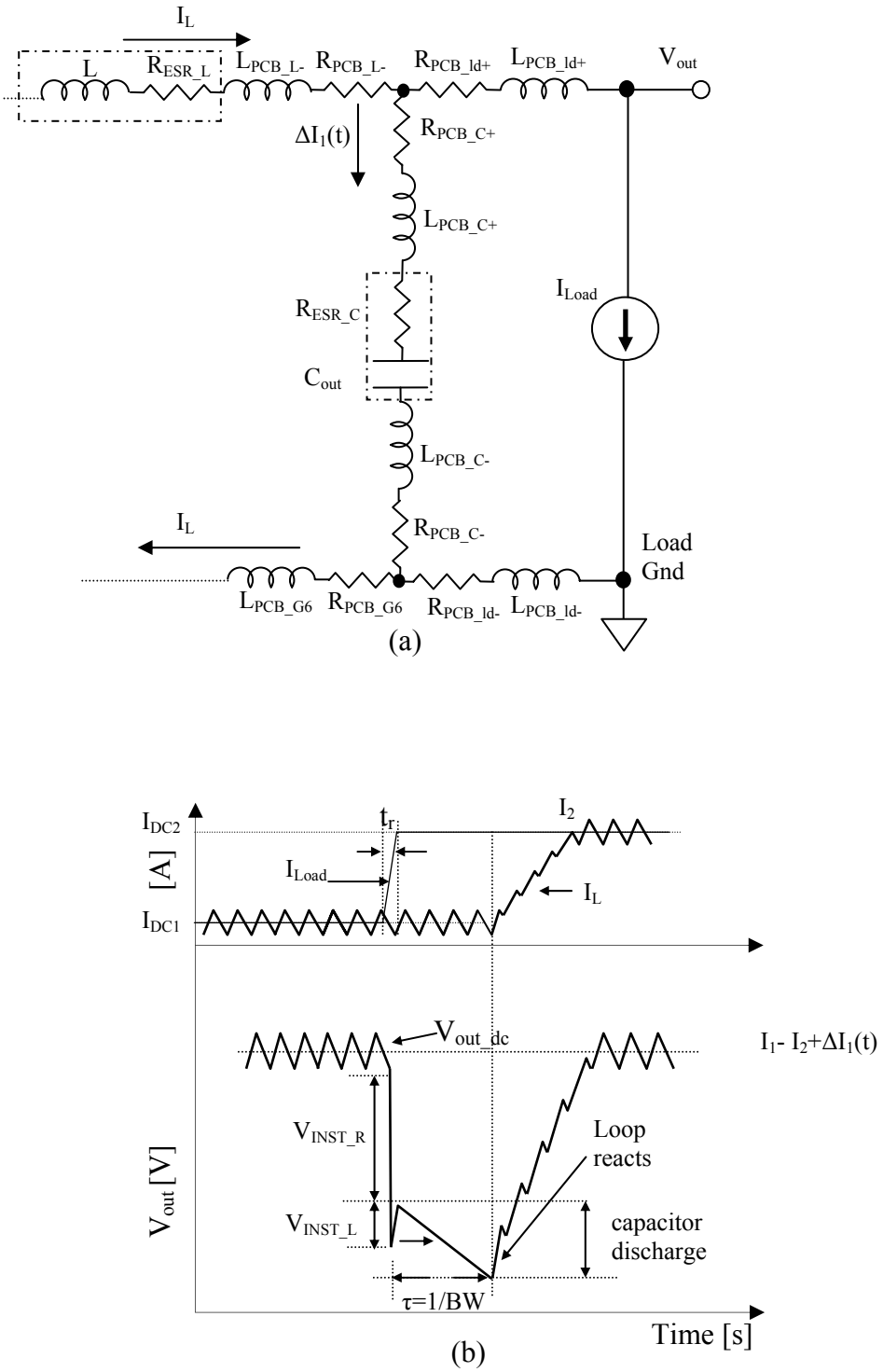



**Figure 6. (a) Equivalent circuit and (b) output voltage waveform during a current load transient for a buck converter.**

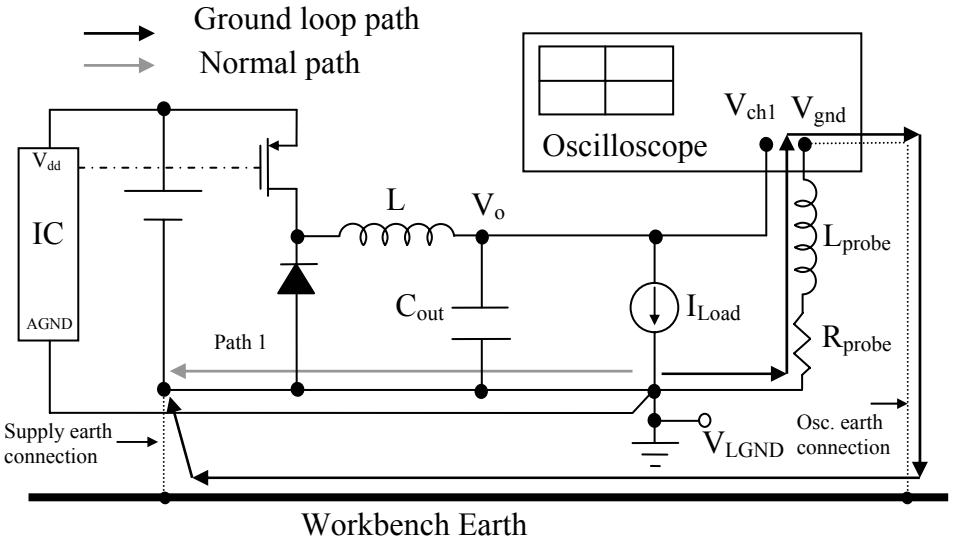



**Figure 7. Illustration of ground loop problem: if the oscilloscope and power supply are not isolated, the oscilloscope probe ground conducts high switching current and generates an unwanted voltage drop across the ground probe lead and the oscilloscope ground.**