Frequency Response of Hysteretic Comparators in Switching Converters

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Abstract

Hysteretic switching dc-dc converters are popular because they are (i) relatively simple (i.e., self-oscillating and self-compensating), (ii) fast (i.e., able to respond within one switching cycle: $f_{\text{0dB}} = f_{SW}$), and (iii) robust (i.e., reliably stable). Although the time-domain operation of a hysteretic comparator can at times be intuitive, its ac transfer response in a switching converter (i.e., gain and phase) is not because linearizing what is already an inherently nonlinear circuit is difficult. This presentation illustrates how to derive a describing (rather than transfer) function that conveys more ac insight and shows how the oscillator circuit ensures there is just enough phase shift across the feedback loop to sustain oscillations (i.e., reach $180^\circ$ of phase shift at $f_{\text{0dB}} = f_{SW}$).
Summary

- Hysteretic switching converter ≡ Oscillator (i.e., \( f_{SW} = f_{0db} = f_{180} \));
- AC Response ≡ Large Signal (i.e., loop processes \( f_{SW} \) signal);
- LC eliminates higher-than-\( f_{SW} \) frequencies
  \( \therefore \) Only comparator's \( f_{SW} \) component is relevant.

\[
\text{Gain} = \frac{\Delta V_{\text{OUT}}(f_{SW})}{\Delta V_{\text{IN}}(f_{SW})} = \left(\frac{4}{\pi}\right)\frac{V_{DD}}{\Delta V_{\text{IN}(PP)}} \leq \left(\frac{4}{\pi}\right)\frac{V_{DD}}{V_{\text{Hyst}}}
\]

- If comparator's \( T_{\text{DLY}} \ll T_{SW} \) \( \therefore \) No in-band comparator pole;
- Comparator waits for \( v_{\text{IN}} \) to reach trip point
  \( \therefore 90^\circ \) if \( \Delta V_{\text{IN}} = V_{\text{Hyst}} \) AND \( < 90^\circ \) if \( \Delta V_{\text{IN}} > V_{\text{Hyst}} \);
- \( -\text{FB} \) adjusts \( \Delta V_{\text{IN}} \) (gain and phase) until oscillations are sustained.

Introduction: Problem Statement

“Hysteretic buck converters are always stable.”


• Hysteretic DC-DC Converters:
  - Simple system and intuitive operation, but always stable?
  - Output voltage ripple often exceeds hysteretic window, why?
  - Output can ring rail-to-rail when the output impedance
    lacks resistive components (e.g., \( R_{\text{ESR}} \) is low in \( C_{O} \)), why?

→ How can we explain the stability and dynamics of hysteretic comparators in switching dc-dc converters?
PWM Switching Converters

A PWM switching converter can be averaged and linearized across a switching cycle.

Hysteretic Switching Converters

- No error amp, Digital output, Circuit processes frequencies near $f_{sw}$.
  - Hysteretic comparator is difficult to linearize (i.e., extract ac transfer function).
- It is well known that the circuit sustains oscillations at $f_{sw}$, but how?
Linearizing a Hysteretic Comparator

Observations:
1) Nonlinear block
2) $T_{CP\text{.IN}} = T_{CP\text{.OUT}} \rightarrow f_{CP\text{.IN(fund)}} = f_{CP\text{.OUT(fund)}}$
3) Gain and phase-shift relationships can be defined.


Describing Function: Gain and Phase Shift

\[
\text{Gain} = \frac{\text{Output Amplitude}}{\text{Input Amplitude}}
\]

\[
\frac{4V_{DD}}{\pi} \quad \frac{2V_{DD}}{V_{C}} \quad \frac{2V_{DD}}{\pi V_{C}}
\]

\[
\text{Phase-Shift} = \omega_c t_d
\]

\[
V_c \sin(\omega_c t_d) = \frac{V_H}{2}
\]

\[
\omega_c t_d = \sin \left( \frac{\frac{V_H}{2}}{V_C} \right)
\]
**Frequency Response**

- $V_{in} = 2 \times 18.5 \text{ mV}$
- Gain and phase-shift are constant over frequency, but they change with the input ripple (i.e., with $V_n$).
- Max Gain and phase shift with min. input ripple: $V_C = V_{in}/2$.
- Gain and phase shift decreases as input ripple ($V_C$) increases.

**Loop-Gain Transfer Function**

\[
G(V_C) = \frac{2V_{DD}}{\pi V_C} \sin^{-1}\left(\frac{V_H}{2V_C}\right)
\]

\[
H(s) = \frac{1 + sR_{ESR}C_O}{1 + sR_{ESR}C_O + s^2L_OC_O}
\]

⇒ Loop-Gain = $G(V_C) \times H(s)$
The loop changes the amplitude and frequency of the input ripple to ensure $f_{0dB} = f_{180^o}$; 
- Loop sustains oscillation; 
- $f_{5W} = f_{0dB} = f_{180^o}$

Equilibrium
@ zero P.M.

Small $V_C$
(-1) P.M. $V_C$

Large $V_C$
(1) P.M. $V_C$

1
2
3
Theory vs. Simulation

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Theoretical Estimation</th>
<th>Simulated Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SW}$</td>
<td>230 KHz</td>
<td>262 KHz</td>
</tr>
<tr>
<td>$v_{OUT(Repl)}$</td>
<td>22 mV</td>
<td>20 mV</td>
</tr>
</tbody>
</table>

*Source of Error*: $v_{OUT}$ is not a sinusoidal waveform.

Conclusions

Hysteretic DC-DC Switching Converters:
- Sustained oscillation of $v_{OUT}$ about $V_{REF}$ $\rightarrow f_{0dB} = f_{180^\circ}$;
- Respond within 1 switching cycle $\rightarrow f_{0dB} = f_{SW}$;
  $\therefore$ Faster than PWM counterparts.
- Hysteretic comparator is nonlinear.

Describing Function of Hysteretic Comparators:
- Linearize by analyzing fundamental frequency;
- Supply $V_{DD}$ fixes $\Delta v_{OUT}$'s amplitude to a constant;
- Hysteresis delays (phase-shifts) response;
  $\rightarrow$ Gain and phase change with input ripple's amplitude.