Accurate CMOS Reference-Regulator Circuits

Vishal Gupta
Prof. Gabriel Rincón-Mora

Georgia Tech Analog and Power IC Design Lab

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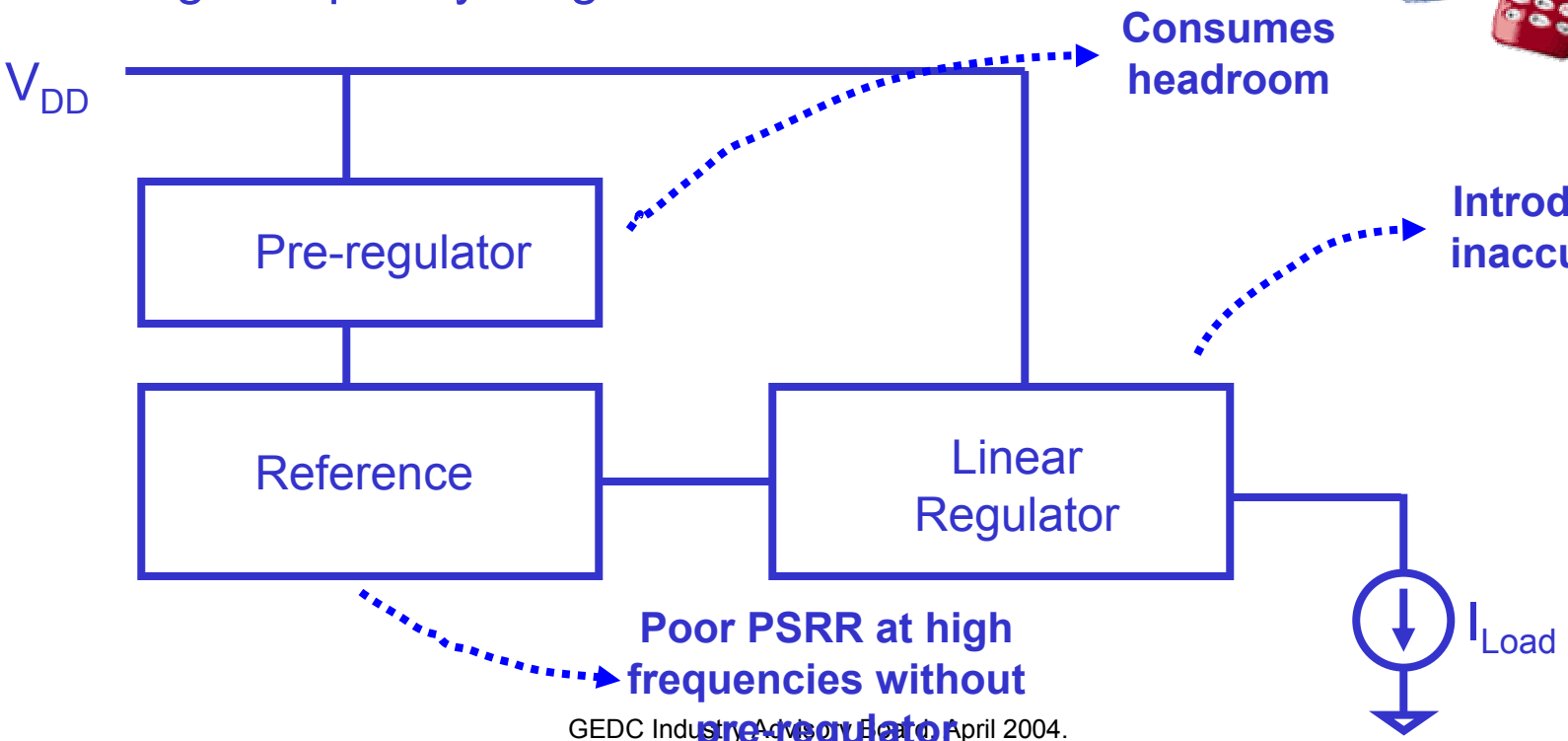
Abstract

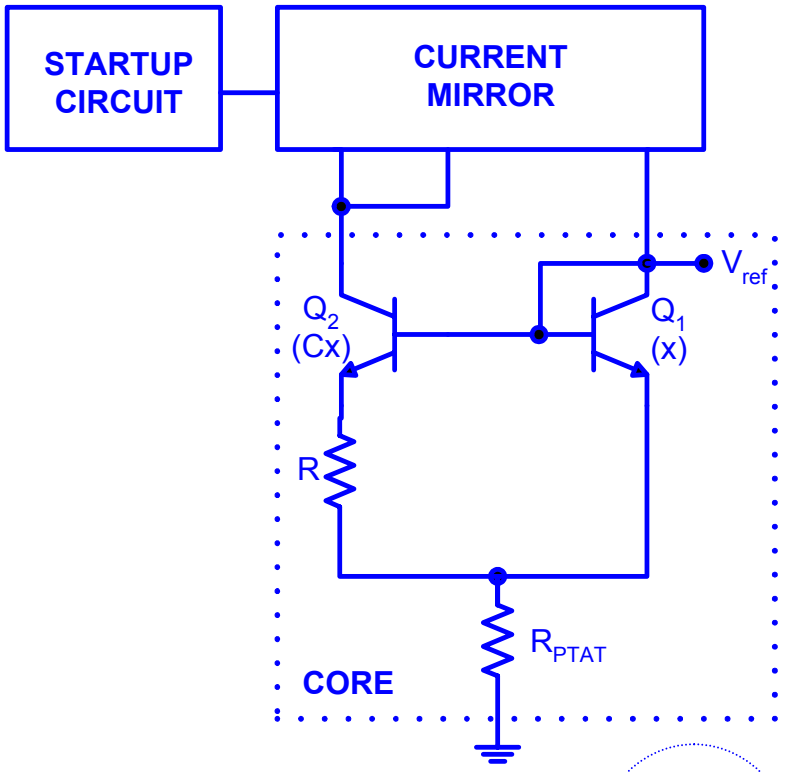
The schematics of two novel reference-regulator circuits have been presented. These use lateral PNP transistors that are available in standard CMOS technologies. The accuracy performance of these references over conventional designs is enhanced due to the use of bipolar devices as input stages of the amplifier. The low Early voltage and β-variation, characteristic of these devices, has been accounted for in the designs.

Motivation

- Mobile systems ⇒ low voltage headroom ⇒ constraints on accuracy, low dropout
- Mobile systems ⇒ SoC and SoP ⇒ noisy ⇒ linear regulators to shield load circuit from power supply noise over large frequency range.



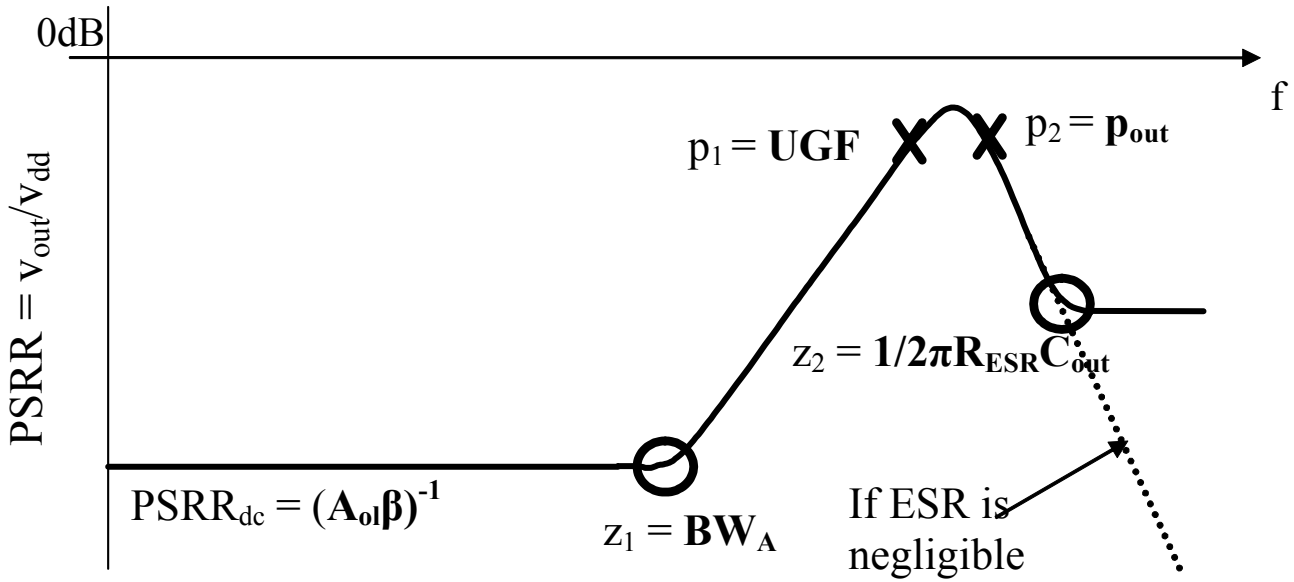
Error Sources in Bandgap References

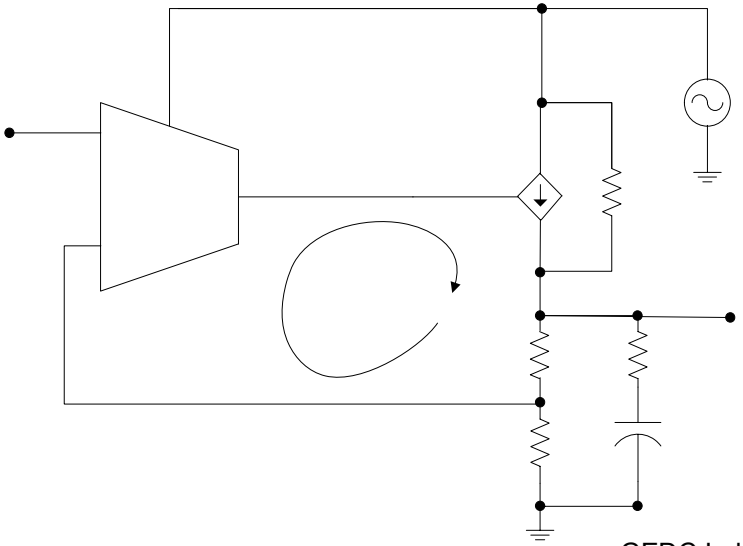


$$V_{ref} = V_{BE1} + V_T \ln(C) \frac{R_{PTAT}}{R}$$

Error	Typical Value (3-σ)	Relative Magnitude of Effect	Trimmable	Temp. Dependence
Current-Mirror Mismatch	±1 % - 10 %	Very Large	Yes	Linear
V_{BE} spread	±24 mV	Very Large	Yes	Linear
Opamp offset	±10mV	Large	No	Non-linear
Resistor Mismatch	±1 %	Large	Yes	Linear
Package Shift	±5 – 7 mV	Large	No	Non-linear
Resistor T.C.	500/°C, 200/°C^2	Large	No	Non-linear
Transistor Mismatch	±1%	Small	Yes	Linear
Early voltage, lambda	50V, 0.1	Small	No	Non-linear
Resistor Tolerance	±20 %	Small	Yes	Linear

PSRR of a linear regulator

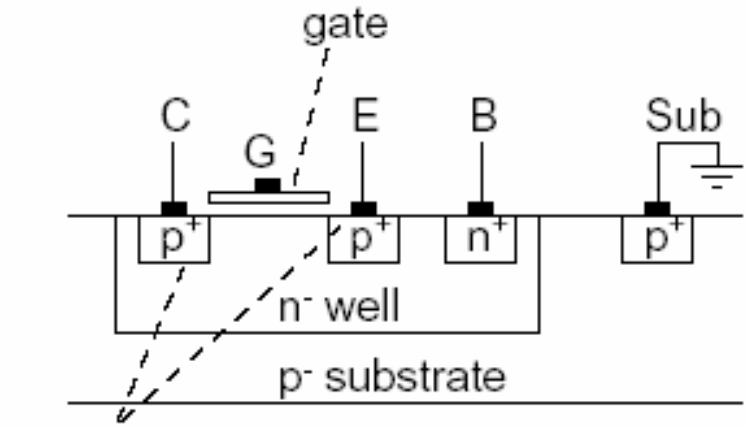


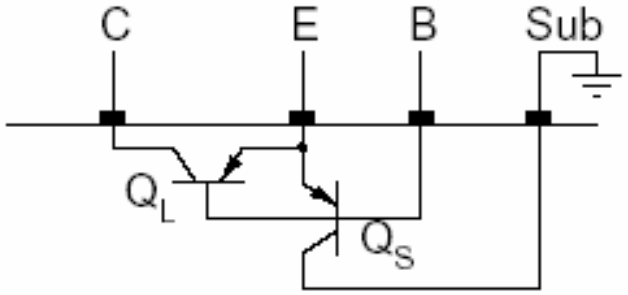


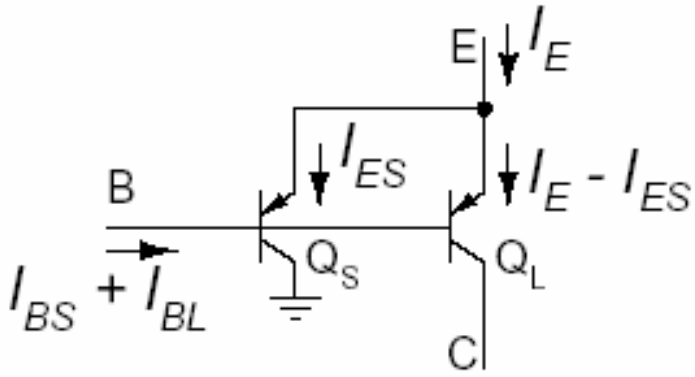
1. $A_{ol}\beta$ effective
2. opamp BW_A worsens PSRR
3. PSRR worst at UGF
4. C_{out} enhances PSRR
5. ESR limits PSRR

PSRR, loop parameters CLOSELY RELATED !!!

Characteristics of Lateral PNPs available in standard CMOS



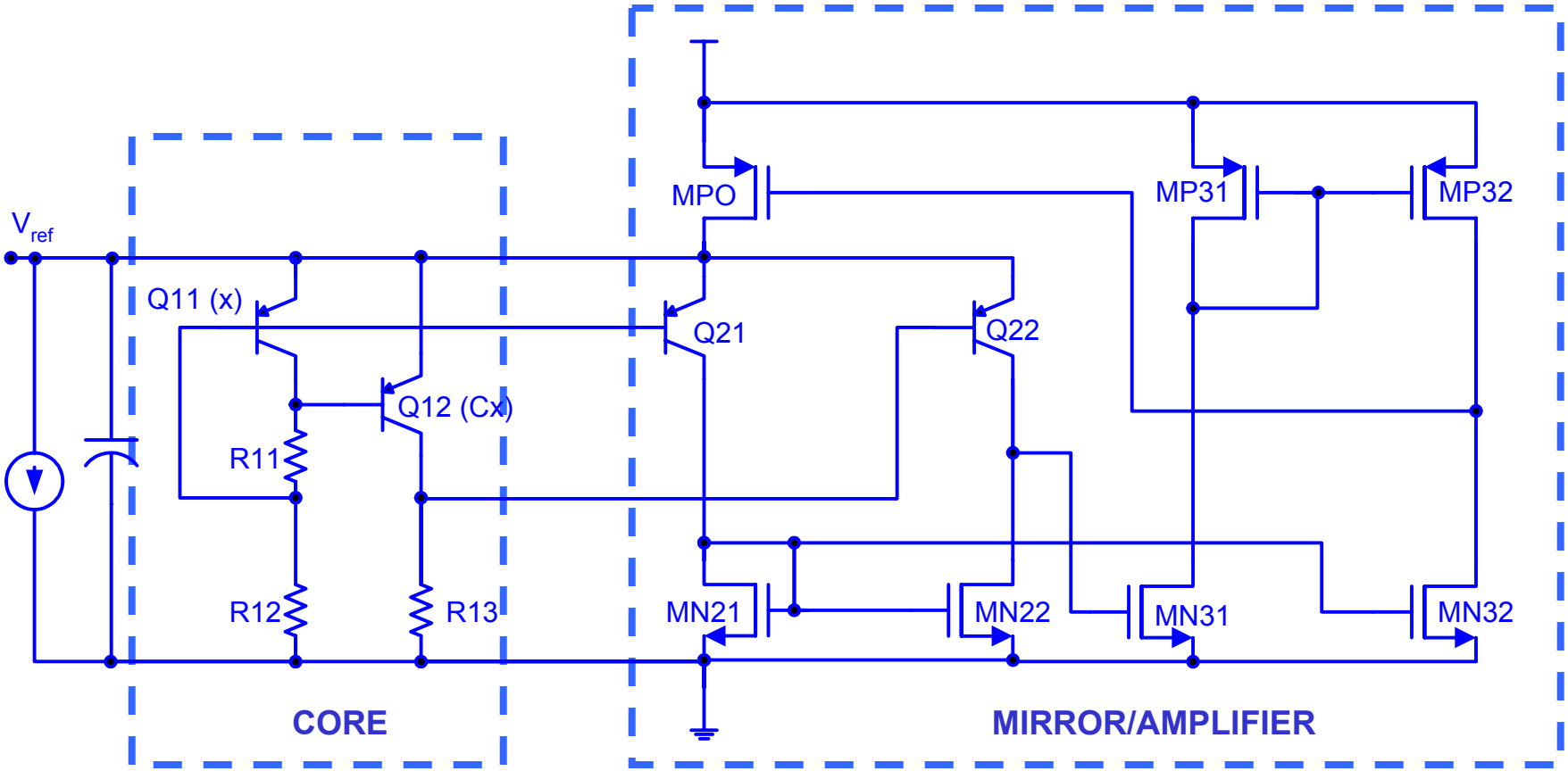




Characteristics of Lateral PNPs available in standard CMOS

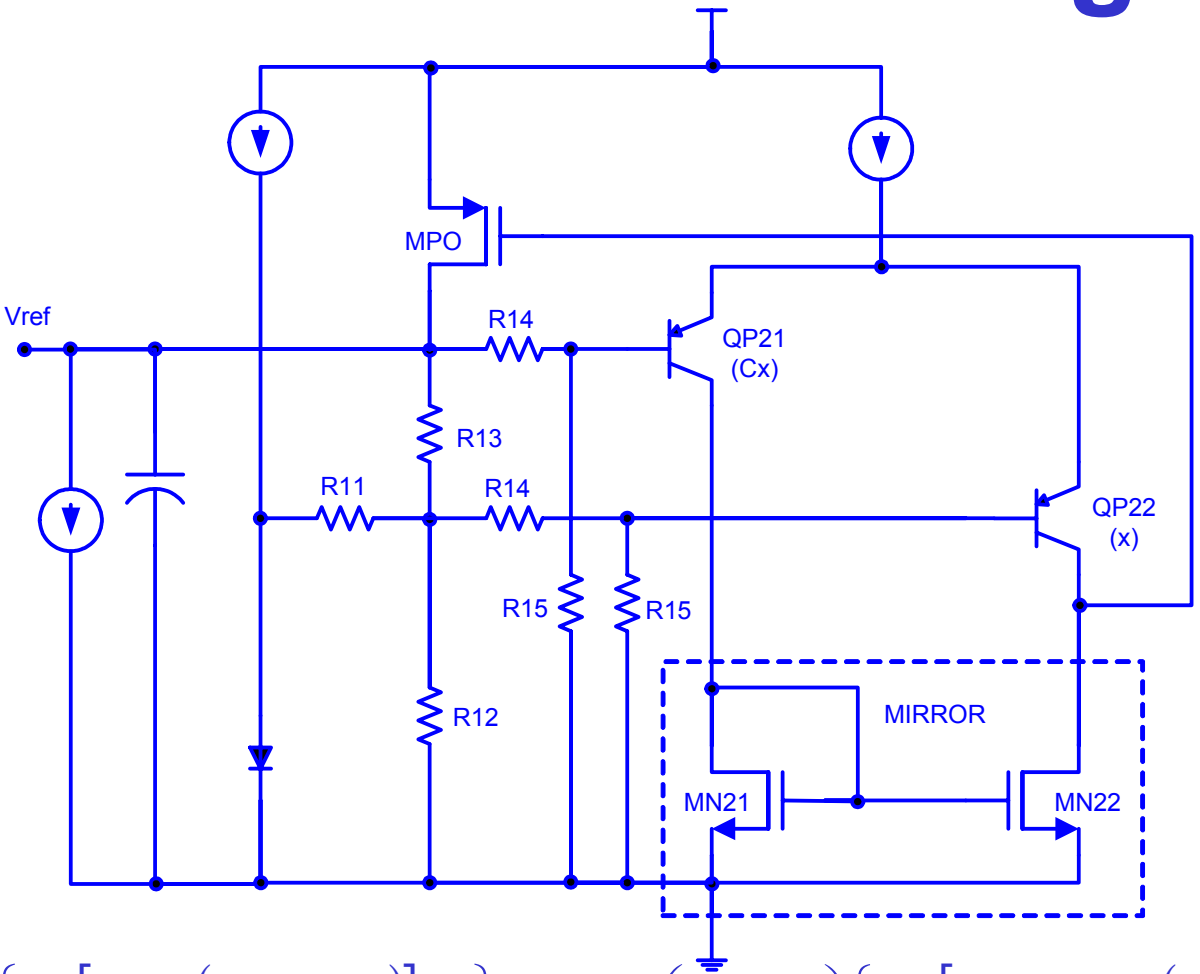
- Advantages
  - High nominal β (~50 – 100)
  - Collector not grounded ⇒ common-emitter configuration possible
- Disadvantages
  - Low Early voltage (~15V)
  - Parasitic PNP that increases power consumption

1.2V CMOS Reference Regulator



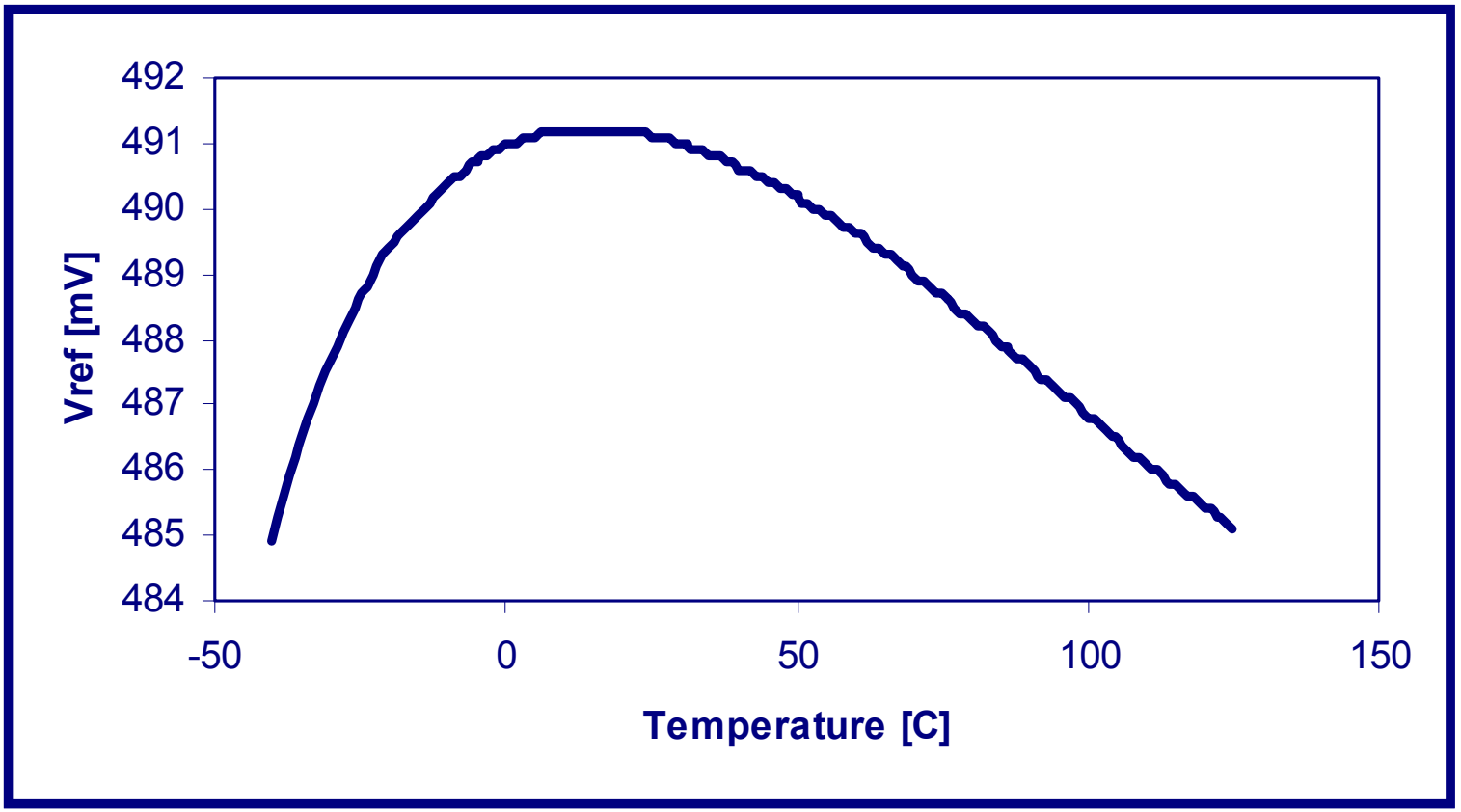
$$V_{ref} = V_{BE11} + \Delta V_{BE} \frac{R_{12}}{R_{11}}$$

0.6V CMOS Reference Regulator



$$V_{ref} = V_{BE11}\left\{\frac{\left[R_{12} \parallel (R_{14}+R_{15})\right]}{R_{11}+\left[R_{12} \parallel (R_{14}+R_{15})\right]}\right\} + \Delta V_{BE}\left(1+\frac{R_{14}}{R_{15}}\right)\left\{1+\frac{\left[R_{11} \parallel R_{12} \parallel (R_{14}+R_{15})\right]}{R_{13}}\right\}$$

Temperature coefficient of V_{ref}



Design Notes

- Since bipolar transistors have lower offset, accuracy improved by using BJTs for input stage of amplifier
- Base current errors mitigated using base-current cancellation
- Early voltage effects have been minimized by equalizing the collector-emitter voltages of the transistors.
- Bipolar transistors will not be used for gain stages since they have low Early voltage.

Future Work

- Characterize lateral PNP devices
- Verify hand calculations of accuracy of proposed topologies through Monte Carlo simulations
- Develop compensation scheme for reference-regulator circuit
- Design and fabricate circuit in a CMOS technology