An Integrated, Dynamically Adaptive Energy-Management Framework for Linear RF Power Amplifiers

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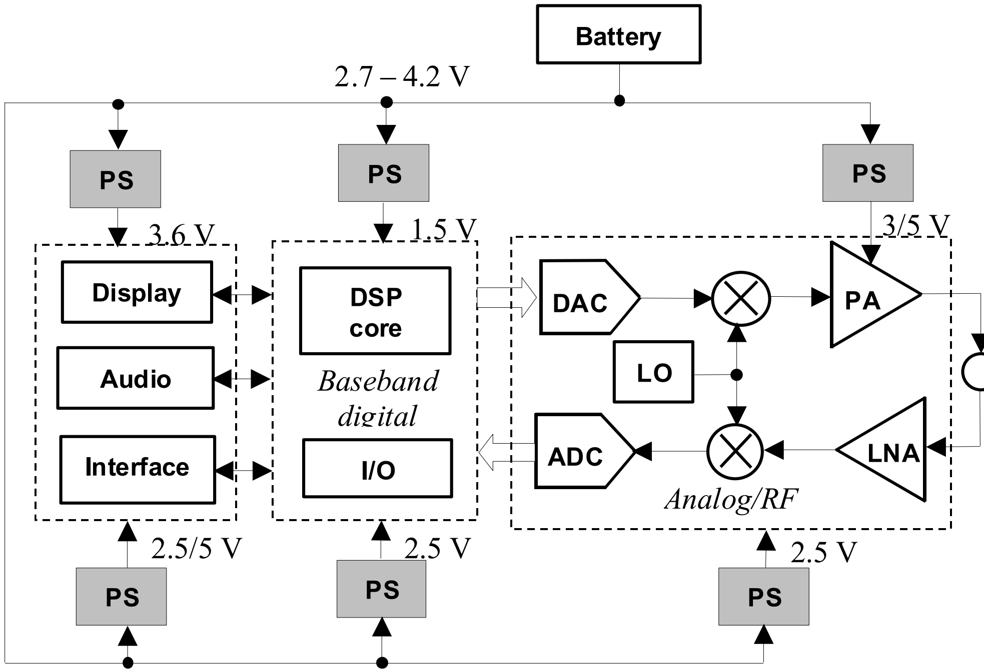
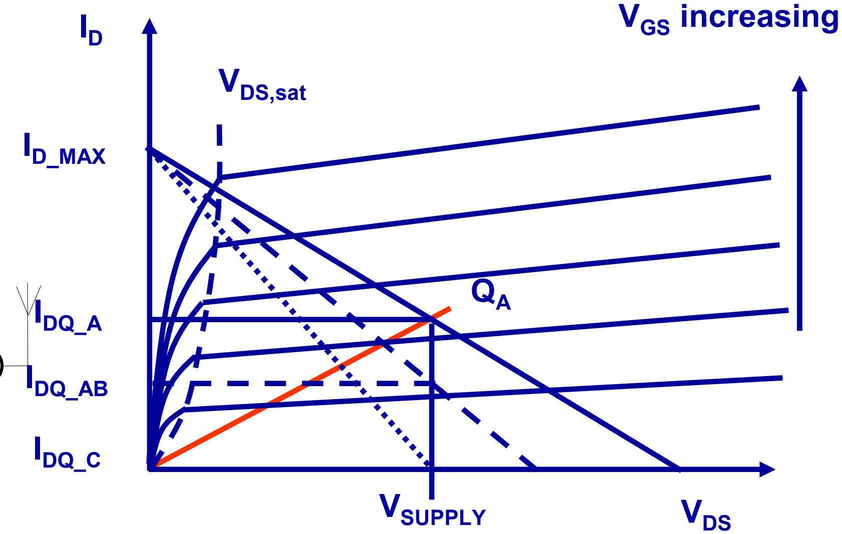
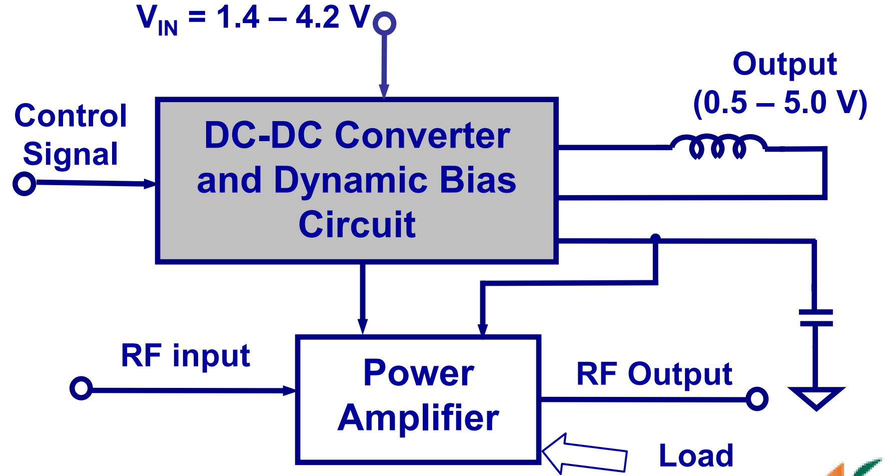
Abstract

- Energy-efficient, linear RF power amplifiers are *critical* and *paramount* to achieve *longer battery life* in state-of-the-art wireless handsets.
- In the proposed system, the energy-efficiency of a PA is improved by dynamically adjusting the supply voltage and current as a function of its transmitted power.
- System Requirements
  - ✓ High efficiency $\Rightarrow$ Improvement in battery life
  - ✓ Low voltage $\Rightarrow$ Single cell operation (***Li-ion***/NiCd/NiMH/***Fuel Cell***)
  - ✓ Integrated $\Rightarrow \downarrow$ External components, $\downarrow$ Cost
  - ✓ Low noise $\Rightarrow \downarrow$ Interference
- This work addresses the design challenges and trade-offs involved in realizing an integrated circuit (IC) for such a system with a *wide range of supply voltage*.
  - Lower limit – Minimum supply voltage for circuits to be operational (1.4 V)
  - Higher limit – Process technology constraints (5 V), AMI 0.5 μm CMOS

Energy-Efficient Linear PA

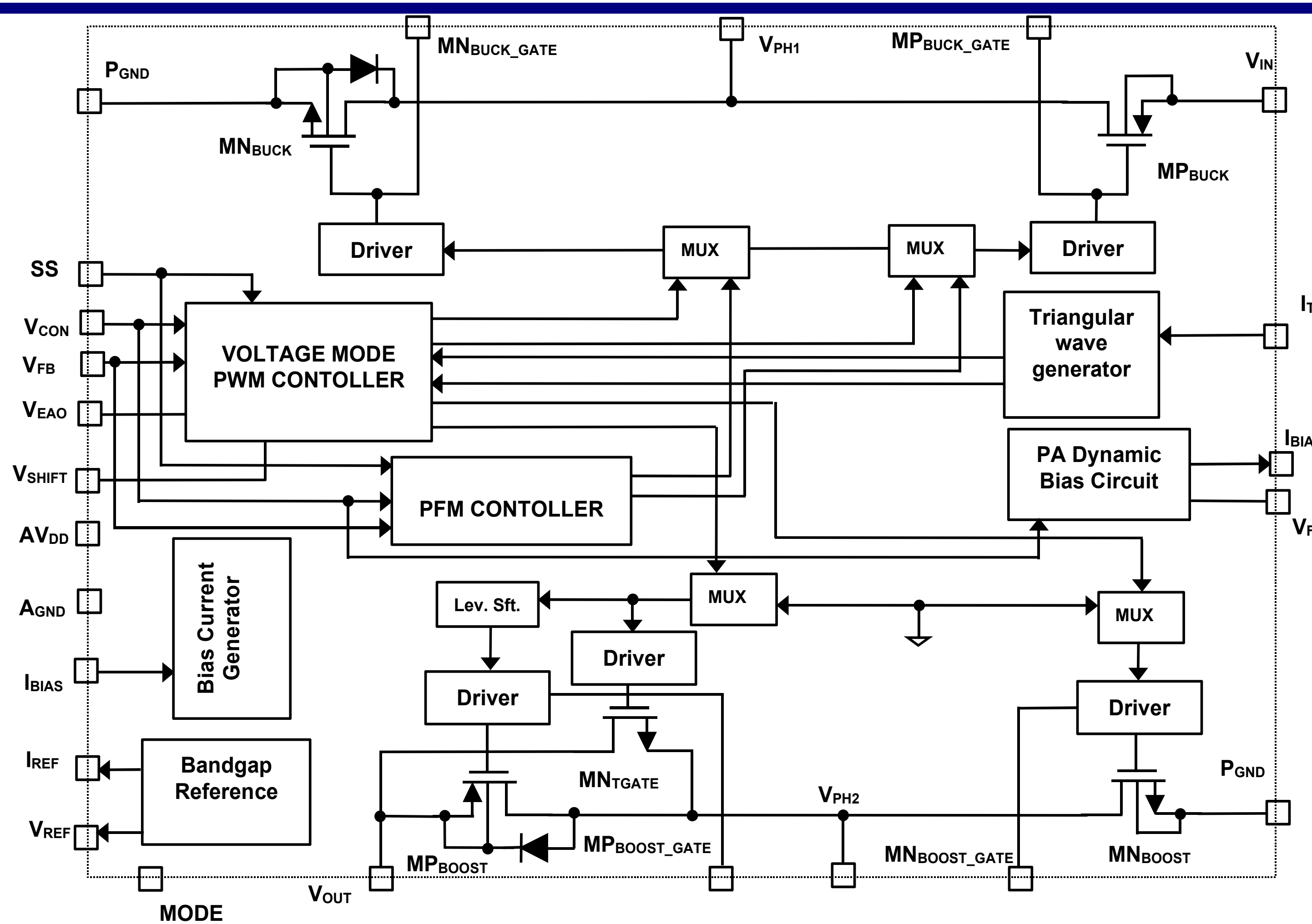






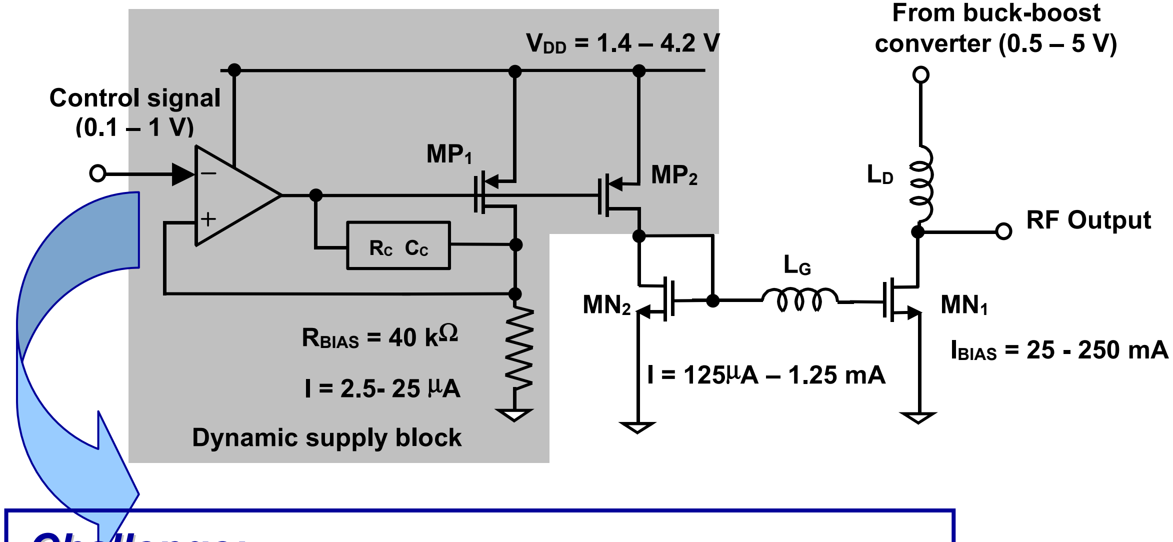
- ⇒ Reduce the input power drawn from the battery as transmitter output power decreases
- ⇒ Gain variation requires calibration with the rest of the transmitter chain

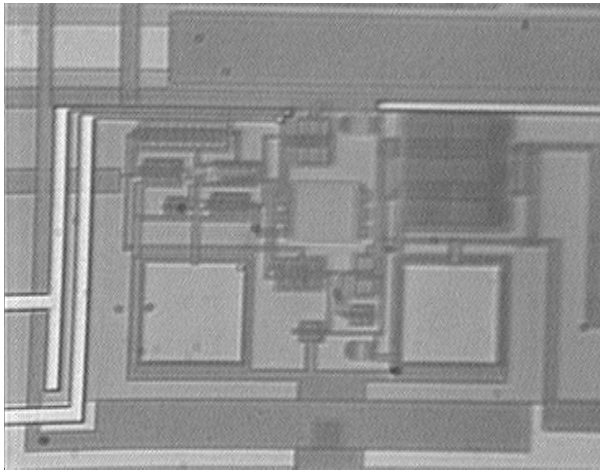
The System – An Integrated Solution



- ⇒ Integrated Power FETS
- ⇒ Dual-mode noninverting buck-boost converter for high efficiency over wide loading conditions
- ⇒ Voltage-mode PWM controller at high PA output power
- ⇒ PFM controller at light loading conditions
- ⇒ Integrated bandgap reference
- ⇒ Integrated power amplifier dynamic bias circuit

Dynamic Gate Bias Circuit

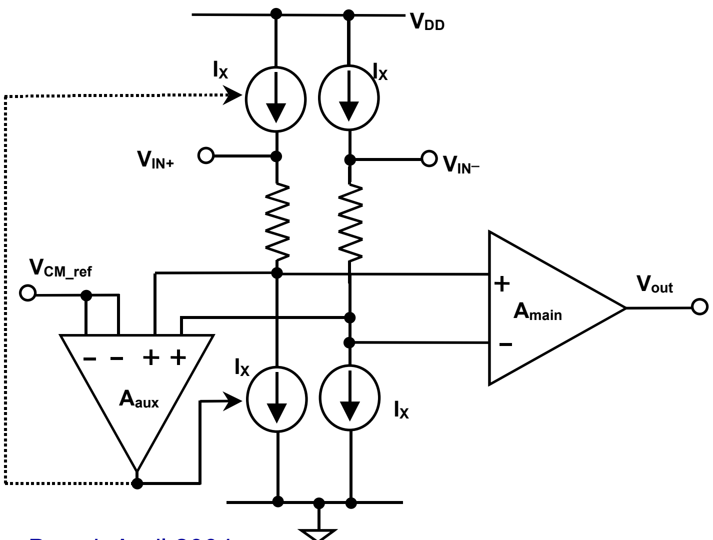




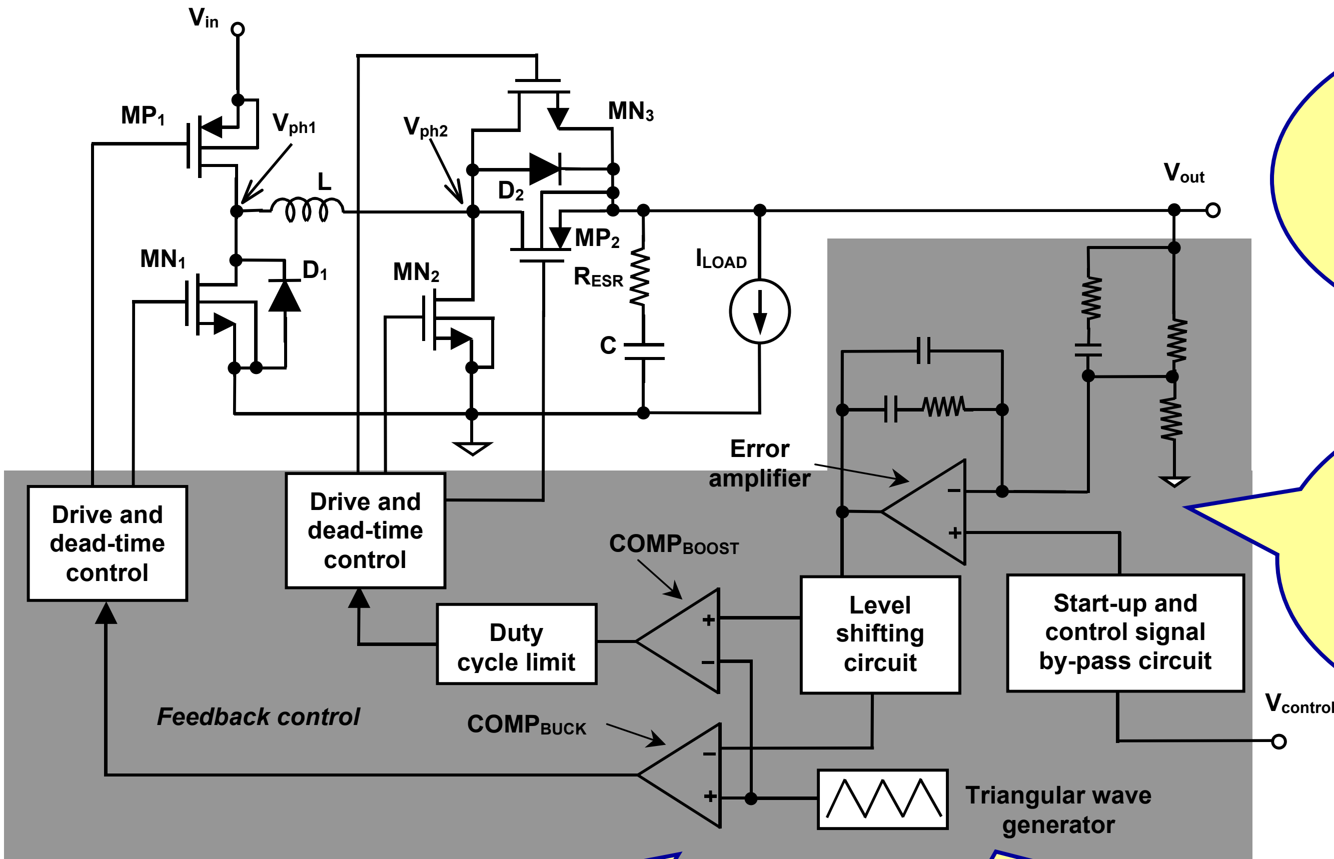
Die photo of the circuit

Challenge:
Designing an op-amp with rail-to-rail input common mode range with $V_{DD} < |V_{TP}| + V_{TN}$

⇒ **Power-supply-adaptive, common-mode feedforward circuit**
⇒ **Auxiliary amplifier sets the common-mode signal for the main amplifier only when required**
⇒ **Added power consumption, noise, offset**



Buck-Boost Converter – PWM Mode



V_{IN} = 1.4 V – 4.2 V
V_{OUT} = 0.5 V – 5 V
$V_{RIPPLE} \leq$ 10 - 100 mV
Voltage mode control
Type–III compensation

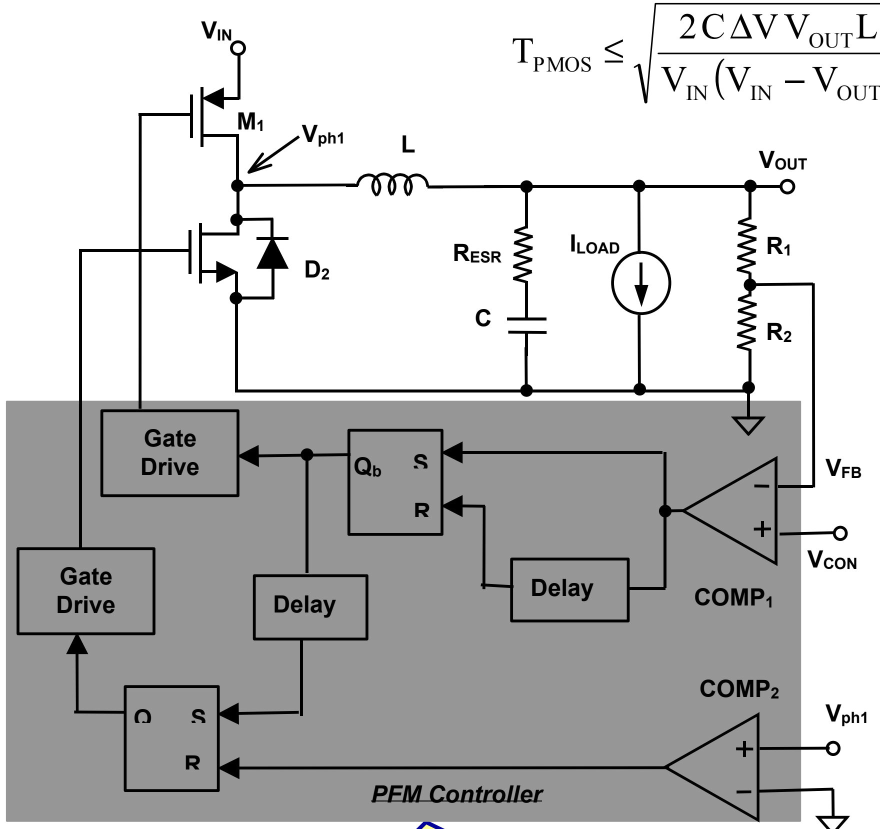
Error amplifier
Gain : ≥ 70 dB
ICMR : 0.1 – 1 V
OS : 0.2 V – (V_{DD} - 0.2 V)
Input Offset: ≤ 10 mV

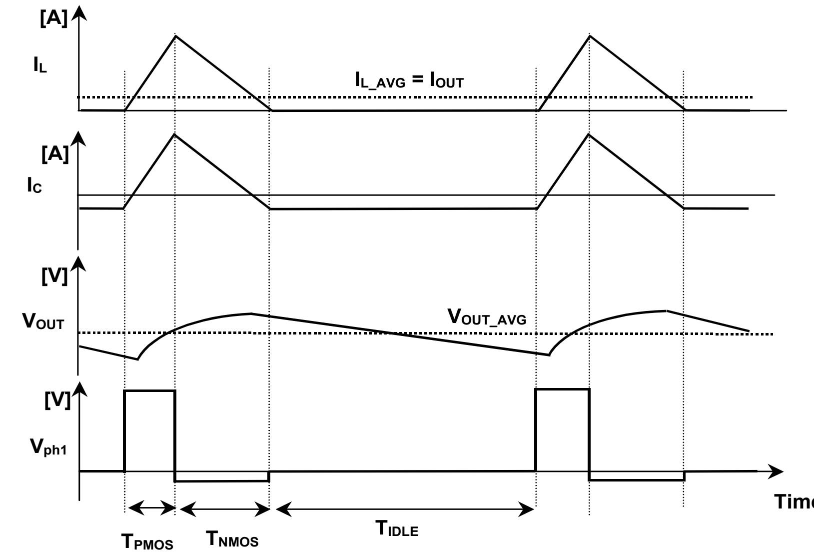
PWM Comparators
ICMR : 0.9 V – 1.25 V
Prop. Delay : ≤ 100 ns
Input Offset: ≤ 10 mV

Triangular wave generator
V_{TW} = 0.95 V – 1.25 V
Freq.= 0.9 – 1.1 MHz

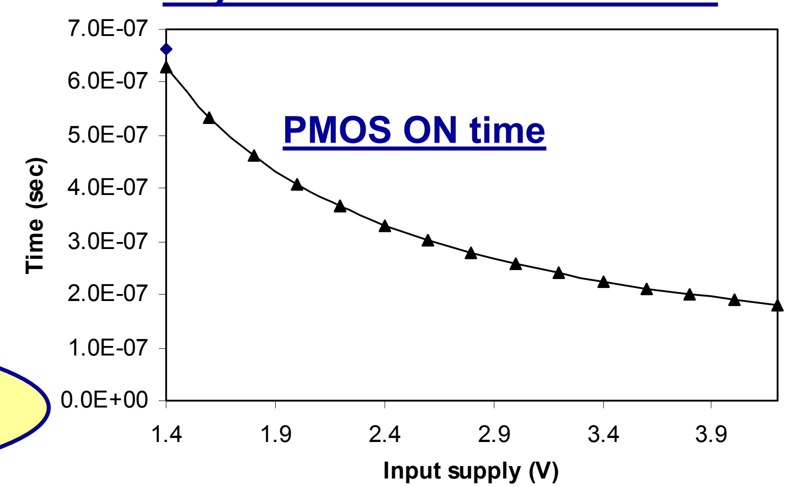
Buck-Boost Converter – PFM Mode

$$T_{PMOS} \le \sqrt{\frac{2C\,\Delta V\,V_{OUT}L}{V_{IN}\left(V_{IN}-V_{OUT}\right)}}$$





Key Waveforms in PFM Control



VARIABLE DELAY BLOCK

Required delay is inversely proportional to V_{DD}

Larger $V_{DD} \Rightarrow$ lower $T_{ON} \Rightarrow$ PMOS $\Rightarrow I_L$ desired

The Building Blocks

Error amplifier Op-amp

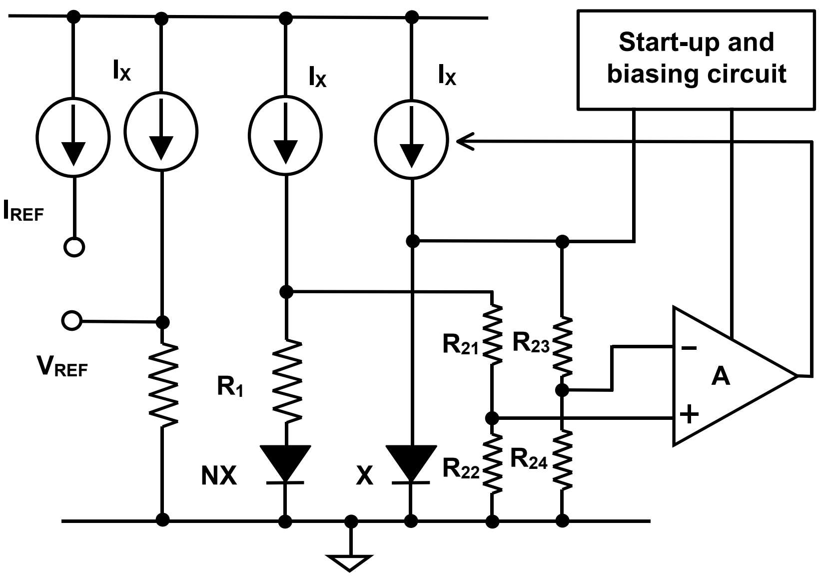
- **Input common-mode range (ICMR)**
  - By dynamically shifting the input signal as a function of supply voltage, a PMOS input stage is used.
  - $\Rightarrow$ ICMR $\uparrow$, Noise $\uparrow$, Offset voltage $\uparrow$
- **Input Offset Voltage**
  - Error in output voltage = Offset voltage $\times$ Closed loop gain of the converter.
  - Depending on the accuracy requirement, offset cancellation techniques can be used.
- **DC Gain and Bandwidth**
  - As DC gain $\uparrow$, steady-state error $\downarrow$
  - $UGF_{OPAMP} >> \text{Loop } BW_{CONVERTER}$
- **Architecture similar to the dynamic bias circuit**

Bandgap reference

$I_{REF} = I_{PTAT} + I_{CTAT}$

$V_{REF} = I_{REF}R$

Substrate vertical PNPs as diodes



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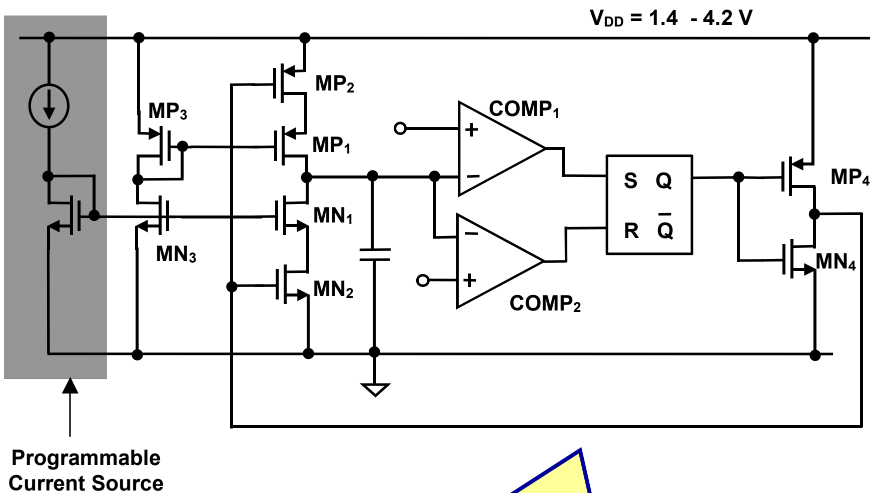
The Building Blocks

Triangular Wave Generator



Comparators
ICMR : 0.9 V – 1.25 V
Prop. Delay : ≤ 100 ns
Input Offset: ≤ 10 mV

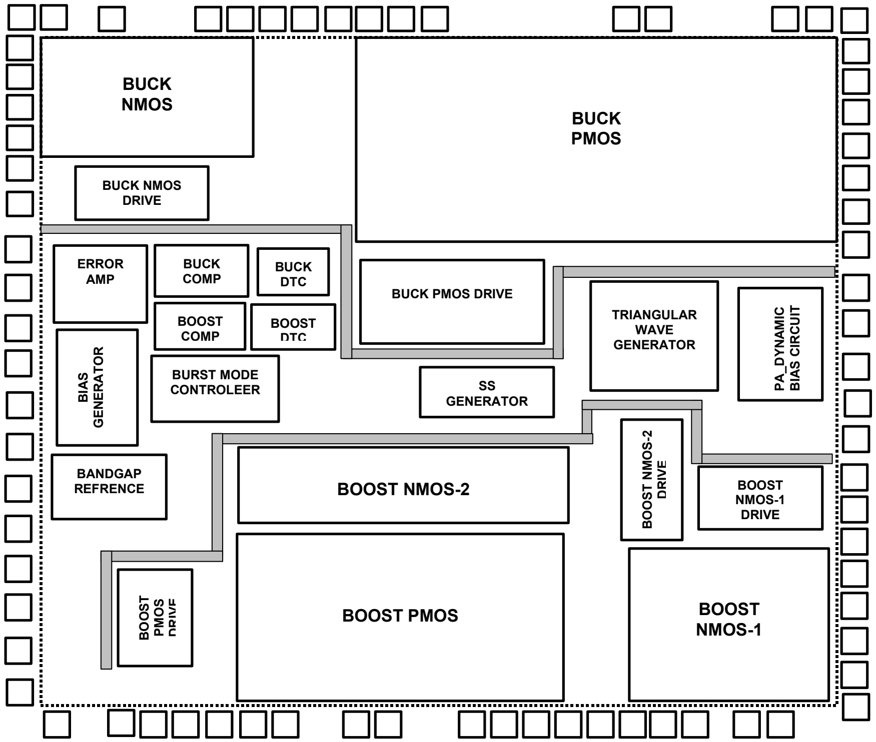
Spread spectrum triangular wave by adjusting the charging/discharging current dynamically

Potential reduction in EMI and noise

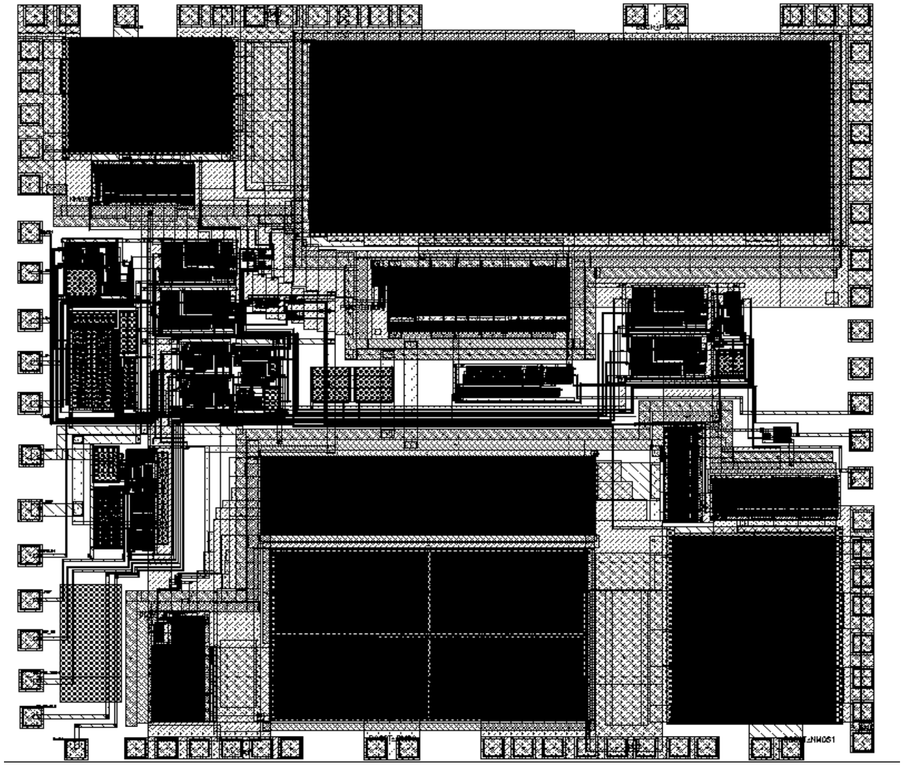
Performance Summary of the Converter

Specifications	*Target*	*Sims.*
Input voltage (V)	1.4 – 4.2	1.4 – 4.2
Voltage mode PWM controller		
Output voltage (V)	0.5 – 5	0.5 – 5
Peak-to-peak ripple (mV)	≤ 10 – 100	≤ 2 – 47
Efficiency (%)	–	60-97 %
Quiescent current (mA)	–	1
PFM controller		
Output voltage (V)	0.5	0.5 – 0.51
Peak-to-peak ripple (mV)	≤ 50	≤20 – 36
Efficiency (%)	–	50 – 84 %
Quiescent current (μA)	–	200

Layout of the System



System Floor Plan



System Layout

Layout size: 3.5 mm × 3.3 mm – Power transistor area more than 75 %

Targeted Package: LCC 44 – Design for Testability

Summary

- IC design issues of key building blocks of a new energy-management system for linear RF PA is discussed. Key challenges with respect to implementation of low-voltage circuits are addressed.
- **System Efficiency Enhancement**
  - Nominal voltage and current at peak PA output power
  - Reduced supply and current as PA output power reduces
- **Buck-Boost Converter Performance Enhancement**
  - PWM Mode at full/mode load, PFM Mode at light load
  - Buck/Buck-Boost/Boost Mode of operation
  - DC accuracy ⇒ Low –offset, wide input common-mode range op-amp for error amplifier
  - Ripple voltage/Noise spectrum ⇒ Spread-spectrum clocking
  - Transient accuracy ⇒ Higher bandwidth, slew rate
- **Future Work:** *Performance evaluation of the IC*

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