An Integrated, Dynamically Adaptive Energy-Management Framework for Linear RF Power Amplifiers

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Abstract

- Energy-efficient, linear RF power amplifiers are *critical* and *paramount* to achieve *longer battery life* in state-of-the-art wireless handsets.

- In the proposed system, the energy-efficiency of a PA is improved by dynamically adjusting the supply voltage and current as a function of its transmitted power.

- **System Requirements**
  - ✓ High efficiency ⇒ Improvement in battery life
  - ✓ Low voltage ⇒ Single cell operation (*Li-ion*/NiCd/NiMH/*Fuel Cell*)
  - ✓ Integrated ⇒ ↓ External components, ↓ Cost
  - ✓ Low noise ⇒ ↓ Interference

- This work addresses the design challenges and trade-offs involved in realizing an integrated circuit (IC) for such a system with a *wide range of supply voltage*.
  - Lower limit – Minimum supply voltage for circuits to be operational (1.4 V)
  - Higher limit – Process technology constraints (5 V), AMI 0.5 μm CMOS
Energy-Efficient Linear PA

⇒ Reduce the input power drawn from the battery as transmitter output power decreases

⇒ Gain variation requires calibration with the rest of the transmitter chain
The System – An Integrated Solution

⇒ Integrated Power FETS
⇒ Dual-mode noninverting buck-boost converter for high efficiency over wide loading conditions
⇒ Voltage-mode PWM controller at high PA output power
⇒ PFM controller at light loading conditions
⇒ Integrated bandgap reference
⇒ Integrated power amplifier dynamic bias circuit
Dynamic Gate Bias Circuit

**Challenge:**

*Designing an op-amp with rail-to-rail input common mode range with $V_{DD} < |V_{TP}| + V_{TN}$*

⇒ Power-supply-adaptive, common-mode feedforward circuit
⇒ Auxiliary amplifier sets the common-mode signal for the main amplifier only when required
⇒ Added power consumption, noise, offset
Buck-Boost Converter – PWM Mode

Vin

Vout

MN2

MP2

D2

D1

MP1

MN1

L

C

RESR

Vph1

Vph2

Vcontrol

Vout

Error amplifier

Gain : ≥ 70 dB
ICMR : 0.1 – 1 V
OS : 0.2 V – (VDD - 0.2 V)
Input Offset: ≤ 10 mV

PWM Comparators
ICMR : 0.9 V – 1.25 V
Prop. Delay : ≤ 100 ns
Input Offset: ≤ 10 mV

Triangular wave generator

VTW = 0.95 V – 1.25 V
Freq. = 0.9 – 1.1 MHz

VIN = 1.4 V – 4.2 V
VOUT = 0.5 V – 5 V
VRIPPLE ≤ 10 - 100 mV
Voltage mode control
Type–III compensation

Drive and dead-time control
Drive and dead-time control
Duty cycle limit
Feedback control
COMPBUCK
COMPBOOST
Level shifting circuit
Start-up and control signal by-pass circuit

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Buck-Boost Converter – PFM Mode

\[ T_{\text{PMOS}} < \frac{2C \Delta V V_{\text{OUT}} L}{V_{\text{IN}} (V_{\text{IN}} - V_{\text{OUT}})} \]

- VARIABLE DELAY BLOCK
  - Required delay is inversely proportional to \( V_{\text{DD}} \)
  - Larger \( V_{\text{DD}} \) ⇒ lower \( T_{\text{ON}} \) ⇒ PMOS ⇒ \( I_L \) desired

Key Waveforms in PFM Control

- PMOS ON time

\[ I_L, \quad I_{\text{OUT}} \]

\[ V_{\text{OUT}} \quad V_{\text{OUT}, \text{AVG}} \]

\[ T_{\text{PMOS}}, \quad T_{\text{NMOS}}, \quad T_{\text{IDLE}} \]

Input supply (V) vs. Time

Gate Drive

Delay

PMOS

VFB

VFB

COMP1

COMP2

PFM Controller
The Building Blocks

Error amplifier Op-amp

- Input common-mode range (ICMR)
  - By dynamically shifting the input signal as a function of supply voltage, a PMOS input stage is used.
  - $\Rightarrow$ ICMR ↑, Noise ↑, Offset voltage ↑

- Input Offset Voltage
  - Error in output voltage = Offset voltage $\times$ Closed loop gain of the converter.
  - Depending on the accuracy requirement, offset cancellation techniques can be used.

- DC Gain and Bandwidth
  - As DC gain ↑, steady-state error ↓
  - $\text{UGF}_{\text{OPAMP}} \gg \text{Loop BW}_{\text{CONVERTER}}$

- Architecture similar to the dynamic bias circuit

Bandgap reference

$I_{\text{REF}} = I_{\text{PTAT}} + I_{\text{CTAT}}$

$V_{\text{REF}} = I_{\text{REF}}R$

Substrate vertical PNPs as diodes
The Building Blocks

Triangular Wave Generator

Programmable Current Source

V_{DD} = 1.4 - 4.2 V

Comparators
ICMR : 0.9 V – 1.25 V
Prop. Delay : ≤ 100 ns
Input Offset: ≤ 10 mV

Spread spectrum triangular wave by adjusting the charging/discharging current dynamically

Potential reduction in EMI and noise

Performance Summary of the Converter

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Target</th>
<th>Sims.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (V)</td>
<td>1.4 – 4.2</td>
<td>1.4 – 4.2</td>
</tr>
<tr>
<td>Output voltage (V)</td>
<td>0.5 – 5</td>
<td>0.5 – 5</td>
</tr>
<tr>
<td>Peak-to-peak ripple (mV)</td>
<td>≤ 10 – 100</td>
<td>≤ 2 – 47</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>–</td>
<td>60-97 %</td>
</tr>
<tr>
<td>Quiescent current (mA)</td>
<td>–</td>
<td>1</td>
</tr>
</tbody>
</table>

Voltage mode PWM controller

| Output voltage (V)               | 0.5 | 0.5 – 0.51 |
| Peak-to-peak ripple (mV)         | ≤ 50 | ≤ 20 – 36 |
| Efficiency (%)                   | –   | 50 – 84 % |
| Quiescent current (µA)           | –   | 200 |

PFM controller
Layout of the System

System Floor Plan
Layout size: 3.5 mm × 3.3 mm – Power transistor area more than 75%
Targeted Package: LCC 44 – Design for Testability

System Layout
Summary

- IC design issues of key building blocks of a new energy-management system for linear RF PA is discussed. Key challenges with respect to implementation of low-voltage circuits are addressed.

- **System Efficiency Enhancement**
  - Nominal voltage and current at peak PA output power
  - Reduced supply and current as PA output power reduces

- **Buck-Boost Converter Performance Enhancement**
  - PWM Mode at full/mode load, PFM Mode at light load
  - Buck/Buck-Boost/Boost Mode of operation
  - DC accuracy ⇒ Low –offset, wide input common-mode range op-amp for error amplifier
  - Ripple voltage/Noise spectrum ⇒ Spread-spectrum clocking
  - Transient accuracy ⇒ Higher bandwidth, slew rate

- **Future Work:** *Performance evaluation of the IC*