Integrating Large Filter / Compensation Capacitors for SoC Applications

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Capacitor Multipliers

- **WHY ?** Capacitors supply large transient current and significantly reduce voltage fluctuations
- **DEMAND:** Low voltage, low power and small area
- **PROBLEM:** Large capacitors occupy too much silicon area
- **GOAL:** To design circuits that "multiply" the capacitance of small capacitors - **Capacitor Multipliers**

Capacitor Multiplication Techniques

I - Merged Transistor

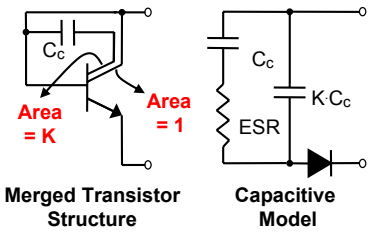
- $C_{eff} = (K+1)C_C$ - Capacitor Multiplication Factor = **"K+1"**

ADVANTAGES

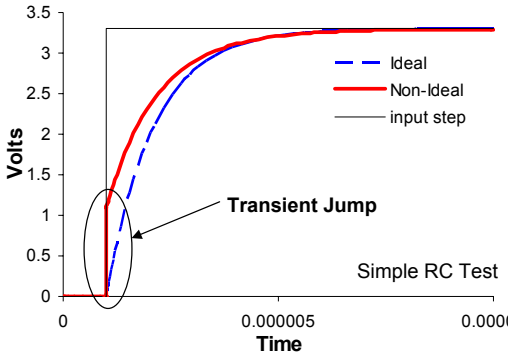
- Easily integrated
- C_{eff} dependant on K only and varies little with temperature and process
- No DC biasing requirement

DISADVANTAGES

- For high K values, C_{eff} increases but transistor mismatch degrades accuracy
- Undesired transient jump

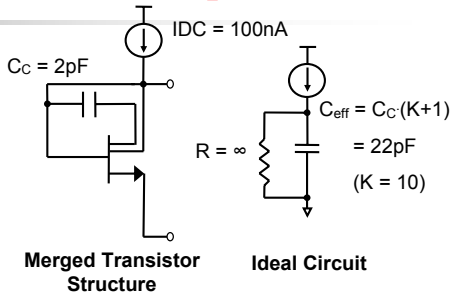


Merged Transistor Structure | Capacitive Model

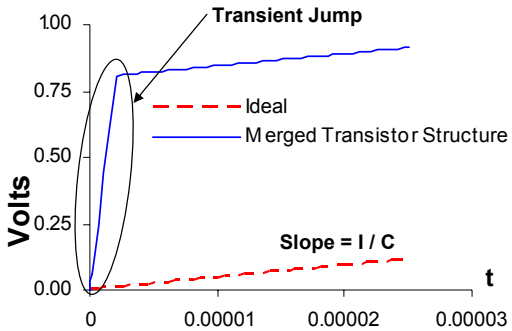


I - Merged Transistor Undesired Transient Jump

- Ideal response to a constant current = I / C = 100nA/22pf
- Merged transistor response = 100nA/22.1pf
- Accuracy = 99.5 %
- **However:** undesired transient jump (Y-intercept of top trace) is ~0.8 V.
- The Y-intercept depends directly on the V_T of the transistors.



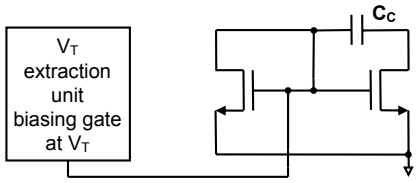
Merged Transistor Structure | Ideal Circuit

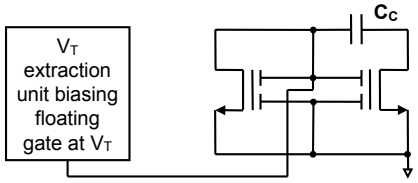


I - Merged Transistor Eliminating Transient Jump

(Current Research)

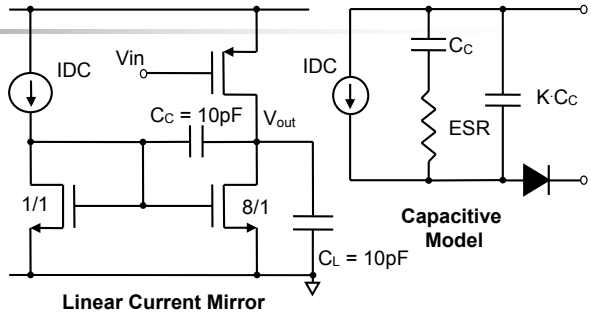
- Transient jump occurs because parasitic capacitance C_{GS} is charged first to V_{GS} for transistors to start conducting current
- Biasing gate at V_T will thus eliminate transient jump
- Simple V_T extraction circuit used for biasing purposes
- Floating-Gate transistors used to store charge on gate





II - Linear Mirror

- Without capacitor C_C the dominant pole $p_1 = \frac{1}{2}\cdot\pi\cdot R_{out}\cdot C_L = 112KHz$
- With C_C the dominant pole becomes $p_2 = \frac{1}{2}\cdot\pi\cdot R_{out}\cdot C_{eff} = 11.4$ KHz, where $C_{eff} = C_L + (K+1)\cdot C_C$
- $p_2 = p_1/10$ therefore C_{eff} is increased by a factor of 10, when C_C was added



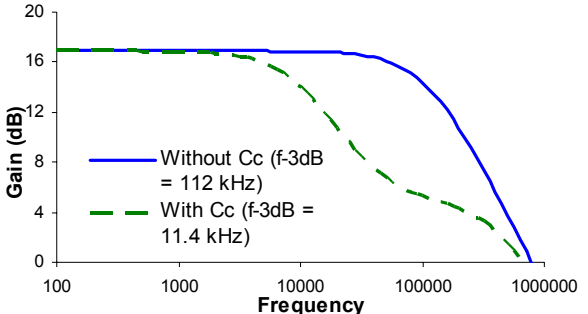
Linear Current Mirror Structure

ADVANTAGES

- C_{eff} is dependant on K only and varies little with temperature and process

DISADVANTAGES

- Adding C_C will introduce a LHP Zero @ $Z = \frac{1}{2}\cdot\pi\cdot ESR\cdot C_C$
- C_{eff} increases with K but, transistor mismatch is a limiting factor
- Requires DC Bias current

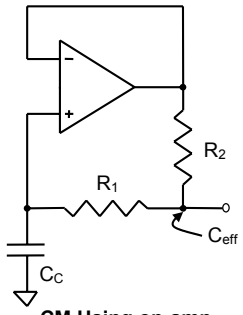


III - Op-Amp

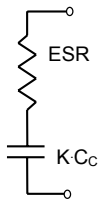
- The node between R_1 and R_2 constitutes the terminal of an effective capacitance to ground given by

$$C_{eff} = C_C \cdot (R_1/R_2)$$

- Since R_2 determines the ESR of C_{eff} a small value is desired for accuracy.



CM Using op-amp



Capacitive Model

ADVANTAGES

- Large effective capacitances can be achieved at the expense of resistive die area
- Temperature dependence of the resistors cancel

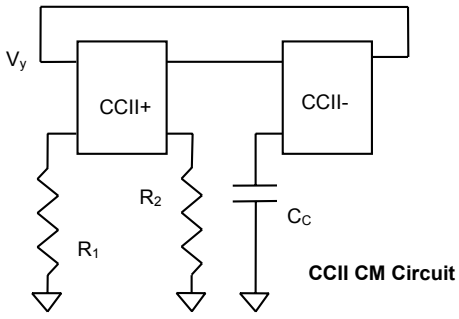
DISADVANTAGES

- Circuit Complexity

IV - Current Conveyor

- Assuming ideal CCIIs, the equivalent effective capacitance at V_y is

$$C_{eff} = C_C \cdot (R_2/R_1)$$



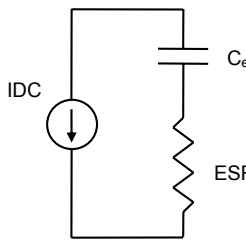
CCII CM Circuit

ADVANTAGES

- This circuit can provide capacitive gain of up to 10^3.
- Higher gain is achieved by exploiting the current gain features of the two CCIIs.

DISADVANTAGES

- A DC Bias current has to be supplied
- Power dissipation increases with current gain
- Circuit complexity
- CCII non-idealities diminish higher gain.



Capacitive Model

Summary Table

Technique	Merged Transistor	I - Mirror	Op - Amp	CCII
Area	Lowest	Low	High	Highest
Undesired Transient Jump	Yes	No	No	No
Circuit Complexity	Low	Low	High	Highest
Ceff Terminals	Floating	Floating	Floating	Floating
Temperature Dependence	Moderate	Moderate	Low	Low
Accuracy	Moderate	Moderate	High	High
Gain	Moderate	Moderate	High	Highest
DC Current Drain	No	Yes	No	Yes

Conclusion

- Merged transistor technique best in terms of area and circuit complexity
- Merged transistor structure has undesired transient jump associated with it
- Current conveyor technique best in terms of gain
- Current conveyor and linear mirror techniques require DC bias current