Abstract

• **Motivation for Improving Efficiency in Mobile Applications**
  
  **System-On-Chip (SOC)**
  
  Low power demands, low cost, and compactness make SOC suitable for portable, battery-powered applications, like cellular phones, pagers, laptop computers, MP3 players, PDAs, etc.

  **Low-voltage circuits**
  
  Required to satisfy the demand for single battery operation and the ever decreasing breakdown voltages of state-of-the-art technologies

  **Highly efficient, totally integrated DC-DC converters** are strongly desired!

  - High Efficiency ➔ Low current drain ➔ Maximum battery life
  - Total integration ➔ Small size and weight ➔ Optimum portability

• **Research Focus**
  
  Develop *power-saving techniques* for *low voltage* DC-DC converters suitable for *integrated solutions.*
Light load efficiency – Why is it important?

Most people use the cell phone for small amounts of time. Improving **light load efficiency is important** for extending battery life!

<table>
<thead>
<tr>
<th>Probability Density of Cell Phone Usage</th>
<th>CDMA RF PA Output Characteristic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak usage time (normalized) = 0.03 (s/s) or 300 min/month</td>
<td>Peak usage current (normalized) = 0.005 (A/A) or 7 dBm output power</td>
</tr>
</tbody>
</table>

Most of the time, the PA operates with small current.

Power Losses – Where do they come from?

**Conduction Losses**

(through resistive elements)
- PMOS on-resistance
- NMOS on-resistance
- Body diodes
- Inductor Equivalent Series Resistance (ESR)
- Capacitor ESR
- Gate resistances

**Switching Losses**
- V-I overlap loss
  Voltage falling and current rising overlap vice versa during MOSFET turn on/off.
- Gate drive loss
  Charging and discharging of gate capacitances during switching.

**Thermal Losses**
- Cooling devices
- As T increases, $R_{ON}$ thus conduction losses increase.

**Efficiency**

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}$$

**General Power Equations:**

- Load current: $P_{load} = D \times I_{load} \times R_{eq}$
- RMS current: $P_{ RMS} = D \times (\frac{\Delta I}{12}) \times R_{eq}$
- Body diodes: $P_{body} = t_d \times V_d \times (I_{load} + \Delta I / \sqrt{12}) \times f_s$
- V-I overlap loss: $P_{V-I} = t_s \times V_{in} \times I_{load} \times f_s$
- Gate drive loss: $P_{GD} = (16/3) \times C_{gs} \times V_t^2 \times f_s$

How to improve efficiency? – Existing techniques

1. Mode Hopping: Hop to most efficient mode based on operating conditions

- At high load:
  - Syn. CCM: Smaller $\propto I$, thus smaller conduction losses
  - More efficient than DCM

- At light load:
  - Asyn. DCM: Smaller $\propto I$, thus smaller conduction losses
  - Also may decrease $f_s$, thus smaller switching losses
  - More efficient than Syn. DCM

Load dependent Mode Hopping to keep high efficiency over wide load range

Challenge: Need to sense $I_L$ to determine the correct operation mode

One solution: Disable NMOS periodically to force Asyn. DCM without current sensing
But converter latches in DCM even after enabling NMOS

Improvement: Disable NMOS after sensing ringing at $V_{ph}$ to save gate drive loss


2. Variable Frequency

- Switching losses ($\propto f_s$) dominate at light loads

- Reduce $f_s$ in proportional to $I_{load}$

- Light load efficiency is significantly improved

- At heavy loads, switching losses are still high

3. Hybrid Control

- Mode Hopping + Variable Frequency

- Constant $f_s$ at heavy loads
  - Reduced $f_s$ at light loads

- High efficiency over wide load range

- Complicated controller design


How to improve efficiency? – Existing techniques

4 Predictive Gate Drive (PGD)™

- **Fixed:**
  - Preset the dead time and doesn’t change
  - Body diode conduction loss and reverse recovery loss

- **Adaptive:**
  - Detect the body diode conduction and control the dead time in the current cycle accordingly
  - Internal logic delay
  - Body diode conduction is minimized but still existent

- **Predictive:**
  - Sense the body diode conduction in the current cycle and progressively reduce the dead time in the next cycle until no body diode conduction is detected
  - Virtually eliminate the NMOS body diode conduction and reverse recovery losses
  - Also help reduce the PMOS V-I overlap loss
  - Extremely precise gate timing is crucial!

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5 Zero-Voltage Switching (ZVS): switch transistors when $V_{ds} = 0$

- **Operation:**
  - Snubber capacitor $C_s$ added at $V_{ph}$ to slow down the voltage transition
  - Inductor $L$ acts as a current source during dead time to charge/discharge $V_{ph}$
  - Both PMOS and NMOS are turned on when their $V_{ds} = 0$ → zero-voltage switching

- **Pros:**
  - Virtually eliminate V-I overlap loss and body diode losses
  - Good for high $f_S$ → Small size and weight

- **Cons:**
  - Additional off-chip component
  - Charge/discharge $C_s$ → more switching loss
  - Operate in Syn. DCM → more conduction loss
  - Only suitable for light loads

- **Challenges:**
  - Adaptive dead time control
  - Fast gate drive

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Comparative Evaluation of Power Saving Techniques

<table>
<thead>
<tr>
<th>Power Losses (mW)</th>
<th>Operation Condition ($V_{in}=3.3V$)</th>
<th>Power Saving Techniques</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$I_{load} = 1$ A (CCM) $f_s = 1$ MHz</td>
<td>Gate Dr.</td>
</tr>
<tr>
<td></td>
<td>$I_{load} = 500$ mA (DCM) $f_s = 500$ kHz</td>
<td></td>
</tr>
<tr>
<td>$R_{PMOS}$</td>
<td>80 (35%) 28 (12%)</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>79 (45%) 29 (17%)</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>24 (21%) 5 (4%)</td>
<td>✓</td>
</tr>
<tr>
<td>$R_{NMOS}$</td>
<td>30 (40%) 7 (9%)</td>
<td>✓</td>
</tr>
<tr>
<td>$V_{Diode}$</td>
<td>22 (10%) 9 (5%)</td>
<td>Good</td>
</tr>
<tr>
<td>$R_{L_ESR}$</td>
<td>12 (5%) 12 (7%)</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>14 (13%) 4 (4%)</td>
<td>✓</td>
</tr>
<tr>
<td>$R_{C_ESR}$</td>
<td>7 (3%) 8 (5%)</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>5 (4%) 4 (4%)</td>
<td>✓</td>
</tr>
<tr>
<td>$R_{Gate}$</td>
<td>3 (1%) 2 (1%)</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>3 (3%) 1 (1%)</td>
<td>✓</td>
</tr>
<tr>
<td>$V-I _Ov.$</td>
<td>73 (32%) 33 (19%)</td>
<td>Better</td>
</tr>
<tr>
<td></td>
<td>52 (47%) 19 (26%)</td>
<td>✓</td>
</tr>
<tr>
<td>Gate Dr.</td>
<td>5 (2%) 2 (1%)</td>
<td>✓</td>
</tr>
<tr>
<td>Tot. Cond.</td>
<td>152 (66%) 139 (80%)</td>
<td>Best</td>
</tr>
<tr>
<td></td>
<td>155 (73%) 55 (49%)</td>
<td>✓</td>
</tr>
<tr>
<td>Tot. Sw.</td>
<td>78 (34%) 35 (20%)</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>57 (51%) 20 (27%)</td>
<td>✓</td>
</tr>
<tr>
<td>Total Loss</td>
<td>230 174 112 75</td>
<td></td>
</tr>
<tr>
<td>$\eta$</td>
<td>86.4% 90% 89.4% 92.6%</td>
<td></td>
</tr>
</tbody>
</table>

Summary

- **Rank of Losses:**
  - #1 Loss: **PMOS Conduction Loss** ➞ Reduce $R_{PMOS}$
  - #2 Loss: **V-I Overlap Loss** ➞ Zero-Voltage Switching
  - #3 Loss: **NMOS Conduction Loss** ➞ Reduce $R_{NMOS}$
  - #4 Loss: **Body Diode Losses** ➞ Novel gate drive / dead time control
  - #5 Loss: **ESR Conduction Losses** ➞ Reduce $R_{ESR}$
  - #6 Loss: **Gate Drive Loss** ➞ Reduce parasitic C and/or $f_s$

- To improve **overall efficiency** ➞ Improve **light load efficiency!**

- At heavy loads: **Conduction Losses** $\propto f$ (current, ...) dominate
- At light loads: **Switching Losses** $\propto f$ (frequency, ...) dominate

- **Hybrid Control** : best for reducing conduction losses
- **ZVS** : best for reducing switching losses ➞ **Combine?**