Integrated Low Voltage, Power Efficient DC-DC Converters for Dynamic Power Supplies of Power Amplifiers

Biranchinath Sahu
Advisor: Dr. G.A. Rincon-Mora

Georgia Tech Analog Consortium
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, USA
March 22, 2002

Abstract

- **Power Amplifiers**
  - Consume majority of power in radio transceivers
  - Maximum efficiency when output signal is rail-to-rail
  - Dynamic power supply for the PA depending on signal strength
  - High efficiency voltage regulators

- **DC-DC Converters**
  - High efficiency compared to linear regulators
  - Dynamic control loop for selection of supply voltage
  - Efficient and stable control of high speed converters

- **Implementation**
  - SiGe BiCMOS process technology
  - Prototype: Converter and PA separately
  - Goal: High efficiency linear integrated PA
Objective

- Power Amplifiers are “long pole” in the tent
  - Cost, reliability and battery life

![Diagram of power amplifier stages]

- Variable supply voltage to the PA on demand
  ⇒ Optimum efficiency, improves battery life

Why Switching Regulators?

- Linear regulators
  - Simple, low cost
  - Poor efficiency

- Switching regulators
  - Complex, costlier
  - High efficiency (80-95%)
  - Noisy
PA as a Load for Converter

$$V_{DD} = 0.4 - 2.5 \, \text{V}$$

$$I_{load} = 0 - 1 \, \text{A}$$

$$L (nH)$$

$$R_c + V_{CEO}/I_CQ$$

CDMA-IS 95 requirements

Functional Block Diagram

Battery supply

Protection circuitry

Band gap reference

Dynamic reference for converter

DC-DC converter

Power amplifier

Soft start circuit

RF input

RF Output
Supply Selection Schemes

DC-DC controllers

<table>
<thead>
<tr>
<th>Control mode</th>
<th>Voltage</th>
<th>Peak-I</th>
<th>Average-I</th>
<th>Hysteretic</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{out-ripple}$</td>
<td>Worst</td>
<td>Worst</td>
<td>Worst</td>
<td>Best</td>
</tr>
<tr>
<td>D-limit</td>
<td>Poor</td>
<td>Poor</td>
<td>Poor</td>
<td>Best</td>
</tr>
<tr>
<td>Frequency</td>
<td>Best</td>
<td>Best</td>
<td>Best</td>
<td>Poor</td>
</tr>
<tr>
<td>Complexity</td>
<td>Good</td>
<td>Poor</td>
<td>Poor</td>
<td>Best</td>
</tr>
<tr>
<td>Compensation</td>
<td>Worst</td>
<td>Good</td>
<td>Poor</td>
<td>Best</td>
</tr>
<tr>
<td>$V_{in- \text{t response}}$</td>
<td>Worst</td>
<td>Worst</td>
<td>Good</td>
<td>Best</td>
</tr>
<tr>
<td>$I_{load- \text{t response}}$</td>
<td>Worst</td>
<td>Worst</td>
<td>Worst</td>
<td>Best</td>
</tr>
</tbody>
</table>

Design Considerations

- High efficiency over wide loading conditions
  - Conduction loss at heavy load
  - Switching loss at low load
- Dynamic voltage adjustment
  - 0.4 V to 2.5 V on demand
- Fast response, output slew rate
  - $V_{ref}$ variation at 1.22 MHz
  - Power adjustment of 1 dB in 666 μsec as directed by the base station
- Stability over duty cycle range
  - Duty cycle variation: 16% to 100%
- Switching frequency
  - Smaller external components at higher frequency
  - Higher switching loss
- Noise
  - Switching noise
  - Substrate coupling
- Layout

Work Plan

<table>
<thead>
<tr>
<th>Activity</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specifications</td>
<td>In progress</td>
</tr>
<tr>
<td>Design of prototype converter</td>
<td></td>
</tr>
<tr>
<td>Evaluation of prototype</td>
<td></td>
</tr>
<tr>
<td>Design of Integrated PA</td>
<td></td>
</tr>
<tr>
<td>Evaluation of integrated PA</td>
<td></td>
</tr>
</tbody>
</table>