Error Sources in First Order Bandgap References

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Abstract

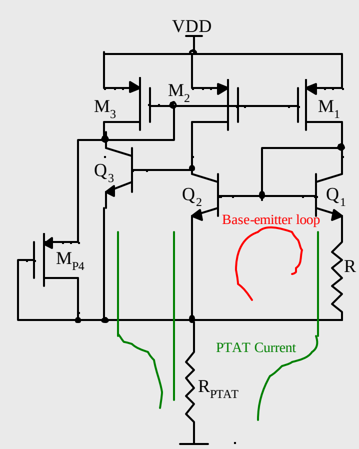
The error-sources that arise in first-order bandgap references have been studied. Analytical expressions for the effect of these error-sources on the reference voltage have been derived. These expressions have been verified through SPICE simulations of a basic first-order bandgap reference.

Why study error sources?

- As voltage headroom in current technologies shrinks, the study of the accuracy of the bandgap reference becomes critical
- The study of the effect of the error sources on the reference voltage may lead us to reduce them through circuit design techniques

Typical First-order Bandgap Reference

- **M_{P1}, M_{P2}, M_{P3} : Current Mirror** (Mirror PTAT current)
- **Q_1, Q_2 : Critical Transistors** (Difference in base-emitter voltages produces PTAT current through R)
- **M_{P4} : Start-up** (Draws current for M3 to start-up circuit)
- **Q_3 : Reduces Early voltage effects** (maintains the collector-emitter voltages at diode drop)

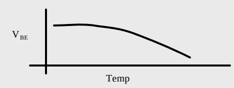


$$V_{ref} = V_{BE1} + 3 I_{PTAT} R_{PTAT}$$

Tools : The basic equations ...

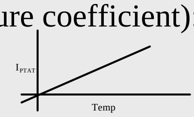
The base-emitter drop (negative temperature coefficient):

$$V_{BE} = V_T \ln\left(\frac{I_C}{J_S \cdot Area}\right)$$



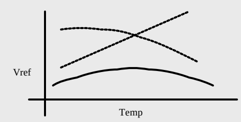
The PTAT current (positive temperature coefficient):

$$I_{PTAT} = \frac{V_{BE2} - V_{BE1}}{R} \qquad \therefore I_{PTAT} \equiv I_{C2} = \frac{V_T}{R}\ln\left(\frac{Cx}{x}\cdot\frac{I_{C1}}{I_{C2}}\right)$$



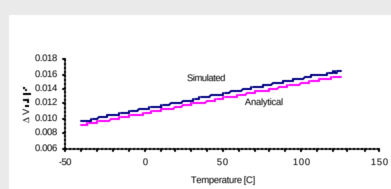
The reference voltage (linear temperature coefficient nullified) :

$$V_{ref} = V_{BE1} + 3 I_{PTAT} R_{PTAT} \qquad \Delta V_{ref} = \Delta V_{BE1} + 3\Delta I_{PTAT} R_{PTAT}$$



Error due to Resistor Mismatch

- Takes place due to mismatch in resistors R and R_{PTAT}
- Simulated by adding resistor in series with R_{PTAT}, δ_{RR}.R
- Simulated δ_{RR}= 2%

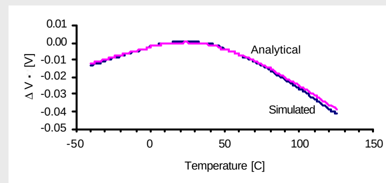


$$R_{ptat-x} = \frac{R_{ptat}}{R} R(1+\delta_{RR}) = R_{ptat}(1+\delta_{RR})$$

$$\Delta V_{ref} = 3 I_{PTAT} R_{PTAT} \delta_{RR}$$

Error due to Resistor Temperature Drift

- Temperature drift of resistors cancel out in PTAT component
- Affects V_{BE} component
- $R(T) = R(T_r)[1+A(T-T_r)+B(T-T_r)^2]$
- Simulated A=500/ºC, B=200/ºC²



$$V_{BE2-x} = V_{BE2} + V_T \ln\left(\frac{R(T_r)}{R(T)}\right)$$

$$\Rightarrow \Delta V_{BE2} = -V_T \ln(1+A(T-T_r)+B(T-T_r)^2)$$

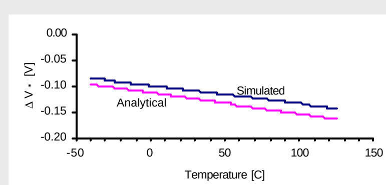
$$\Delta V_{ref} = -V_T \ln(1+A(T-T_r)+B(T-T_r)^2)$$

Error due to Resistor Tolerance

- Process variations lead to the deviation of the resistors from their nominal values
- Simulated by adding a resistor in series with R, $\delta_{RA}.R$
- Simulated δ_{RA} = 20%

$$\Delta V_{BE2} \approx -V_T \delta_{RA}$$

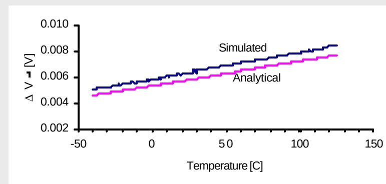
$$\Delta I_{PTAT} = -\frac{V_T \ln C}{R}\delta_{RA}$$



$$\Delta V_{ref} = -\left(V_T \delta_{RA} + 3\frac{V_T \ln C}{R} R_{PTAT}\delta_{RA}\right)$$

Error Due to Transistor Mismatch

- Takes place due to deviation in the required ratio of the areas of Q_1,Q_2
- Simulated by adding a deviation in the ratio of the transistors C, δ_{NPN}.C
- Simulated δ_{NPN}= 2%



$$I_{PTAT-x} = \frac{V_T}{R}\ln(C(1+\delta_{NPN})) = I_{PTAT} + \frac{V_T}{R}\ln(1+\delta_{NPN})$$

$$\Delta I_{PTAT} \approx \frac{V_T}{R}\delta_{NPN}$$

$$\Delta V_{BE2} = V_T \ln\left(\frac{\ln[C(1+\delta_{NPN})]}{\ln C}\right) \approx V_T \ln\left(1+\frac{\delta_{NPN}}{\ln C}\right)$$

$$\Delta V_{BE2} \approx \frac{V_T \delta_{NPN}}{\ln C}$$

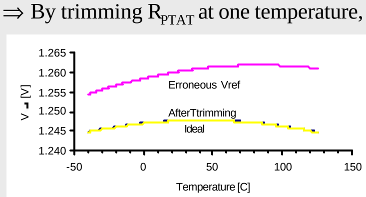
$$\Delta V_{ref} = \frac{V_T \delta_{NPN}}{\ln C} + 3\frac{V_T}{R}R_{PTAT}\delta_{NPN}$$

Epilogue : Tuning R_{PTAT}

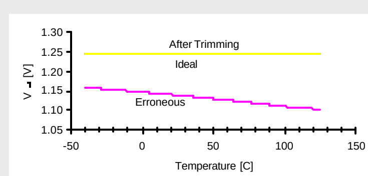
The error due to resistor mismatch, resistor tolerance, transistor tolerance have a linear dependence on temperature, thus the error can be corrected by trimming at room temperature

⇒ Nullifying the error at ONE temperature, corrects the curve for ALL temperatures !

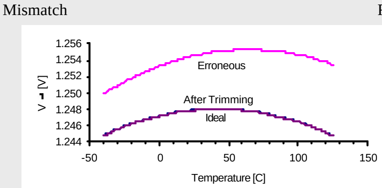
⇒ By trimming R_{PTAT} at one temperature, the erroneous curve falls back to the ideal curve !



Resistor Mismatch



Resistor Tolerance



Transistor Mismatch

Conclusions : Taking Stock ...

- Analytical expressions for the effect of the error sources on the reference voltage have been derived
- These have been verified through SPICE simulations
- **Future work** involves analyzing error due to Package Shift, Current Mirror Mismatch

ΔV_{ref} at 25 °C / Type of Error	Analytical [mv]	Simulated [mv]
Resistor Mismatch	11.7	12.3
Resistor Tolerance	-12.8	-10.7
Resistor TC	0.0	0.5
Transistor Mismatch	6.0	6.6