

Survivor

A Novel Strategy for Reducing the Effects of Device Mismatch

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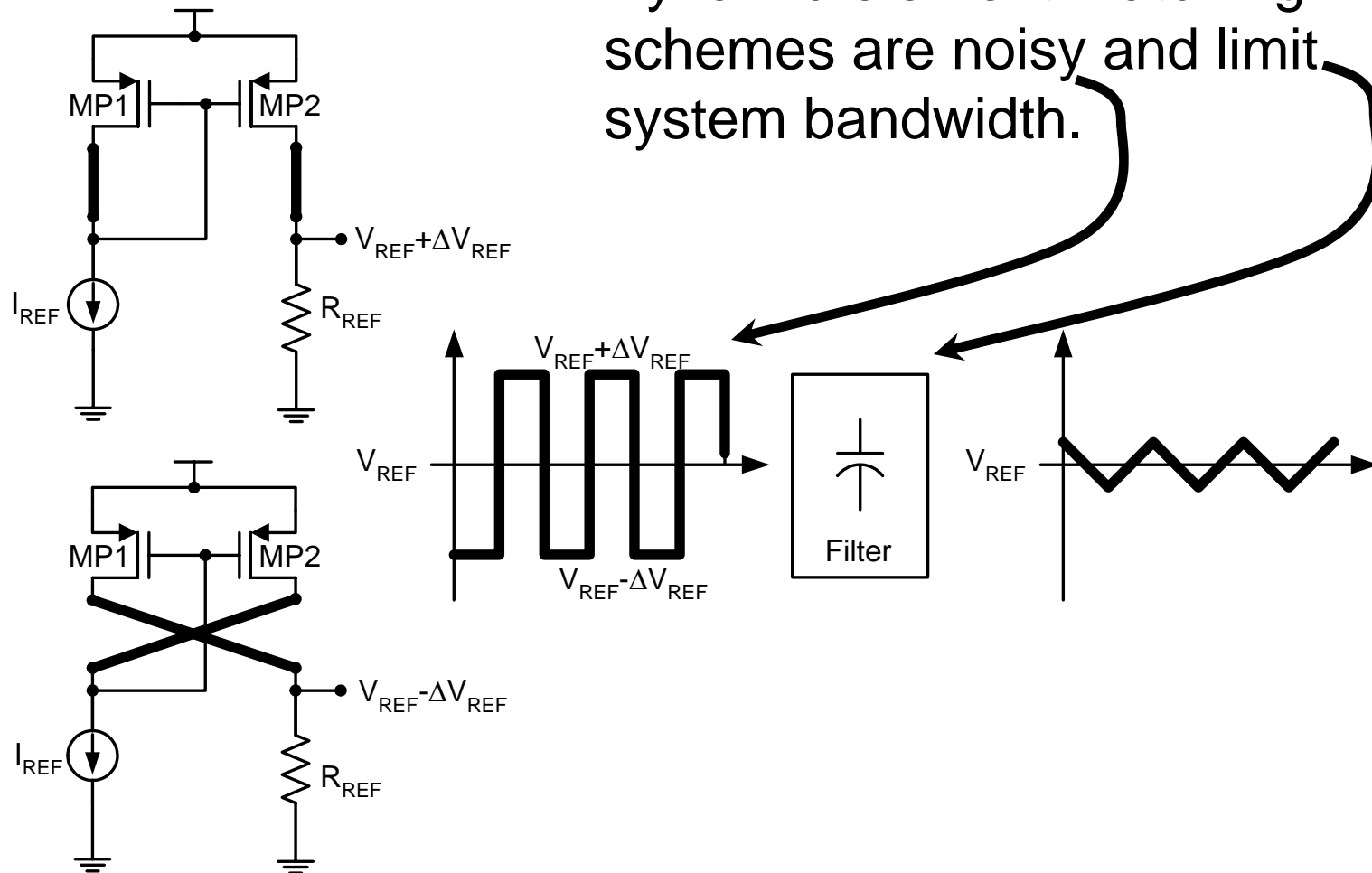
Outline

- Why are we exploring this strategy?
 - **Motivation**
- What is the technique about?
 - **System Concept**
- How is it implemented?
 - **Basic Strategy**
 - **Comparator Cell**
 - **System**
- Will it work?
 - **Input Parameters**
 - **Simulation Results**
 - **Discussion: Another Comparator Topology**
 - **Future Work**



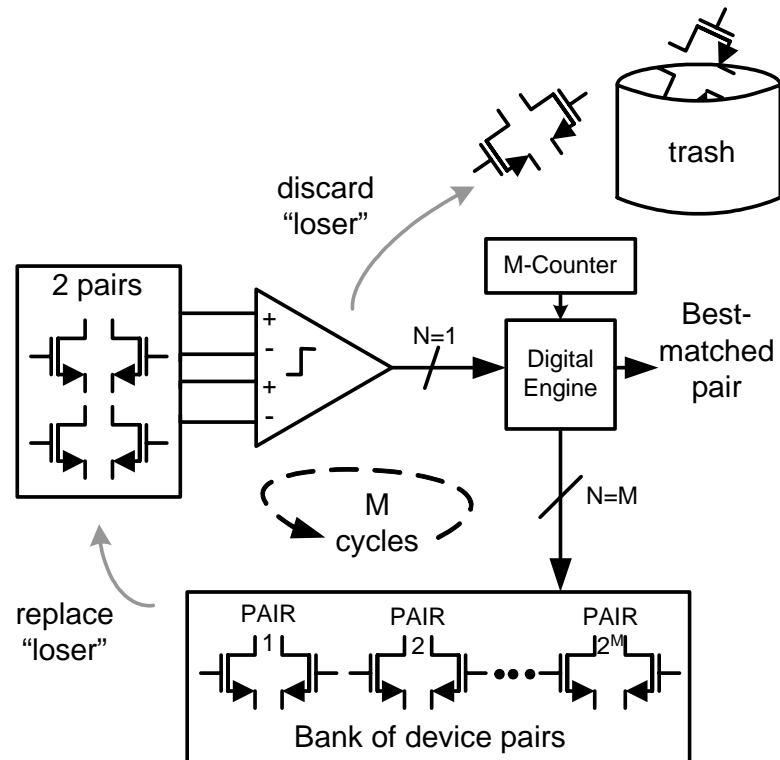
Motivation

Dynamic-element matching schemes are noisy and limit system bandwidth.

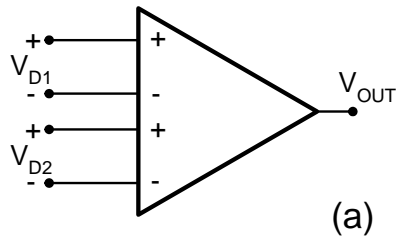


System Concept

- Bank of device pairs fabricated.
- Two pairs compared for mismatch in comparator cell.
- Digital engine discards loser pair and provides replacement.
- Survivor emerges after final comparison.



Basic strategy



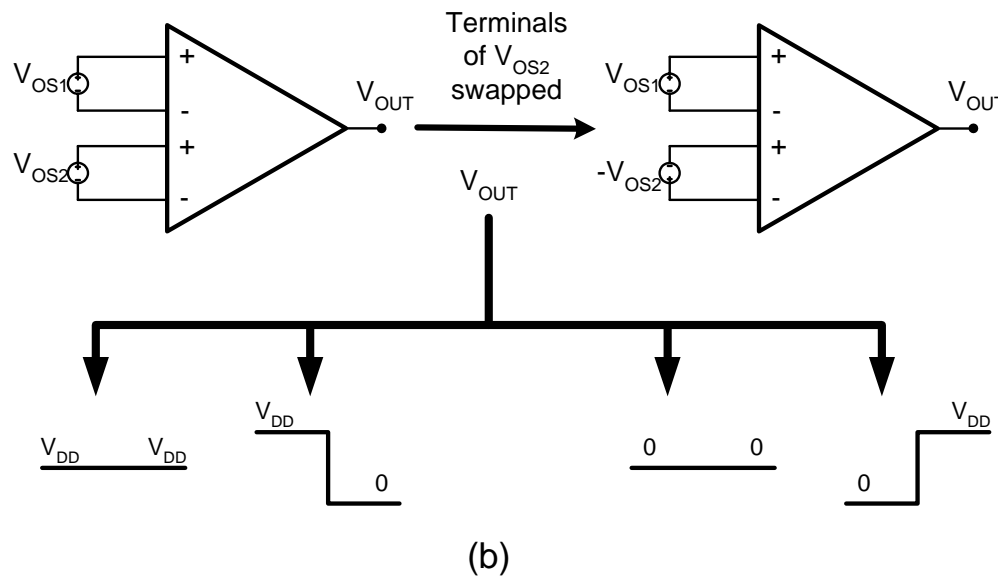
$$V_{OUT} = V_{DD} \quad (0 < V_{D1} + V_{D2})$$

$$V_{OUT} = 0 \quad (V_{D1} + V_{D2} < 0)$$

Change in V_{OUT}



$$|V_{OS1}| < |V_{OS2}|$$

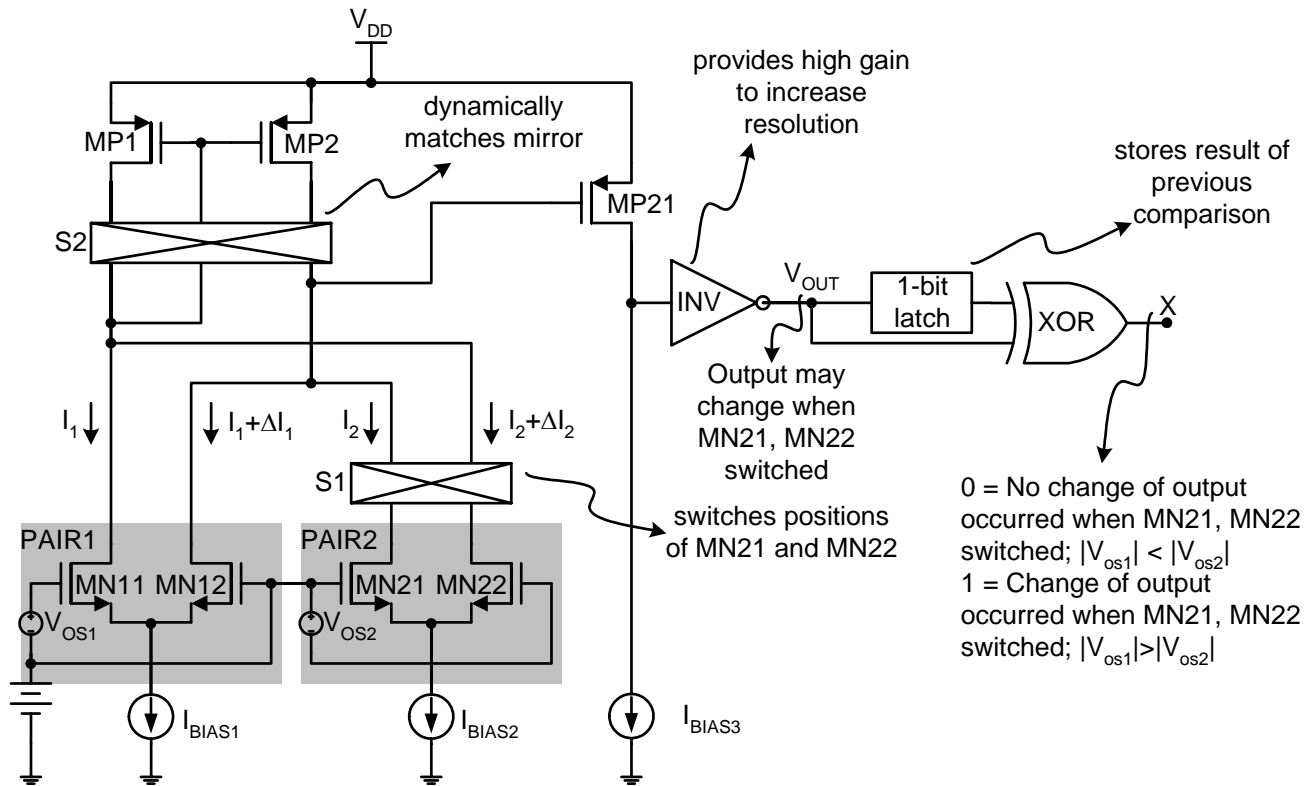


No Change in V_{OUT}



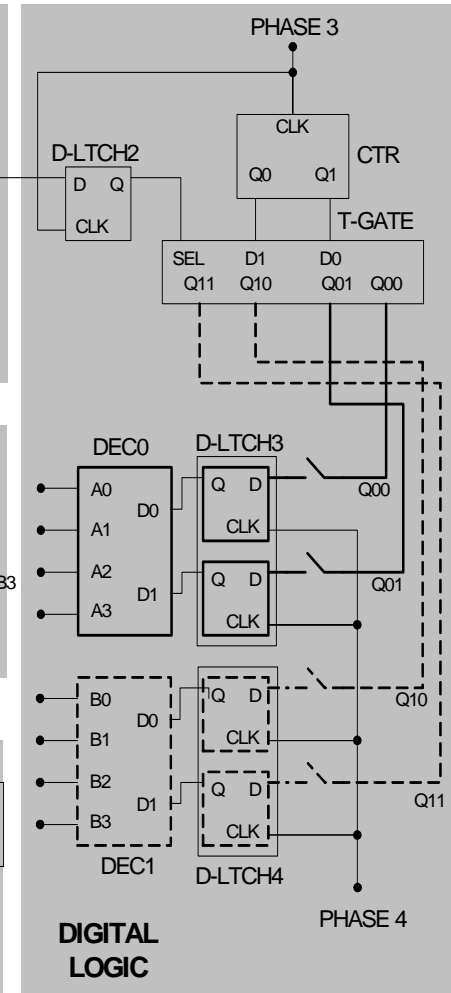
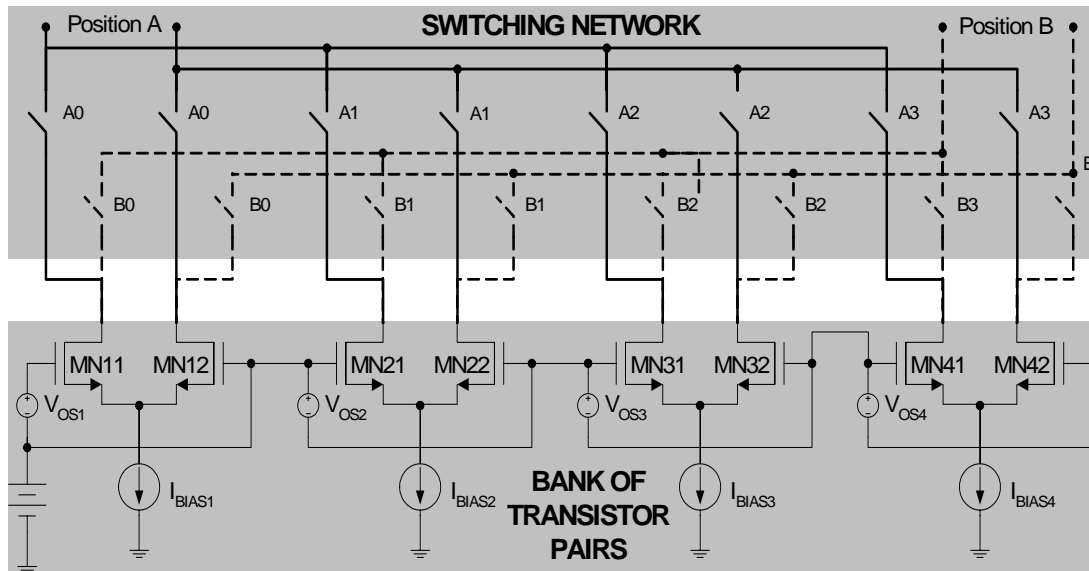
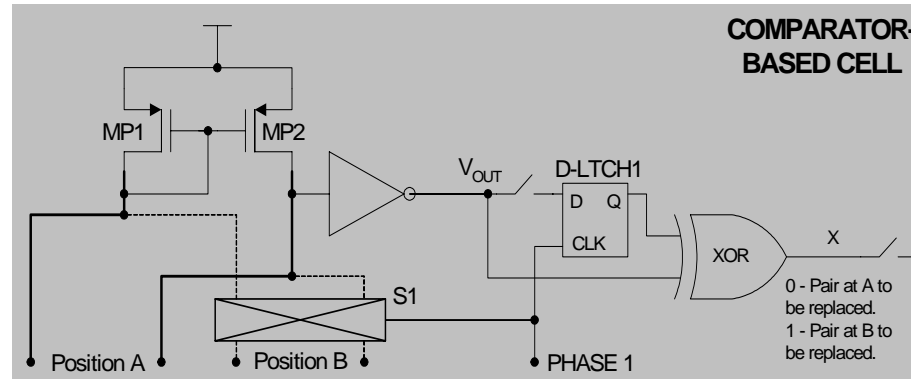
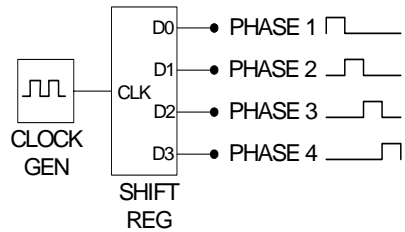
$$|V_{OS1}| > |V_{OS2}|$$

Comparator Cell



- S1 switches pair MN21-22 to change polarity of V_{OS2} .
- Latch stores result of previous comparison.
- XOR detects changes in V_{OUT} .
- Big question: What is the limit on the resolution?

Survivor System



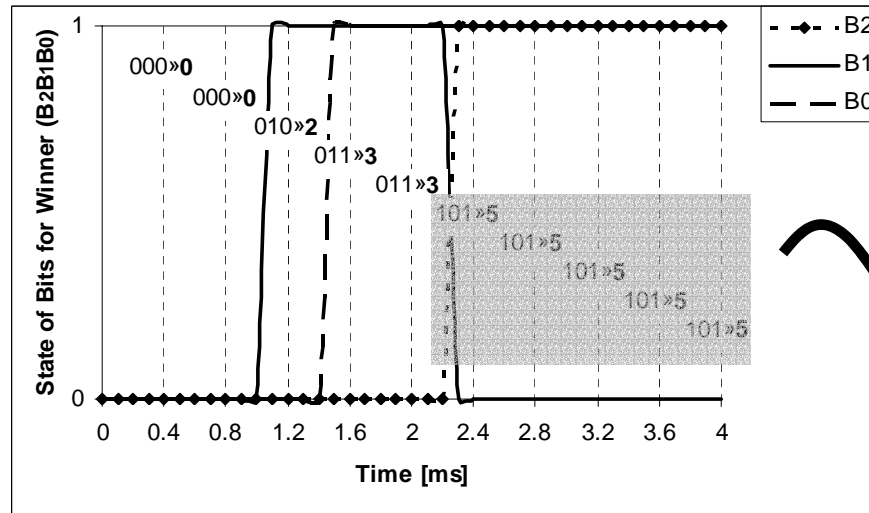
Input Parameters

PAIR	0	1	2	3	4	5	6	7
3-BIT DIGITAL CODE	000	001	010	011	100	101	110	111
OFFSET [mV]	2.0	3.0	1.6	-1.3	2.2	1.0	2.8	2.3

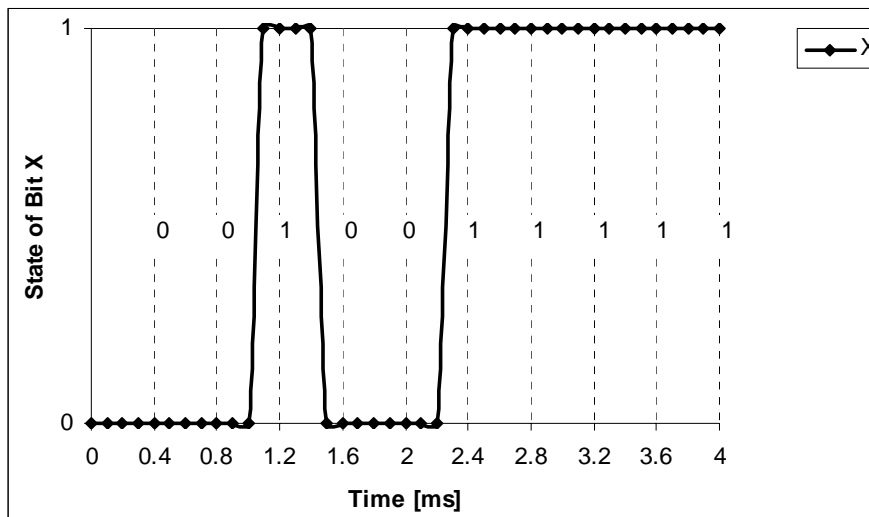
Survivor

CYCLE	PAIR AT POSITION A (OFFSET)	PAIR AT POSITION B (OFFSET)	WINNER	LOSER	INCOMING PAIR	X
1	0 (2.0mV)	0 (2.0 mV)	0	0	1	0
2	1 (3.0mV)	0 (2.0 mV)	0	1	2	0
3	2 (1.6 mV)	0 (2.0 mV)	2	0	3	1
4	2 (1.6 mV)	3 (-1.3 mV)	3	2	4	0
5	4 (2.2 mV)	3 (-1.3 mV)	3	4	5	0
6	5 (-1.0 mV)	3 (-1.3 mV)	5	3	6	1
7	5 (-1.0 mV)	6 (2.8 mV)	5	6	7	1
8	5 (-1.0 mV)	7 (2.3 mV)	5	7	-	1

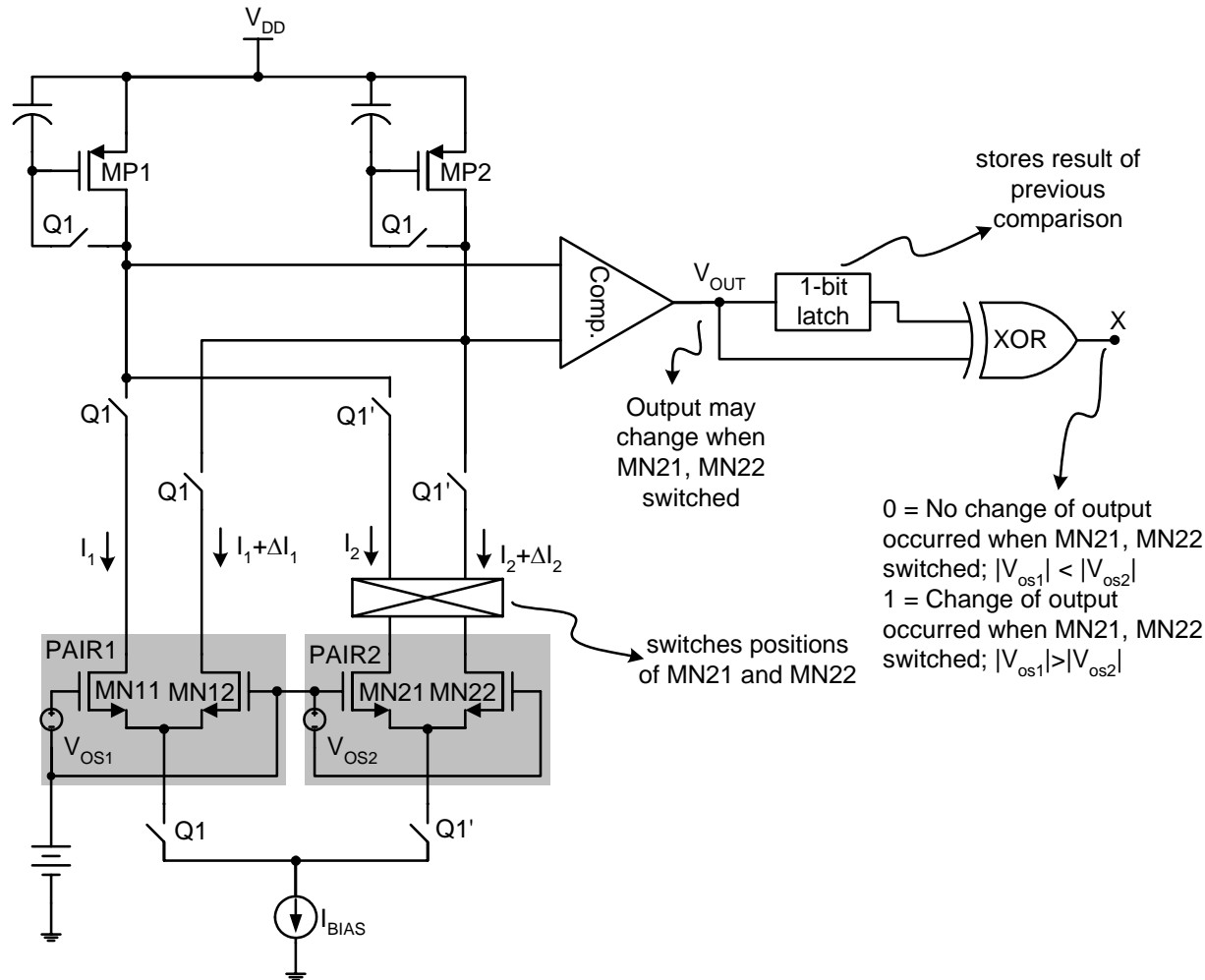
Simulation Results



System converges to pair 5 with lowest offset.



Discussion: Another Comparator Topology



- Topology immune to changes in power supply
- Comparator can have chopper input to reduce impact of offset on resolution.

Future Work

- **Find optimal number of devices required to meet an accuracy specification.**
- **Verify limits of resolution of system.**
- **Design digital system at transistor level.**
- **Fabricate system in IC and verify effectiveness.**

