Circuit Design for Accurate and Lossless Current-Sensing in DC-DC Converters

H. Pooya Forghani-zadeh
Advisor: Prof. Gabriel Rincón-Mora
Georgia Tech Analog and Power IC Lab
Georgia Institute of Technology
April 2005
Abstract

Current-sensing circuits are essential for protection and control of the switching regulators. Our proposed technique estimates the inductor current by filtering the voltage across it. Furthermore, the inductor value and its ESR are measured during the startup to boost the accuracy. This poster focuses on the circuit design of proposed system main part- the current-sensing filter. The design challenges are independently programmable gain and bandwidth, high linearity to prevent the systematic offset, and continuous low-offset operation (input-referred offset<0.5mV) without transient spikes.
System – Normal Operation

\[ V_{\text{sense}} = g_m R_2 \left( \frac{1}{1 + s R_2 C} \right) V_L \]
\[ I_L = \frac{1}{(R_{\text{ESR}} + s L)} V_L \]

If \( R_2 \) is tuned such that \( L/R_{\text{ESR}} = R_2 C \),
\[ V_{\text{sense}} = (g_m R_2)R_{\text{ESR}} \times I_L \]
If \( (g_m R_2)R_{\text{ESR}} = 1\Omega \) → \( V_{\text{sense}} = 1\Omega \times I_L \)

Problem: \( L \) and \( R_{\text{ESR}} \) are not known at the design time

Solution: Measure them at the startup

\[ I_{\text{load}} = \frac{g_m R_2}{R_{\text{ESR}}} \]

\[ V_{\text{in}} = V_L \]
\[ V_{\text{in+}} = V_{\text{in-}} \]

Designer → Inductor selection → PCB → Measurement and Adjustments → Accurate and Lossless Current-Sensing

End user → Startup → Normal Operation → Circuit In Use

GEDC Industry Advisory Board, April 2005.
© 2005 Georgia Electronic Design Center. All Rights Reserved.
Redistribution for profit prohibited.
System - Startup

1. Tuning:
   - Adjust the high frequency gain

   Loop Forces: \( K \frac{g_{m1}}{C} L I_p = V_{ref1} \)

   \[ \frac{g_{m1}}{C} L = \frac{V_{ref1}}{K I_p} \]

2. Calibration:
   - Adjust the low frequency gain

   Loop Forces: \( K (g_{m1} R_2) R_{ESR} I_{test} = V_{ref2} \)

   If \( \frac{V_{ref1}}{I_p} = \frac{V_{ref2}}{I_{test}} \)

   Matched BW \( L/R_{ESR} = R_2 C \)

   Current-sensing gain:
   \[ gain = \frac{V_{ref2}}{K I_{test}} = \frac{V_{ref1}}{K I_p} \]
Ping-Pong Operation - Offset Reduction

**Auto zeroing phase**
Offsets are stored at the hold capacitor

\[ V_s = \left( \frac{g_{m1} R_o V_{os1} + g_{ma} R_o V_{os2} + g_{ma} R_o V_{ref}}{1 + g_{ma} R_o} \right) + V_{error} \]

**Normal operation**
Output voltage is

\[ V_o = g_{m1} V_{in} (R_o \parallel R_2) \]
\[ + V_{os1} \frac{g_{m1} (R_o \parallel R_2)}{1 + g_{ma} R_o} + V_{os2} \frac{g_{ma} (R_o \parallel R_2)}{1 + g_{ma} R_o} \]
\[ - g_{ma} (R_o \parallel R_2) V_{error} + V_{ref} \left[ 1 - \left( \frac{1}{1 + g_{ma} R_o} \frac{R_2}{R_o + R_2} \right) \right] \]

\[ V_{os1}: \text{main input offset} \]
\[ V_{os2}: \text{auxiliary input offset} \]
\[ V_{error}: \text{charge injection voltage error} \]
\[ g_{ma}: \text{auxiliary path transconductance} \]
\[ R_o: g_{m1} \text{ output resistance} \]
\[ V_s: \text{hold capacitor stored voltage} \]
\[ g_m: \text{main path transconductance} \]
**G_m_1 Implementation (1)**

\[ I_o = g_{m1} (V_+ - V_-) + g_{ma} (V_{a+} - V_{a-}) \]

\[ g_{m1} = f(d) = g_{m10} + \frac{g_{m11} d}{128} \]

+ and – : Main inputs

a+ and a-: Auxiliary path inputs

K is the current mirror gain

\[ I_o = \frac{K}{R_1} (V_+ - V_-) + g_{ma} (V_{a+} - V_{a-}) \]
Gm1 Implementation(2)

Current Mirror

- Current mirror gain is adjusted digitally
- The switches are not in the signal path and do not effect the AC response

Current Source

- Current source I4 is adjusted digitally
- Transistors Na-Nd form a current canceling differential pair with lower transconductance compared to simple differential pair
- Auxiliary offset path is formed in current sources
Digitally tunable resistor:

A large output capacitor (C) relative to the switch parasitic capacitance ensures that switch parasitic capacitance does not alter the ideal first order AC response.

\[
Z_{in} = \frac{R_1 + R_2}{1 + (R_1 + R_2)C_s} \left( \frac{1 + s(R_1 || R_2)C_p}{1 + s(R_1 || R_2)C_p} \right) \left( C + \frac{C_p}{R_1 + R_2} \right)
\]

Since \( C >> C_p \)

\[
Z_{in} = \frac{R_1 + R_2}{1 + (R_1 + R_2)C_s}
\]
Simulation Results

Important design values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>L spread</td>
<td>2-6µH</td>
</tr>
<tr>
<td>ESR spread</td>
<td>12-188mΩ</td>
</tr>
<tr>
<td>R1 in ( g_{m1} )</td>
<td>250KΩ</td>
</tr>
<tr>
<td>( g_{m1} ) mirror ratio</td>
<td>1-5</td>
</tr>
<tr>
<td>Mirror No. bits</td>
<td>7</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>325-2900KΩ</td>
</tr>
<tr>
<td>( R_2 ) No. bits</td>
<td>8</td>
</tr>
<tr>
<td>( C )</td>
<td>60pF</td>
</tr>
<tr>
<td>( C_{h1}, C_{h2} )</td>
<td>6pF</td>
</tr>
<tr>
<td>( R_1 ) in ( g_{m1} )</td>
<td>8</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>12-188mΩ</td>
</tr>
<tr>
<td>( R_2 ) No. bits</td>
<td>12-188mΩ</td>
</tr>
<tr>
<td>( C )</td>
<td>325-2900KΩ</td>
</tr>
<tr>
<td>( C_{h1}, C_{h2} )</td>
<td>250KΩ</td>
</tr>
<tr>
<td>( C )</td>
<td>2-6µH</td>
</tr>
<tr>
<td>( R_1 ) in ( g_{m1} )</td>
<td>2-6µH</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>2-6µH</td>
</tr>
<tr>
<td>( L ) spread</td>
<td>2.5-40, 0.075 steps</td>
</tr>
<tr>
<td>( ESR ) spread</td>
<td>0.5µm CMOS</td>
</tr>
<tr>
<td>Technology</td>
<td>0.5µm CMOS</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.7-4.2V (Li-Ion)</td>
</tr>
<tr>
<td>Temperature range</td>
<td>-40° C to 125° C</td>
</tr>
<tr>
<td>Switching input (( V_{in+} )) CMR</td>
<td>0-V_{DD} (rail to rail)</td>
</tr>
<tr>
<td>Non-switching input CMR</td>
<td>0.8V-V_{DD}-1V (Nom: 1.5V)</td>
</tr>
<tr>
<td>Output-referred offset</td>
<td>&lt;5mV</td>
</tr>
<tr>
<td>Nonlinearity (( \Delta g_{m1}/g_{m1} ))</td>
<td>&lt;=-67dB (for rail to rail ICMR)</td>
</tr>
<tr>
<td>BW programmability</td>
<td>1-5KHz, 30Hz steps</td>
</tr>
<tr>
<td>Gain programmability (( V_o/V_{in} ))</td>
<td>2.5-40, 0.075 steps</td>
</tr>
</tbody>
</table>

Summary of circuit performance and specifications

- Technology: 0.5µm CMOS
- Supply Voltage: 2.7-4.2V (Li-Ion)
- Temperature range: -40° C to 125° C
- Switching input (\( V_{in+} \)) CMR: 0-V_{DD} (rail to rail)
- Non-switching input CMR: 0.8V-V_{DD}-1V (Nom: 1.5V)
- Output-referred offset: <5mV
- Nonlinearity (\( \Delta g_{m1}/g_{m1} \)): <=-67dB (for rail to rail ICMR)
- BW programmability: 1-5KHz, 30Hz steps
- Gain programmability (\( V_o/V_{in} \)): 2.5-40, 0.075 steps
Future Work

- Testing $g_m$-C filter fabricated circuit
- Automatic programming circuit
  - Gain Calibration
  - Bandwidth Tuning
- Design of a current-mode buck DC-DC controller
- Applying the current-sensing filter to the switching regulator (i.e., startup control logic)