Integrated, Low Voltage, Dynamically Adaptive Buck-Boost Converter – A Top-Down Design Approach

Georgia Tech Analog Consortium

Biranchinath Sahu

Advisor: Prof. Gabriel A. Rincón-Mora

Analog Integrated Circuits Laboratory
School of Electrical and Computer Engineering
Georgia Institute of Technology

Abstract

- Power-aware, portable, electronic systems incorporate algorithms for dynamically changing the supply voltage depending on work-load/throughput to extend battery life.

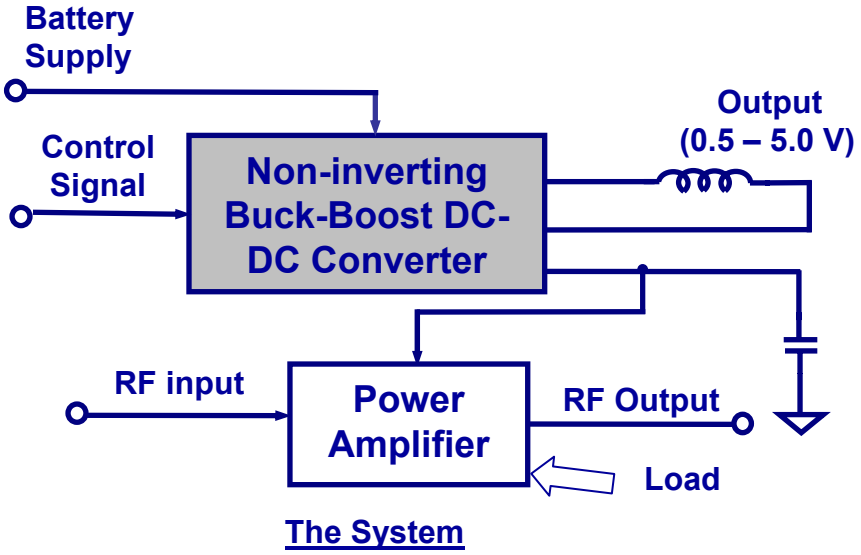
- Single inductor, non-inverting buck-boost converters are *best-suited* to generate a voltage that is higher and lower than the battery supply, with minimum number of external components.

  ⇒ **Dynamically-Adaptive Buck-Boost Converters**

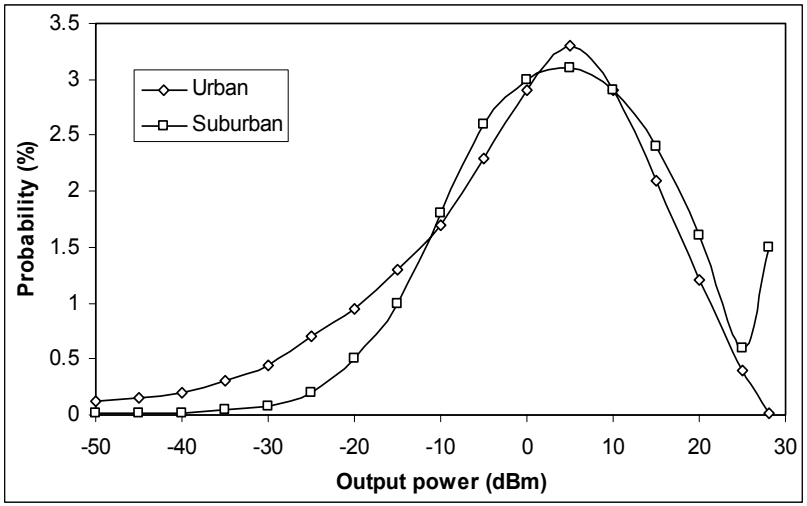
  - ✓ High efficiency ⇒ Improvement in battery life
  - ✓ Low voltage ⇒ Single cell operation (Li-ion/NiCd/NiMH/Fuel Cell)
  - ✓ Integrated ⇒ ↓ External components, ↓ Cost
  - ✓ Low noise ⇒ ↓ Interference

- This work addresses the design challenges and trade-offs involved in realizing an integrated circuit (IC) for such a system with a *wide range of supply voltage*.
  - Lower limit – Minimum supply voltage for circuits to be operational (1.4 V)
  - Higher limit – Process technology constraints (5 V)

Understanding the Load



The System



Loading Profile

- The output power of the power amplifier varies over a wide range

  ⇒ ***Output voltage range of the buck-boost converter***

- For WCDMA architecture, the power transmitted can increase or decrease by 1-dB is every 666 μsec

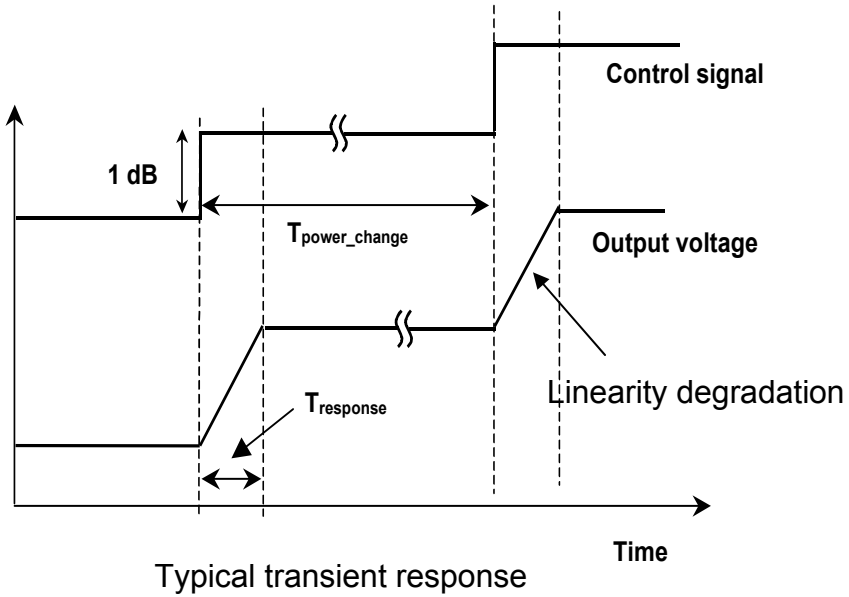
  ⇒ ***Transient requirements***

- The RF power amplifier must meet its adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM) specifications

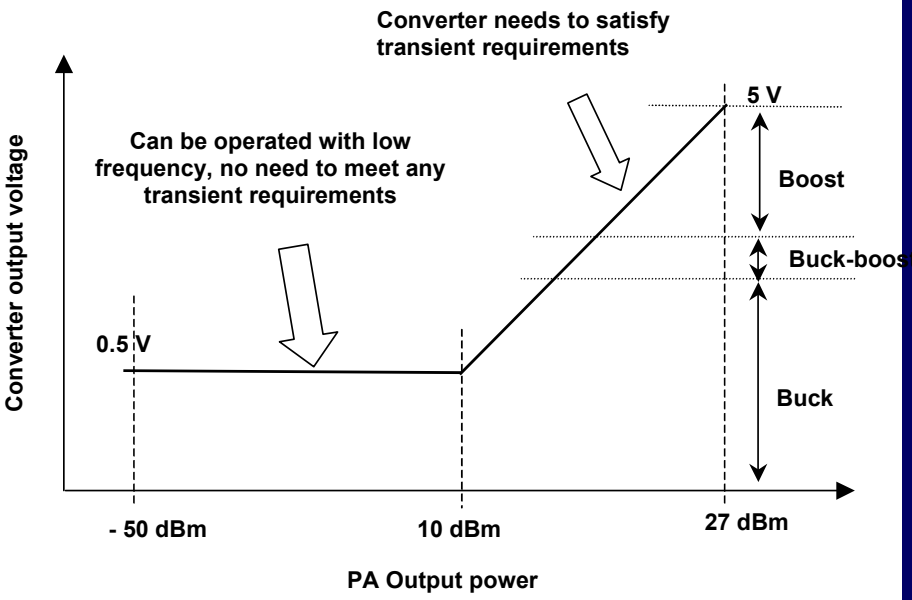
  ⇒ ***Output voltage accuracy (DC, AC, Transient) requirements***

Requirements of the Converter

- Under light-load conditions, the converter can operated in buck-mode with a lower switching frequency, thereby reducing switching losses and consequently improving system efficiency.

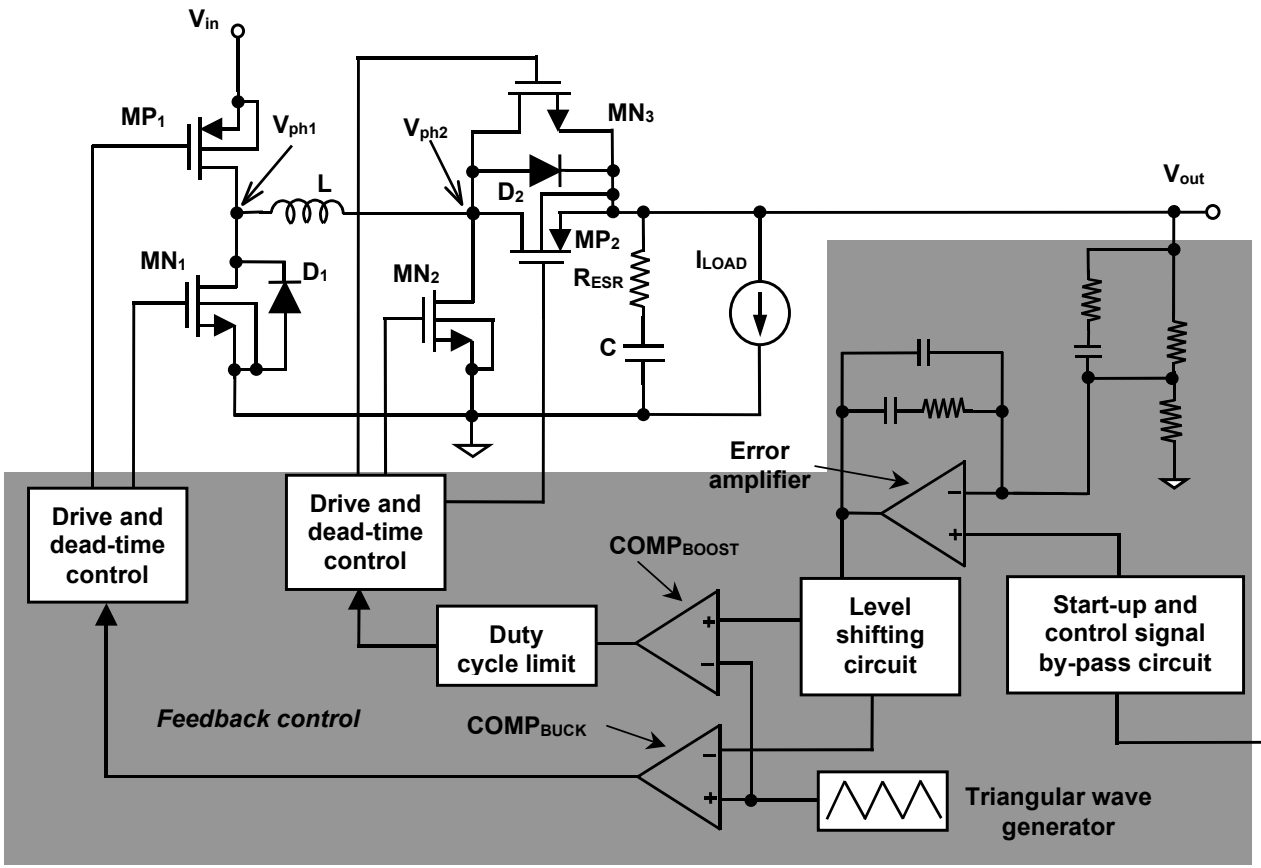


Typical transient response



Specifications	Value
Input voltage (V_{IN})	1.4 - 4.2 V
Output voltage (V_{OUT})	0.4 - 4.0 V
Load current [$I_{LOAD} = f(V_{OUT})$]	0.03 - 0.5A
Output voltage accuracy [$f(V_{OUT})$]	95 %
Load resistance	10-15 Ohms
Switching frequency	1 MHz ± 20%
Closed-loop bandwidth	≥ 50 kHz
1-dB step change response time	≤ 20 μsec
Full-load efficiency	≥ 90 %

Converter Block Diagram



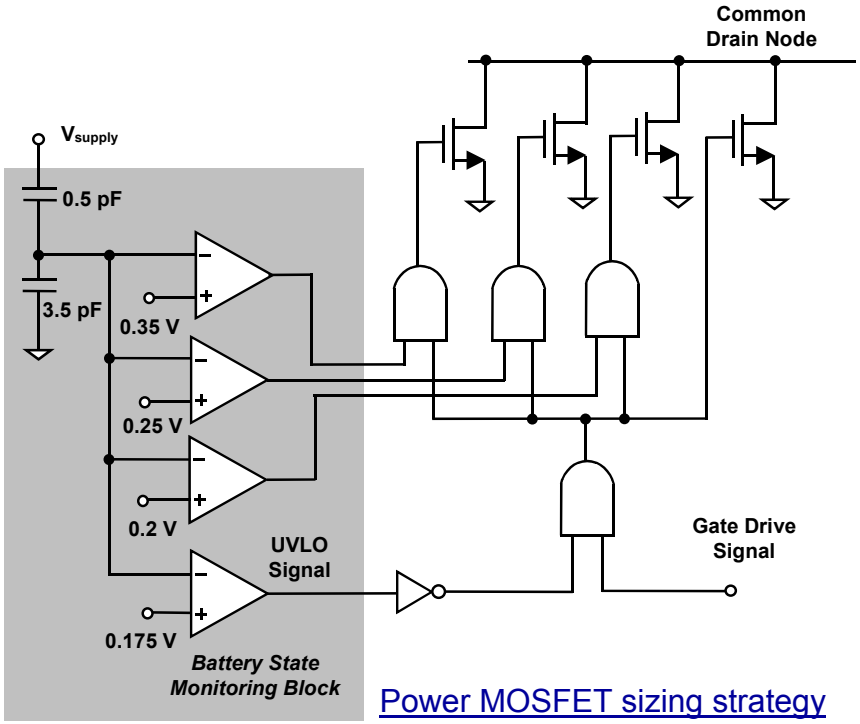
Salient Features

→ Voltage mode control
→ Type–III compensation
→ 1 MHz switching frequency
→ 0.8 μH power inductor
→ 10 μF output capacitor with 10 mΩ ESR

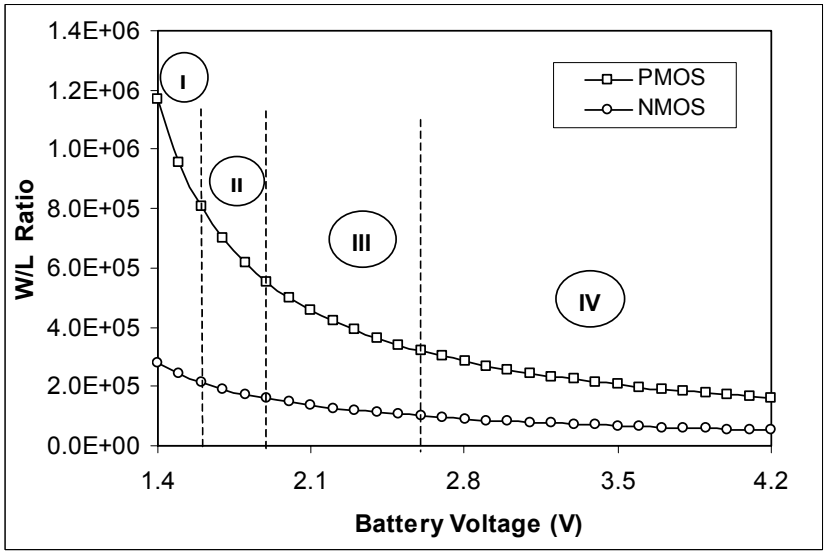
- Buck/Buck-Boost/Boost Mode[1] of operation for improved efficiency
- Low power, sleep mode of operation for optimal efficiency

[1] *FA7618 controller as presented in US Patent No. 5,402,060 (1995) and LTC 3440 application notes (2003).*

Dynamic Sizing of Power MOSFETS



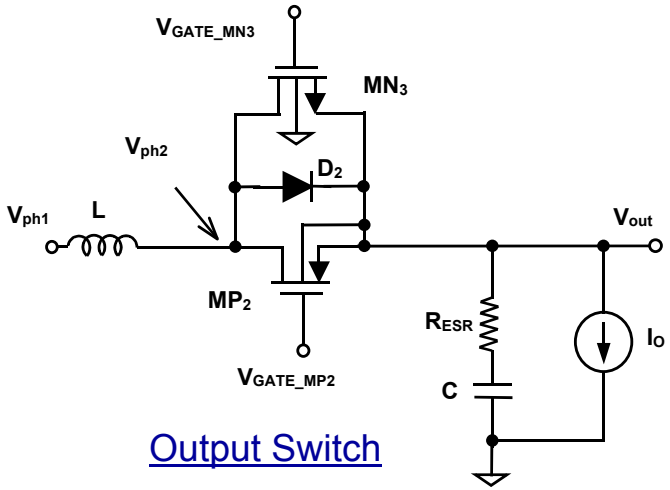
Power MOSFET sizing strategy



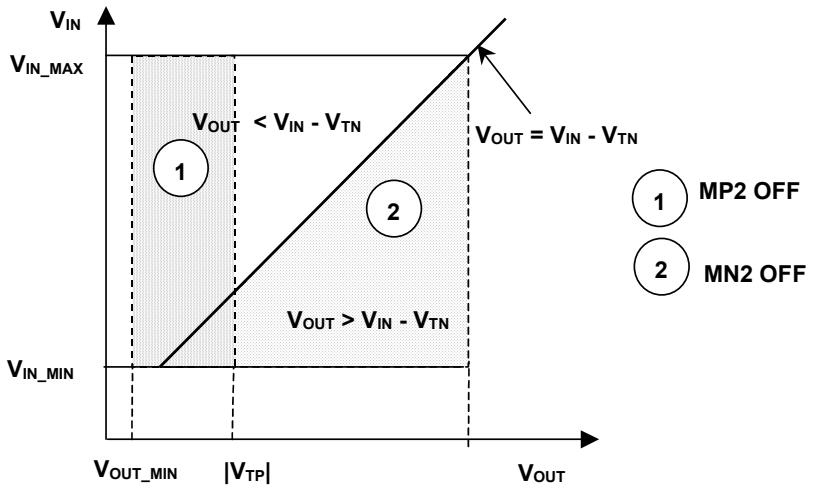
Aspect ratio for same switch ON-resistance with variation in supply voltage

- Dynamic sizing of Power MOSFETs allow minimization of conduction and switching losses for optimal efficiency at a given supply voltage.
  - Conduction loss $\propto$ Switch resistance $\propto 1/W$
  - Switching loss $\propto$ Switch capacitance $\propto W$

Gate Drive Circuits

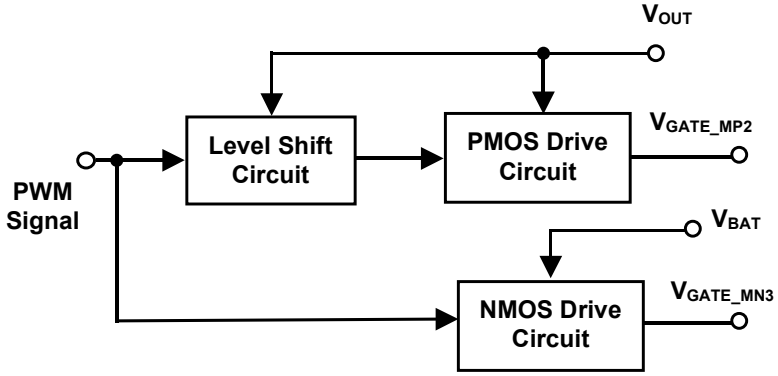


Output Switch



Transmission gate operation

- Except the Boost PMOS switch, all the other switches can be driven by a chain of inverters.
- For the output switch, transmission gate is used to reduce the voltage range for which body diode conducts.
- The PMOS gate driver is powered from the output of the converter to ensure its operation.



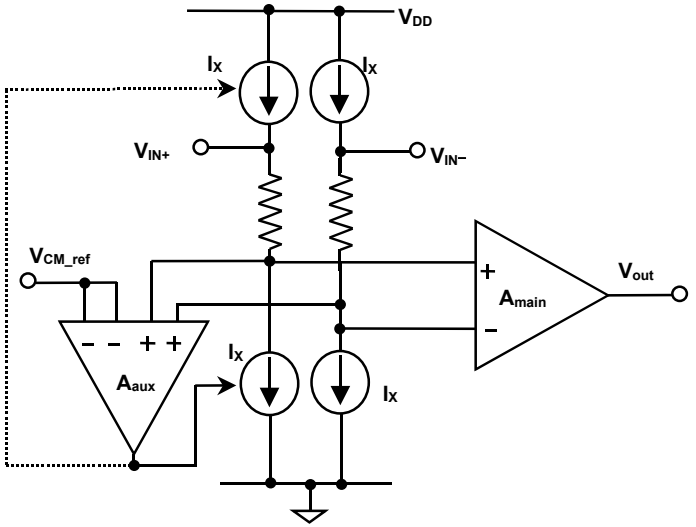
Level shifting circuit for PMOS Boost Drive

Designing the Error Amplifier

Requirements of the Op-amp

- **Input common-mode range (ICMR)**
  - With $|V_{TP}|+V_{TN} > V_{DD}$, the ICMR of NMOS and PMOS exist only close to supply and ground rail, respectively.
  - By dynamically shifting the input signal as a function of supply voltage the input signal a PMOS input stage can be used.

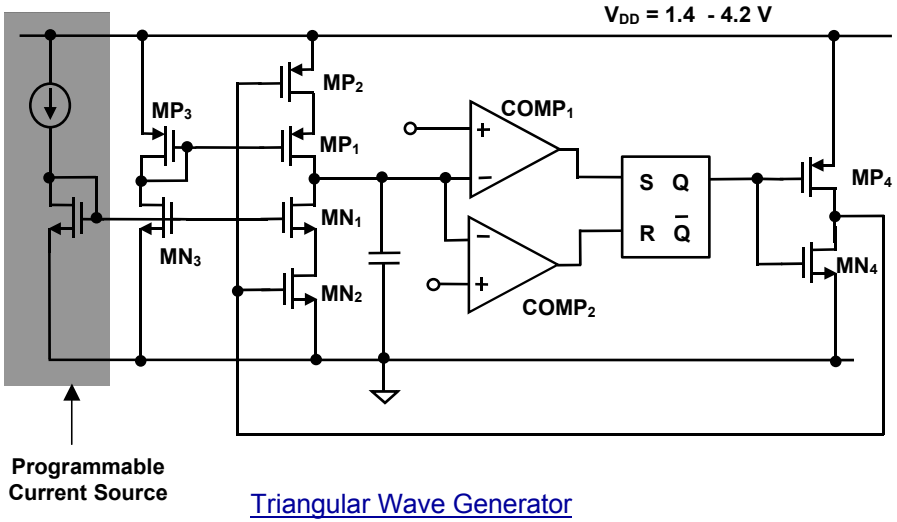
  $\Rightarrow$ ICMR ↑, Noise ↑, Offset voltage ↑
- **Input Offset Voltage**
  - Error in output voltage = Offset voltage × Closed loop gain of the converter.
  - Depending on the accuracy requirement, offset cancellation techniques can be used.
- **DC Gain and Bandwidth**
  - As DC gain ↑, steady-state error↓
  - UGF_{OPAMP} >> Loop $BW_{CONVERTER}$



Low voltage, large ICMR op-amp

Minimum supply voltage = V_T + 3 V_{ON} sets lower limit of operation for the integrated converter

Reducing Noise – Spread Spectrum Switching

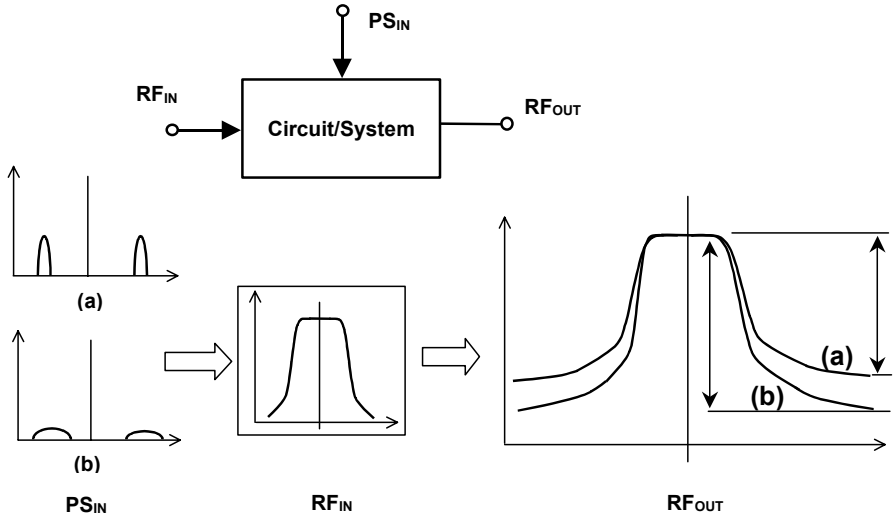


Triangular Wave Generator

- The frequency of the triangular waveform generator is changed in a pseudo-random manner by varying the charging and discharging current of the capacitor.

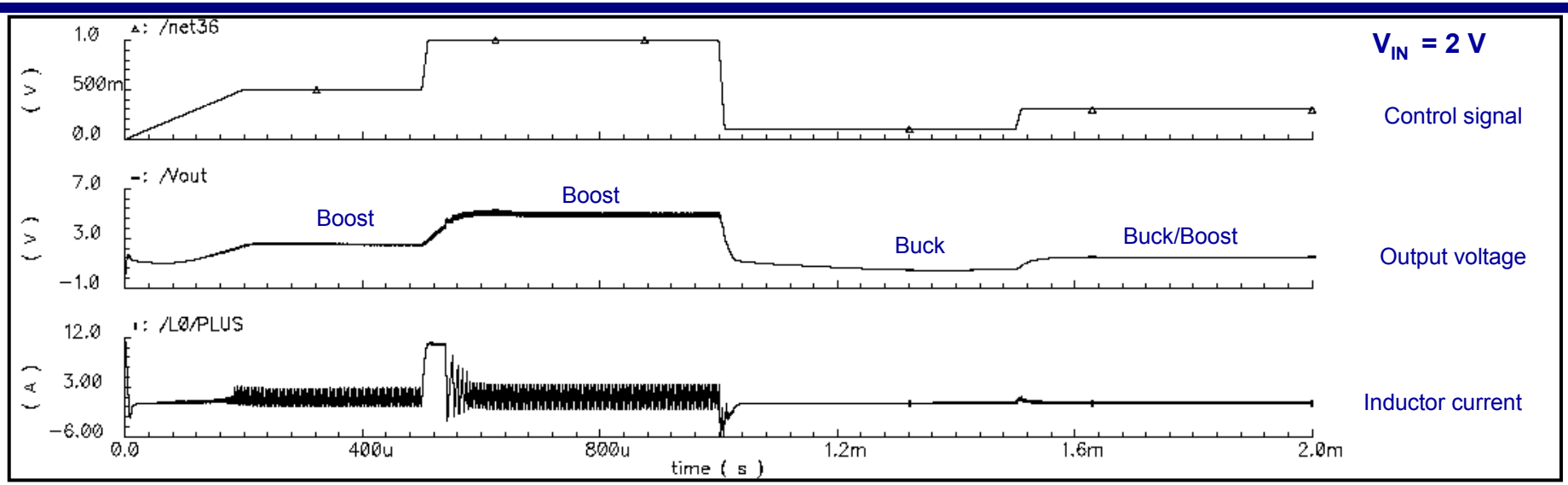
- By incorporating spread-spectrum switching, the ripple noise voltage is distributed over a wider frequency band resulting in a lower side-lobe power with respect to the signal power.

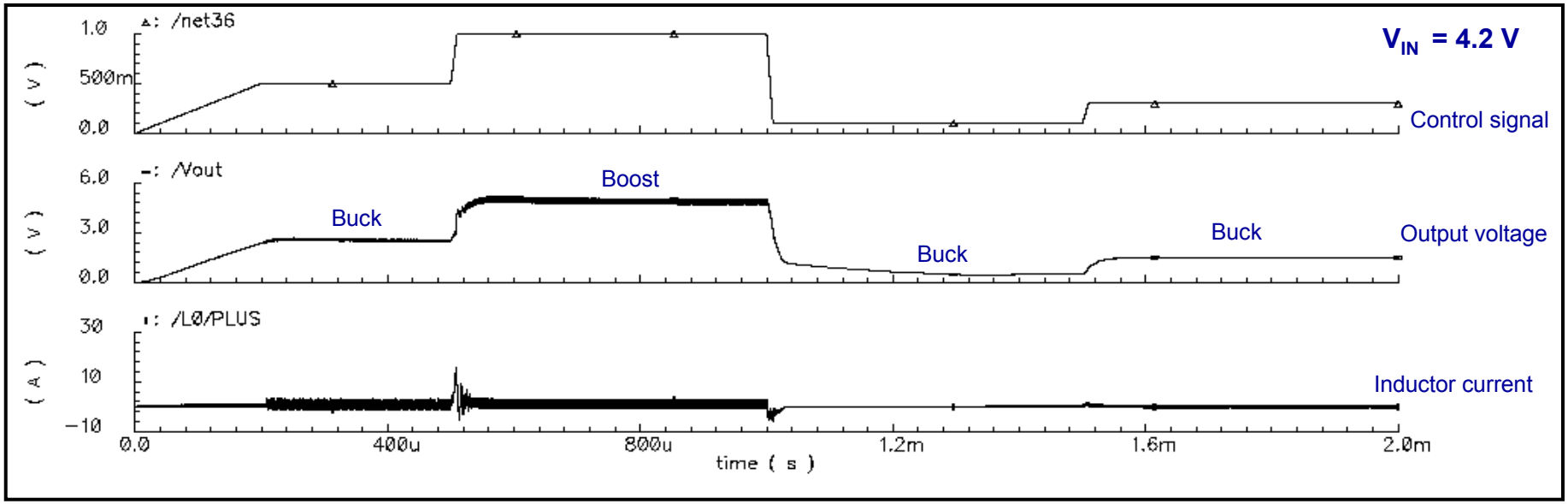
⇒ *Improved signal-to-noise ratio*



Reduced Out-of-band distortion using switching
(a) Without spread-spectrum, (b) With spread-spectrum

Simulation Results





Summary

- A top-down approach for integrated circuit design of key building blocks in a non-inverting buck-boost converter is discussed considering the challenges involved in realizing low voltage circuits.
- **Performance Enhancements**
  - *Efficiency Improvement*
    - Buck/Buck-Boost/Boost Mode of operation
    - Dynamic sizing of power MOSFET switches
    - Decreasing/Increasing the switching frequency to minimize losses depending on the battery voltage
  - *Accuracy*
    - DC accuracy $\Rightarrow$ Low –offset, wide input common-mode range op-amp for error amplifier
    - Ripple voltage/Noise spectrum $\Rightarrow$ Spread-spectrum clocking
    - Transient accuracy $\Rightarrow$ Higher bandwidth, slew rate
- **Future Work:** *Layout and performance evaluation of the IC*