State-of-the-Art in Phase-Locked Loop Filter Integration

Matt Duff
Advisor: Dr. Gabriel A. Rincón-Mora

Georgia Institute of Technology

Introduction

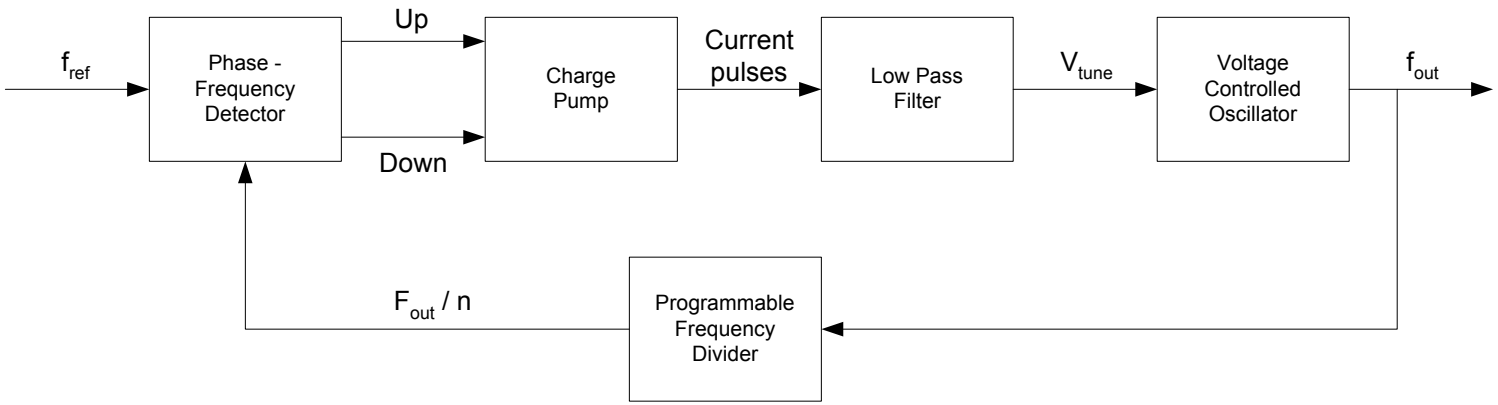
GOAL: Integrate all components of a PLL on-chip: allowing easy inclusion in system-on-a-chip designs.

WHY IS THIS HARD?
Capacitors in the loop filter are very large, so consume too much silicon area. Historically, the loop filter has been placed off chip.

POSSIBLE SOLUTIONS:
- Passive filter with large resistance
- Active filter
- Dual path (combination of both active and passive)
- Discrete Time
- Capacitor Multiplier

EXAMPLE APPLICATIONS: Bluetooth; Cell Phones; consumer products requiring a frequency synthesizer

PLL Block Diagram



EASY TO INTEGRATE BLOCKS:

- **Phase-Frequency detector**: Two D flip-flops and an AND gate
- **Charge pump**: Two current sources and two switches
- **Frequency divider**: Can be simple or complicated. But consists solely of active devices, so easy to integrate.

HARD TO INTEGRATE BLOCKS:

- **VCO** – Difficult to make high quality inductors on-chip
- **Loop Filter** – Capacitors consume large amounts of silicon area

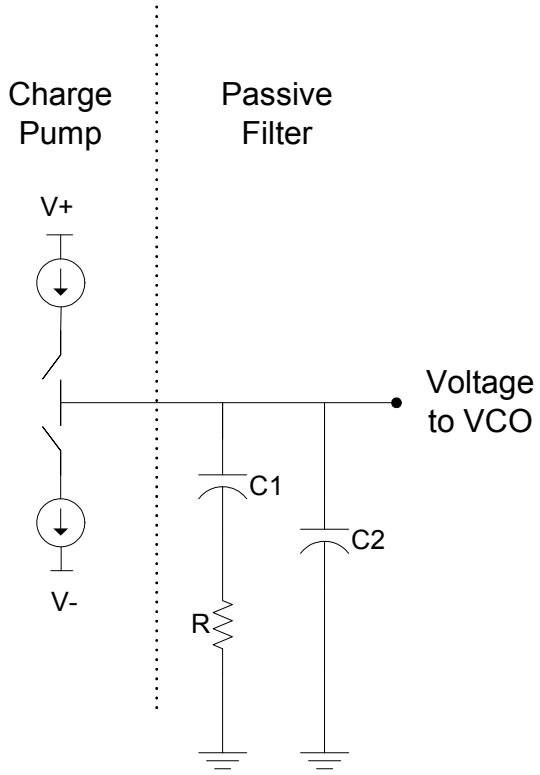
Passive Filter with Large Resistor

Method: Bandwidth is proportional to the charge pump current and C. Decrease charge pump current to decrease capacitance

But: Decrease the loop current → must increase loop filter's R to keep the PLL stable.

Issues:
- Thermal noise from large resistor
- Charge pump noise: overall current decreases → noise current is a bigger proportion of total

Application areas:
- Noise tolerant designs
- Large loop bandwidths
- Quick design time
- Low power.



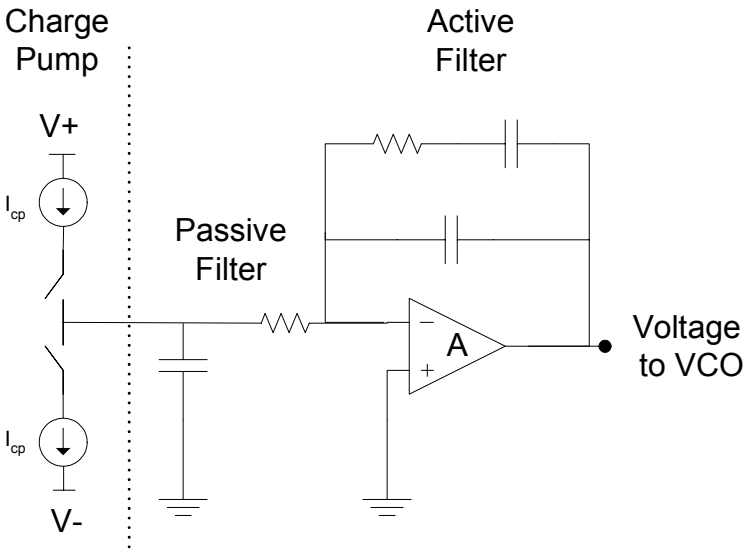
Active Filter

Method: Active filter for higher order filters:
- More flexibility
- Better noise filtering

But: Doesn't address fundamental issue of capacitor size.

Issues:
- Requires a passive filter before active filter so op amp doesn't have to work so hard
- Power. Better filtering → requires quicker op amp → requires more power.
- Op amp noise.

Application areas: Not prevalent in today's literature.



Dual Path

Method:

Op amp integrator

- Low frequencies → low op amp power
- Tiny current → tiny C_z

+

Passive filter

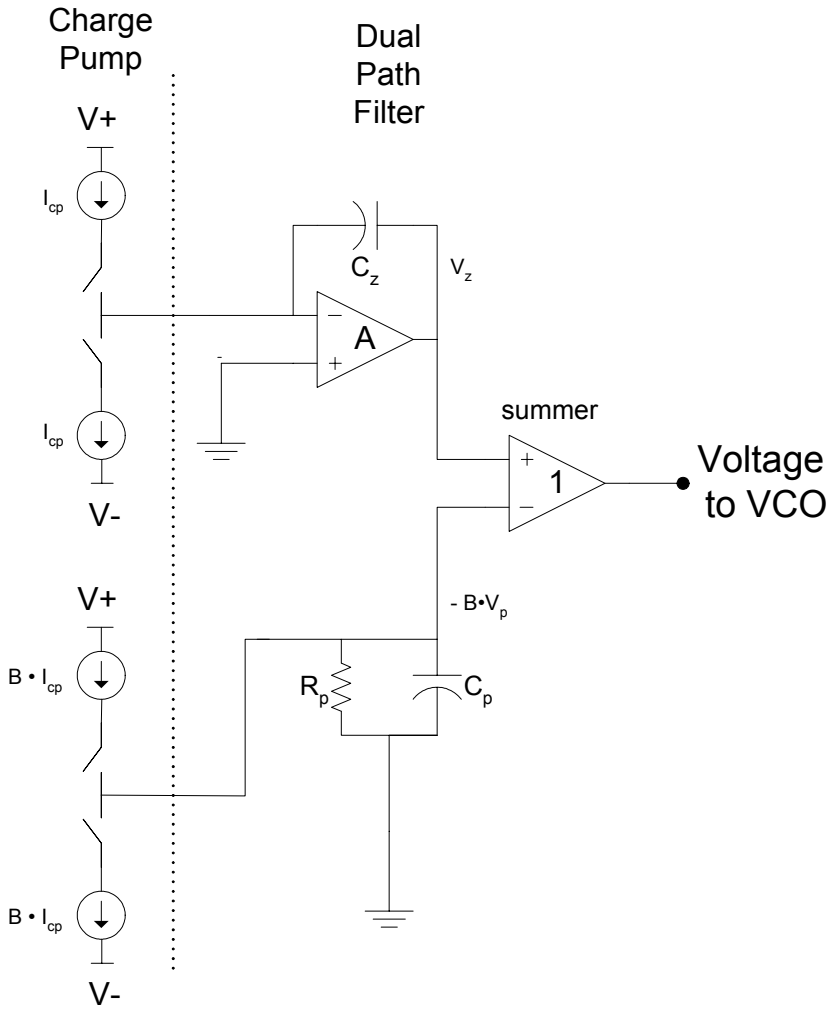
- Large current → R_p can be small)

Issues:

- Requires two charge pumps → Delay mismatches
- Noise from op amp and summer

Application areas:

- Capacitance small → quite popular
- Application must be noise tolerant

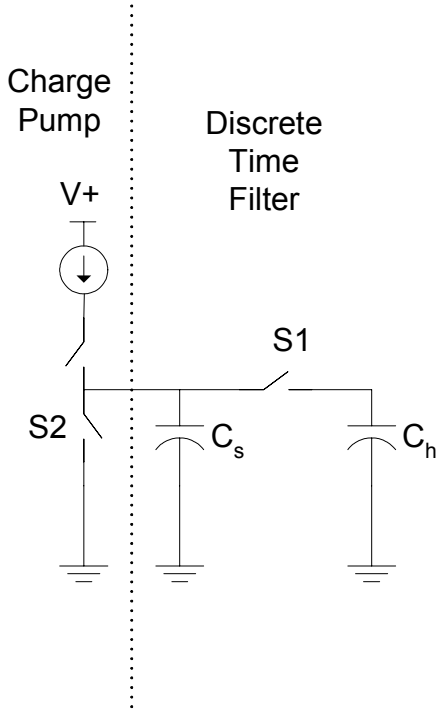


Discrete Time

Method: Filter cutoff is dependent on switching time, not capacitor size.

Issues:
- One pole at origin instead of two → noise rejection lower
- Clock feedthrough from the sampling switch
- Finite lock-in range

Application areas: Main advantage -fast switching speed, since only one pole at origin (Type 1) instead of standard two (Type 2).



Capacitor Multiplier

Method: Multiply small capacitor into big one with active circuitry.

$I = C\, dV/dt$

$\downarrow$

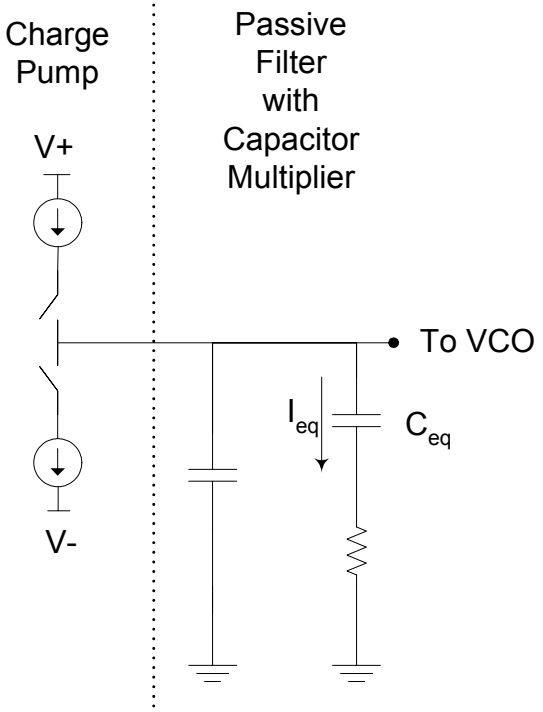
$KI = KC\, dV/dt$

Issues:

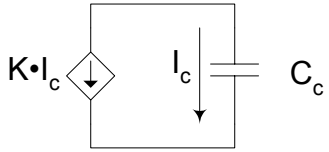
- Power (proportional to charge pump current).
- Leakage current vs. voltage range tradeoff
- ESR. Not a problem in passive circuit configuration, because R dominates.

Application areas:

- Promising newcomer
- Needs more research.



Where C_{eq} is:



$I_{eq} = K \bullet I_c + I_c$

$C_{eq} = (1 + K)C_c$

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Conclusions

	Large Resistor Passive	Active	Dual Path	Discrete Time	Capacitor Multiplier
Power	Fantastic	Bad	Medium	Good	Medium
Noise	Bad	Medium	Medium	Bad	Good
Area	Bad	Bad	Good	Good	Good

Capacitor multiplier looks promising. Needs more research in power and leakage current.

Can capacitor multiplier and dual path be combined?