

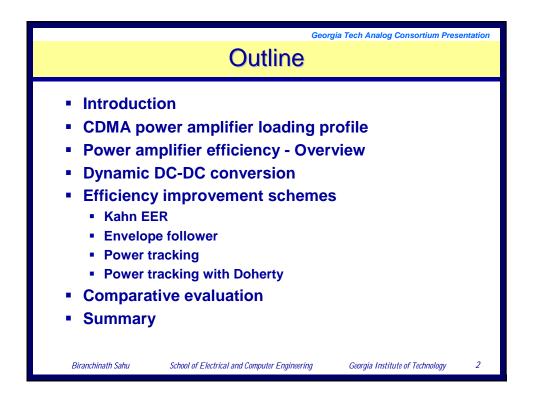
## Efficiency Enhancement of CDMA Power Amplifiers in Mobile Handsets Using Dynamic Supplies

Georgia Tech Analog Consortium Presentation

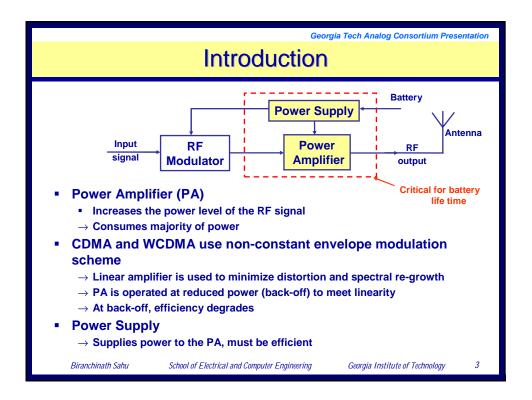
## **Biranchinath Sahu**

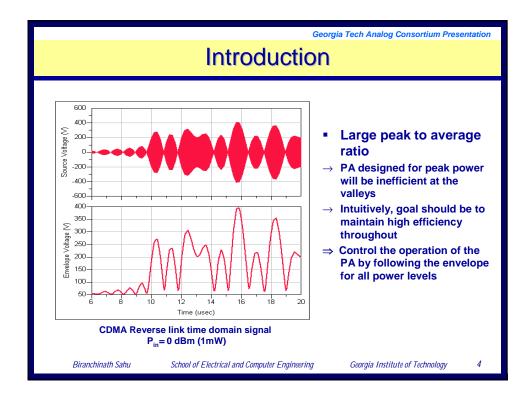
Advisor: Prof. Gabriel A. Rincón-Mora

Analog Integrated Circuits Laboratory School of Electrical and Computer Engineering Georgia Institute of Technology October 25, 2002

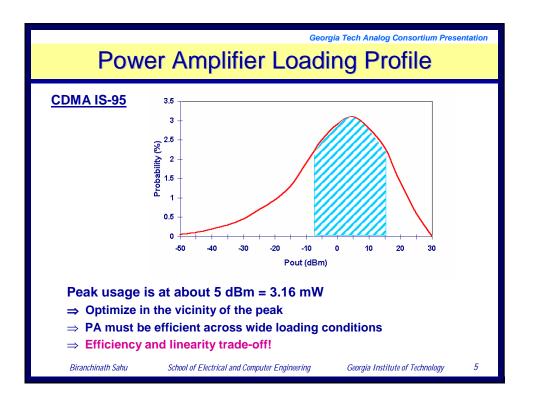


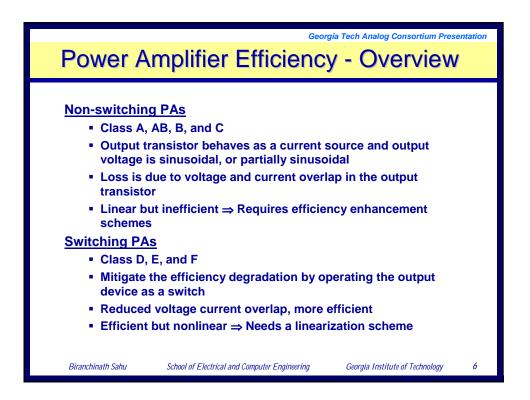




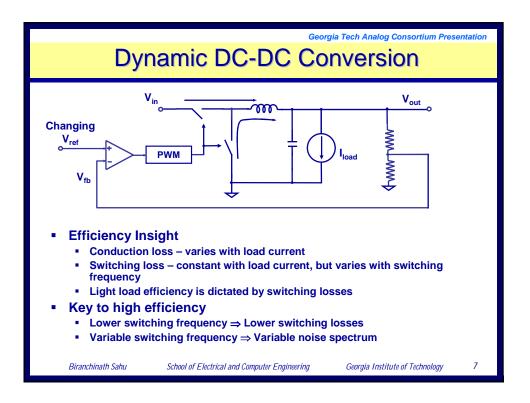


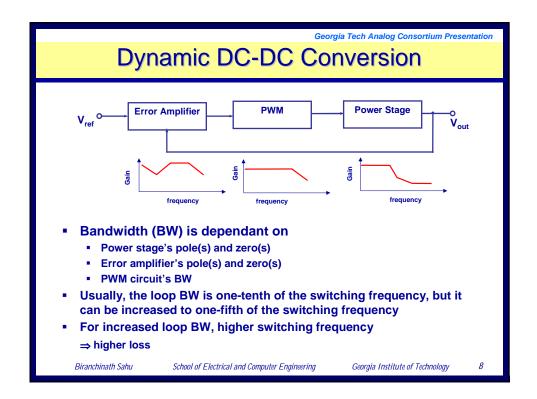




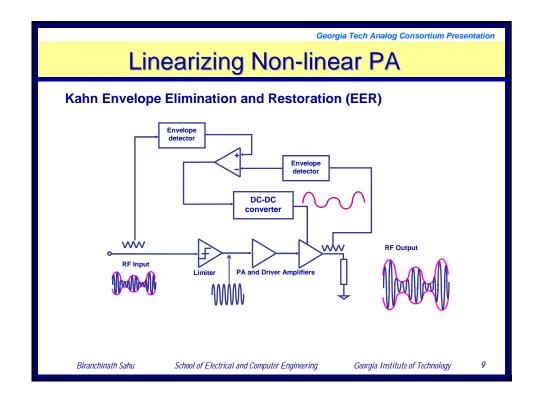






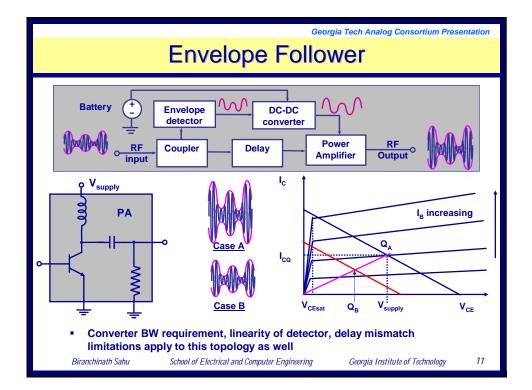


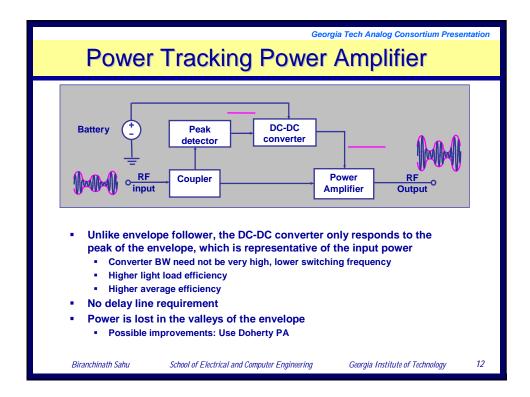




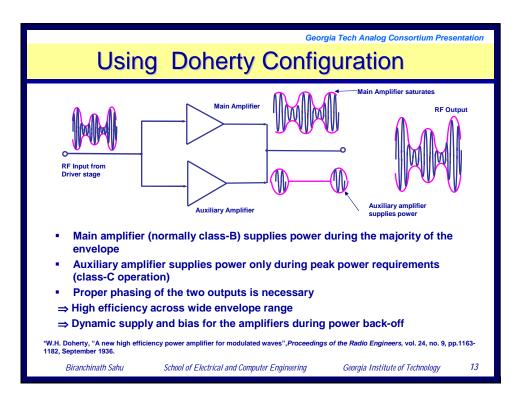
	L ba			a Tech Analog Consortium Prese	ntation
	LIN	earizing	Non-line	ear PA	
• DC	-DC Conve	ter Limitation	s		
		requirement	-		
	Converter			the baseband signal BW	
	Scheme	Baseband BW	Converter BW	Switching frequency	
	CDMA IS-95	1.25 MHz	5 MHz	25 MHz	
	WCDMA	3.84 MHz	15.36 MHz	76.8 MHz	
• Otl	her Limitatior Delay mismat 20 ns <sup>*</sup>		lope signal and R	F signal must be within	
	•	nvelope detector	ation of low powe	r signals (-70 dBm)	
	At present, th		been shown for 3 NADC standard)	0 kHz baseband	
	Intermodulation in Kahi 8, December 1996.	n-Technique Transmitters",	IEEE Transactions on Micro	wave Theory and Techniques, vol. 44, n	o. 12,
Birar	nchinath Sahu	School of Electrical and C	Computer Engineering	Georgia Institute of Technology	10











Scheme	Advantages	Disadvantages
EER	Theoretically maximum efficiency can be obtained	Large converter BW, higher switching frequency, inefficient Linearity of detector, phase distortion of limiter, delay mismatch
Envelope follower	Potentially efficiency is close to the peak PA efficiency	Large converter BW, higher switching frequency, inefficient Linearity of detector, delay mismatch
Power Tracking	•DC-DC converter need not be fast, lower switching frequency, efficient at light load • Simplest scheme	Peak efficiency may not be great (but average efficiency is what matters for battery life)
Power Tracking +Doherty	DC-DC converter need not be fast, lower switching frequency, efficient at light load High peak load efficiency as well	•Higher complexity •Power divider and combiner needs to be micro strip lines (on-chip components are lossy*)



