A Low Voltage, Dynamic Buck-Boost Converter Supply for RF Power Amplifier

Georgia Tech Analog Consortium Presentation
October 25, 2002

Biranchinath Sahu

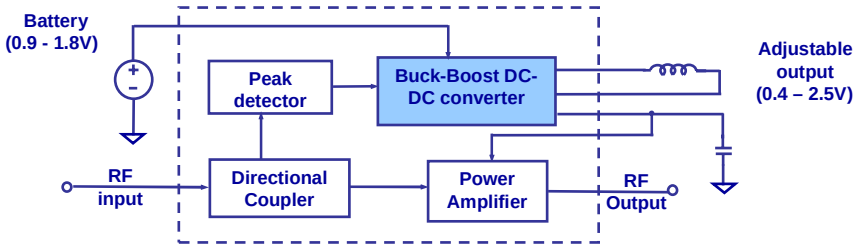
Advisor: Prof. Gabriel A. Rincón-Mora

Analog Integrated Circuits Laboratory
School of Electrical and Computer Engineering
Georgia Institute of Technology

Abstract

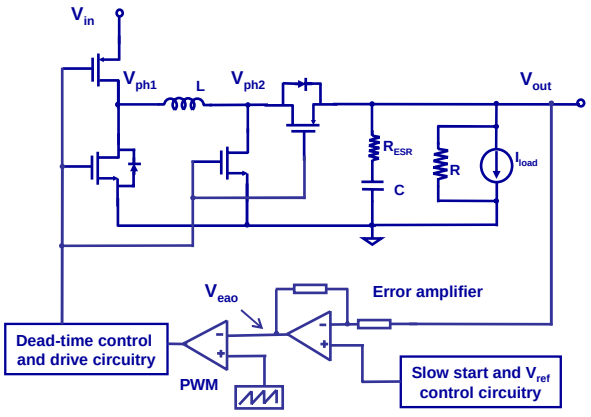
- Efficiency of linear power amplifier (PA) can be enhanced by controlling the bias current and supply voltage dynamically
- For single cell NiMH/NiCd low voltage (0.9–1.8 V) applications, the supply voltage to the PA can be higher or lower than the battery voltage
  ⇒ Dynamic Buck-Boost converter
- Buck-Boost converter presented in this work
  - System: Supplies 0.4-2.5 V output voltage from 0.9-1.8 V battery input voltage *on-the-fly*
  - Intuitive time average model of the power stage
  - Compensation
  - Slow start and dynamically adaptive reference

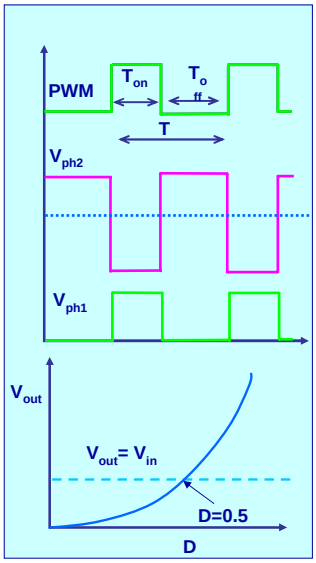
Efficient Linear Power Amplifier System



- Only off-chip components: Converter filter components (L and C)
  Power Amplifier output match, RF choke
  Directional coupler
- DC-DC converter: Dynamically adaptive
- Supply: Low voltage battery
- Technology: 0.25 µm CMOS

Synchronous Buck-Boost Converter



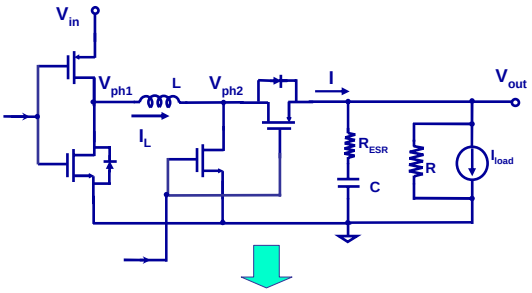


DC condition: L = short

$V_{ph1\text{-}ave}= Dv_{in}= V_{ph2\text{-}ave} = V_{out}(1-D)$

$\Rightarrow V_{out}= V_{in}*D/(1-D)$

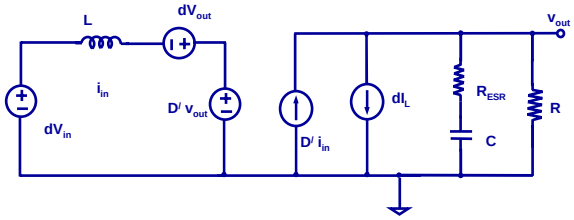
Power Stage Time-average Model



When duty cycle increases from D to D+d the following changes occur:

⇒ V_{ph1} ↑ by dV_{in}
⇒ V_{ph2} ↓ by dV_{out}
⇒ I_L ↑ by i_{in1}
⇒ I ↓ by dI_L, but ↑ by $D'i_{in1}$
⇒ V_{out} ↓ initially, but ↑ by v_{out1}

⇒ V_{ph2} ↑ by $D'v_{out1}$
⇒ I_L increase changes $i_{in1} \rightarrow i_{in}$
⇒ V_{out} increase changes $v_{out1} \rightarrow v_{out}$



Time-averaged small-signal model

Net change:

$V_{ph1} \rightarrow V_{ph1} + dV_{in}$
$V_{ph2} \rightarrow V_{ph2} - dV_{out} + D'v_{out}$
$I \rightarrow I + D'i_{in} - dI_L$
where $D' = 1 - D$

Power Stage Transfer Function

Control-to-output transfer function is given by:

$$H_{o-d}(s) = H_{od}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1-\frac{s}{\omega_{z2}}\right)}{1+\frac{s}{\omega_0 Q}+\frac{s}{\omega_0^2}} \qquad H_{od} = \frac{V_{out}}{DD'}$$

Capacitor ESR zero = $\omega_{z1} = \frac{1}{R_{ESR}C}$

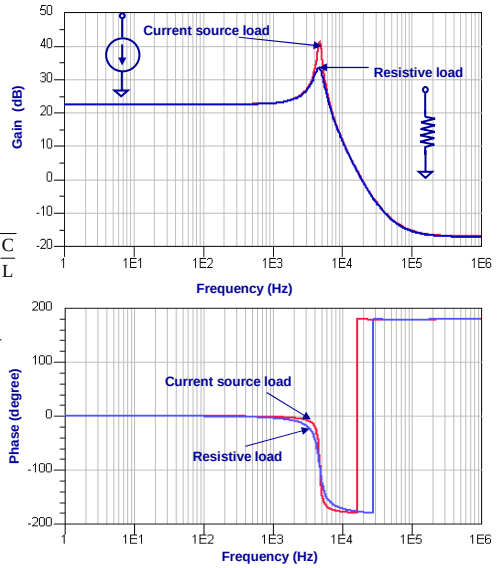
Complex double poles = $\omega_0 = \frac{D'}{\sqrt{LC}}, Q = D' R\sqrt{\frac{C}{L}}$

RHP zero due to opposing feed forward action of inductor = $\omega_{z2} = \frac{D'^2 \frac{V_{out}}{I_O}}{DL}$

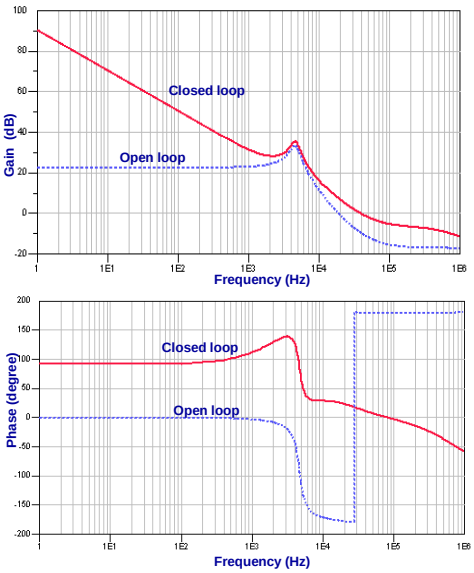
With V_{out}=2.5V, I_O=0.6 A, D =0.7, L=2.2 µH, C= 47 µF, R_{ESR} = 70 mΩ

H_{od} = 21.52 dB, f_0 = 4.695 kHz
f_{z1}= 48.37 kHz, f_{z2}= 38.75 kHz

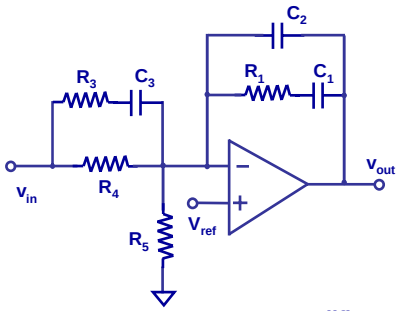
For current source load Q is higher



Compensation and Stability



- Pole at origin
- Double zero at LC complex poles
- Pole at desired loop BW (less than RHP zero)
- Pole >> loop BW to ensure –20dB/dec slope

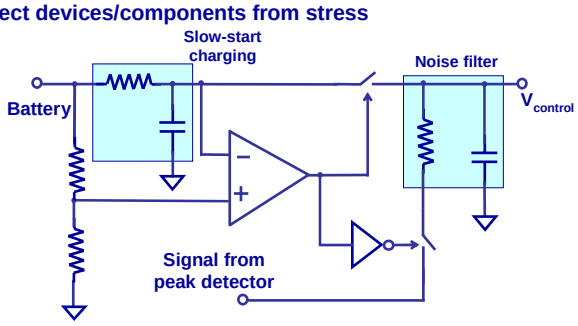


Type-III Error Amplifier

$$A_{EA}(s) = \frac{1}{sR_4(C_1+C_2)}\left(\frac{[1+sC_3(R_4+R_3)](1+sR_2C_2)}{[1+sR_2(C_1+C_2)](1+sR_3C_3)}\right)$$

Slow-start and Dynamic Control Signal

- Slow start is required to:
  - Reduce start-up transients
  - Protect devices/components from stress



⇒ During start-up, the comparator output is high, the slowly charging capacitor voltage provides the control signal

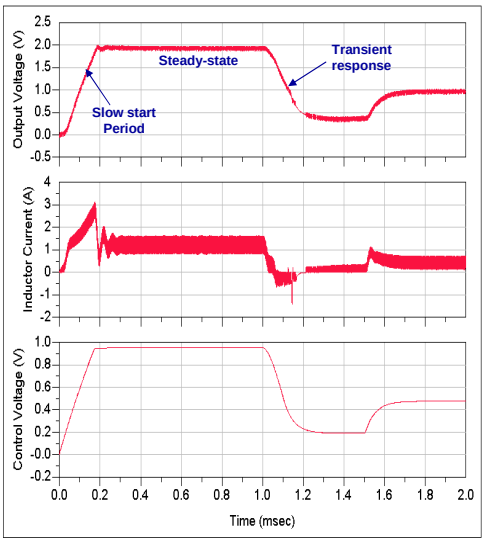
⇒ When slow-start capacitor voltage reached a threshold, comparator output goes low, signal from peak detector takes over control

⇒ The noise filter prevents occurrence of high frequency transients in the control node

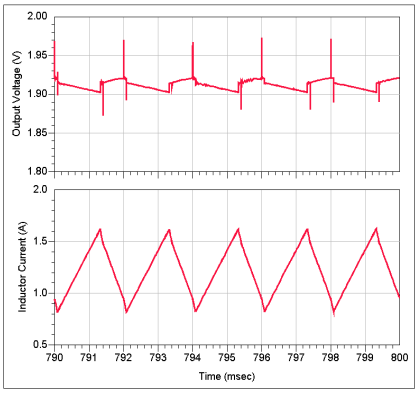
Georgia Tech Analog Consortium 9

Simulation Results

Slow-start and worst case transient operation



Steady-state waveforms



Control Voltage: 0.95 V

Georgia Tech Analog Consortium 10

Summary

- A dynamic, synchronous, non-inverting, voltage-mode buck-boost converter is presented
- Intuitive time-average small signal model of the power stage is derived without complex mathematical analysis
- A Type –III error amplifier compensation scheme is presented
- A slow-start and dynamic control signal circuit is designed for reducing start-up and high frequency transients
- Simulation results for a dynamic control signal shows that the converter is capable to respond worst case power adjustment for CDMA IS-95 specification (1dB in 666 µsec)
- Goal: Integrated dynamically adaptive DC-DC converter with Power Amplifier