An Adjustable, Highly-Linear, Low-Offset Gm-C Filter for Lossless and Accurate Current-Sensing of DC-DC Converters

H. Pooya Forghani-zadeh
Advisor: Prof. Gabriel Rincón-Mora
Georgia Tech Analog and Power IC Lab
Georgia Institute of Technology
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Abstract

Abstract:
Current-sensing circuits are essential for protection and control of the switching regulators. Our proposed technique estimates the inductor current by filtering the voltage across it. Furthermore, the inductor value and its ESR are measured during the startup to boost the accuracy. This poster discusses the circuit design of the filter required for the current sensing. The design challenges are adjustable gain and bandwidth; high linearity to prevent the systematic offset; and continuous, low glitch, high frequency, low-offset operation (input-referred offset<100uV).
The System

- Buck converter
- $V_{in}=2.7V-5V$
- $V_{out}=1.5V$
- $f_s=1MHz$
- $I_{load}>1A$
- Current-mode PWM Controller
- Current-sensing accuracy <7.5% at full load current over temperature and load current range.
- Inductor range inductance: 2uH-6uH
  ESR: 12mΩ-18mΩ
- Temperature range: $T=-40°C-85°C$

Gm-C Filter Specifications

- First order low-pass filter
- Cut-off frequency: Adjustable, 1KHz-5KHz
- Second pole (parasitic): >10MHz
- Gain: Adjustable, 2-44
- Linearity: $\frac{\Delta g_m}{g_m} < -70\text{dB}$
  (avoid systematic offset)
- Input referred offset: <100uV
- Continuous operation
- $\text{In}+$ range: -0.6-$V_{DD}$
- $\text{In}-$ range: 0.6-1.5
**Gm1 Implementation (1)**

\[ I_o = K \frac{V_{in+} - V_{in-}}{R} \]
\[ I_o = G_{m1}(V_{in+} - V_{in-}) + G_{m2}(V_{aux+} - V_{aux-}) \]
\[ G_{m1} = \frac{K}{R} \]

K is the current mirror gain.

**Gm1 Implementation (2)**

- **Current Mirror**
  - Current mirror gain is adjusted digitally.
  - The switches are not in the signal path and do not affect the AC response.

- **Summing amplifier**
  - A simple dual input two-stage amplifier.
  - BW > 10 MHz.
  - Input range range -0.6-VDD-1.
  - Gains of main and auxiliary paths can be different for proper offset cancellation.
**G_m2-C**

\[ G_{m2} = \frac{1}{R_2} \]

\( G_{m2} \) is adjusted digitally

A large output capacitor (C) relative to the switch parasitic capacitance ensures that switch parasitic capacitance does not alter the ideal first order AC response

\[ Z_{in} = \frac{R_1 + R_2}{1 + (R_1 + R_2)Cs} \]

Since \( C \gg C_p \)

\[ Z_{in} = \frac{R_1 + R_2}{1 + (R_1 + R_2)Cs} \]

**Ping-Pong Operation**

Auto zeroing:

Offsets are stored at the hold capacitor

\[ V_{in} = g_m \frac{R_1}{1 + g_m R_2} V_{in} + g_m \frac{R_1}{1 + g_m R_2} V_{in} + g_m \frac{R_1}{1 + g_m R_2} V_{in} + V_{error} \]

Normal operation:

\[ V_{in} = g_m V_{in} (R_1 || R_2) + V_{in} \frac{g_m (R_1 || R_2)}{1 + g_m R_2} \]

\[ V_{in} - V_{in} \frac{1}{1 + g_m R_2} R_1 || R_2 \]

\[ 0 \]

\[ 0 \]

\[ 0 \]

Simulations

**Ping Pong Transient Response**

Because of output capacitor high value, the glitch at the transition is almost negligible (1.2mV).

**Future Work**

- Design of control logic to perform the low offset calibration
- Two stage offset cancellation along with output offset storage is used to reach very low input referred offset (<10uV) at the input

Phase 1: Offset cancellation of the $G_m$-C filter to eliminate saturation of preamplifier in phase 2
Phase 2: Offset cancellation of the measurement system
Phase 3: Input voltage measurement