An Adjustable, Highly-Linear, Low-Offset G_m-C Filter for Lossless and Accurate Current-Sensing of DC-DC Converters

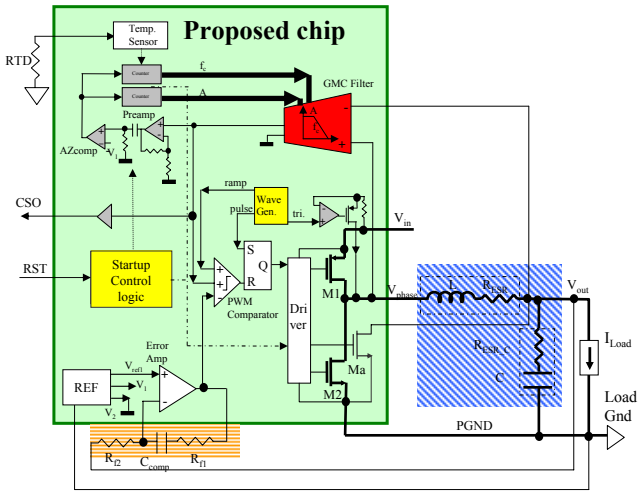
H. Pooya Forghani-zadeh
Advisor: Prof. Gabriel Rincón-Mora
Georgia Tech Analog and Power IC Lab
Georgia Institute of Technology
October 2004

Abstract

Abstract:
Current-sensing circuits are essential for protection and control of the switching regulators. Our proposed technique estimates the inductor current by filtering the voltage across it. Furthermore, the inductor value and its ESR are measured during the startup to boost the accuracy. This poster discusses the circuit design of the filter required for the current sensing. The design challenges are adjustable gain and bandwidth; high linearity to prevent the systematic offset; and continuous, low glitch, high frequency, low-offset operation (input-referred offset<100uV).

GEDC Industry Advisory Board, October 2004.
© 2004 Georgia Electronic Design Center. All Rights Reserved. Redistribution for profit prohibited.

The System



- Buck converter
- V_{in}=2.7V-5V
- V_{out}=1.5V
- f_s=1MHz
- I_{load}>1A
- Current-mode PWM Controller
- Current-sensing accuracy <7.5% at full load current over temperature and load current range.
- Inductor range
  inductance: 2uH-6uH
  ESR: 12mΩ-188mΩ

Temperature range:
T=-40°C-85°C

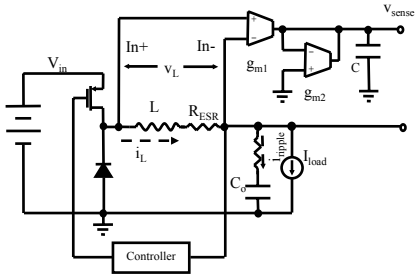
G_m-C Filter Specifications

- First order low-pass filter
- Cut-off frequency: Adjustable, 1KHz-5KHz
- Second pole (parasitic): >10MHz
- Gain: Adjustable, 2-44

$$\begin{cases} i_L = \dfrac{1}{(R_{ESR}+sL)} v_L \\ v_{sense} = \dfrac{g_{m1}}{g_{m2}}\left(\dfrac{1}{1+s(C/g_{m2})}\right) v_L \end{cases}$$

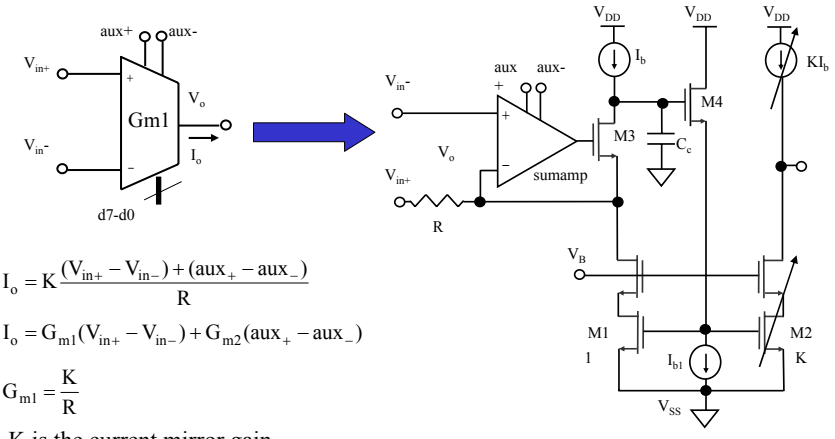
- Linearity: $\dfrac{\Delta g_m}{g_m} < -70\text{dB}$

  (avoid systematic offset)



- Input referred offset: <100uV
- Continuous operation
- In+ range: -0.6-V_{DD}
- In- range: 0.6-1.5

G_{m1} Implementation(1)



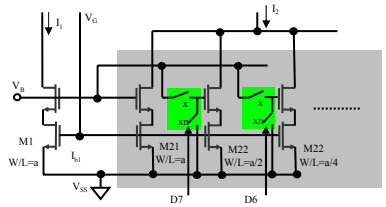
$$I_o = K\frac{(V_{in+} - V_{in-}) + (aux_+ - aux_-)}{R}$$

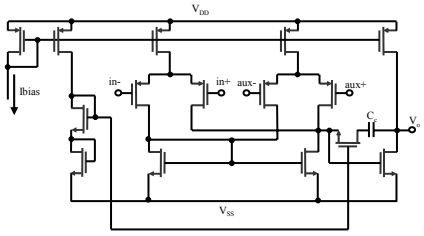
$$I_o = G_{m1}(V_{in+} - V_{in-}) + G_{m2}(aux_+ - aux_-)$$

$$G_{m1} = \frac{K}{R}$$

K is the current mirror gain

G_{m1} Implementation(2)





Current Mirror

- Current mirror gain is adjusted digitally
- The switches are not in the signal path and do not effect the AC response

Summing amplifier

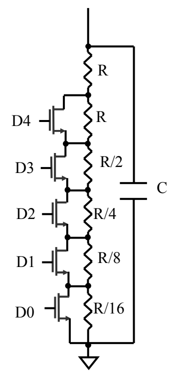
- A simple dual input two-stage amplifier
- BW>10MHz
- Input range range -0.6-V_{DD}-1
- Gains of main and auxiliary paths can be different for proper offset cancellation

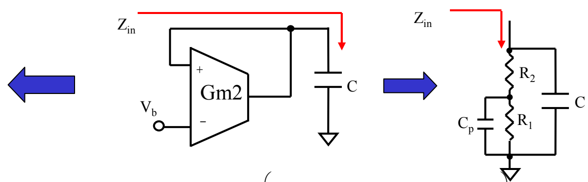
G_{m2}-C

$G_{m2}=1/R_2$

G_{m2} is adjusted digitally

A large output capacitor (C) relative to the switch parasitic capacitance ensures that switch parasitic capacitance does not alter the ideal first order AC response

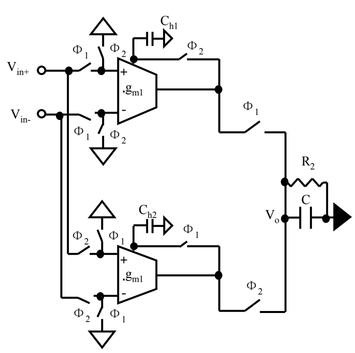




$$Z_{in}=\frac{R_1+R_2}{1+(R_1+R_2)Cs}\left(\frac{1+s(R_1\,||\,R_2)C_p}{1+s(R_1\,||\,R_2)C_p\dfrac{C}{C+\frac{R_1}{R_1+R_2}C_p}}\right)$$

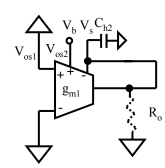
Since $C>>C_p$ $\quad Z_{in}=\dfrac{R_1+R_2}{1+(R_1+R_2)Cs}$

Ping-Pong Operation



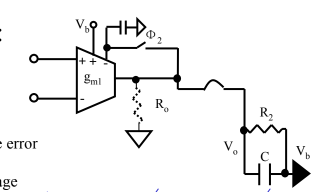
Auto zeroing:

Offsets are stored at the hold capacitor



$$V_s=\frac{g_{m1}R_o}{1+g_{m2}R_o}V_{os1}+\frac{g_{m2}R_o}{1+g_{m2}R_o}V_{os2}+\frac{g_{m2}R_o}{1+g_{m2}R_o}V_b+V_{error}$$

Normal operation:

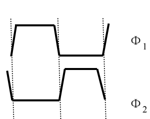


V_{os1}: main input offset
V_{os2}: auxiliary input offset
V_{error}: charge injection voltage error
R_o: Gm1 output resistance
V_s: hold capacitor stored voltage

$$V_o=g_{m1}V_{in}(R_o\,||\,R_2)+V_{os1}\frac{g_{m1}(R_o\,||\,R_2)}{1+g_{m2}R_o}+V_{os2}\frac{g_{m2}(R_o\,||\,R_2)}{1+g_{m2}R_o}-g_{m2}(R_o\,||\,R_2)V_{error}$$
$$+V_b-V_b\left(\frac{1}{1+g_{m2}R_o}\frac{R_2}{R_o+R_2}\right)$$

0 0 0 0

Clock

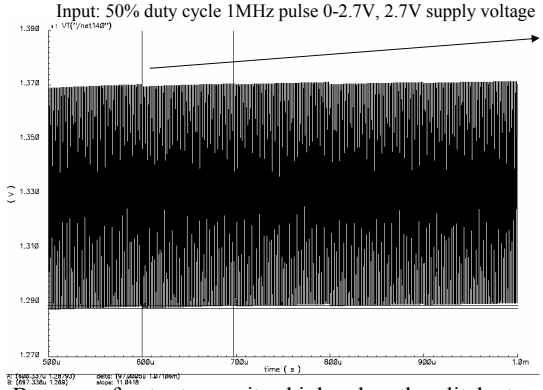


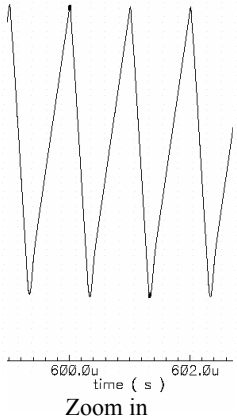
GEDC Industry Advisory Board, October 2004.
© 2004 Georgia Electronic Design Center. All Rights Reserved. Redistribution for profit prohibited.

Simulations

Ping Pong Transient Response

Input: 50% duty cycle 1MHz pulse 0-2.7V, 2.7V supply voltage



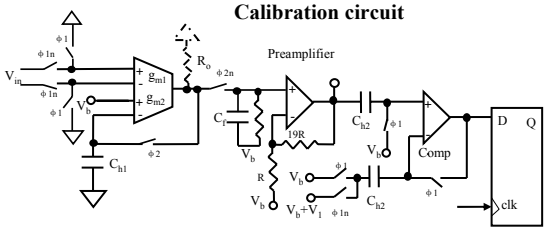


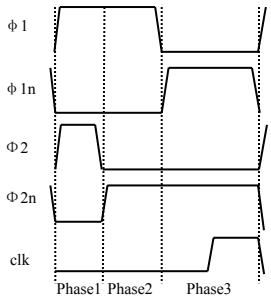
Because of output capacitor high value, the glitch at the transition is almost negligible (1.2mV).

Zoom in

Future Work

- Design of control logic to perform the low offset calibration
- Two stage offset cancellation along with output offset storage is used to reach very low input referred offset (<10uV) at the input





Phase1: Offset cancellation of the G_m-C filter to eliminate saturation of preamplifier in phase 2
Phase 2: Offset cancellation of the measurement system
Phase 3: Input voltage measurement