Low Voltage Design Techniques and Considerations for Integrated Operational Amplifier Circuits

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ABSTRACT

The pertinent literature on low voltage Operational Amplifiers is surveyed and techniques suitable for operation at low power supply voltages are identified. Designs implemented in standard Bipolar, BiCMOS, and CMOS technologies are classified and characterized. The lower limit of the power supply voltage is identified as well as the performance tradeoffs that are sacrificed as that limit is approached. The three aforementioned technologies are compared quantitatively and qualitatively.

I. INTRODUCTION

Today's atmosphere and demands continue to drive operating voltages down, especially for widely used components such as the Operational Amplifier. Some of the motivations driving the market are integration, battery operated components, and biomedical instrumentation. The increased packing densities require reduction in feature size that, in turn, reduces breakdown voltages thereby limiting the power supply. Portable low power electronics pushes toward battery powered products, 1.5-3V. Furthermore, human implantable devices, like pacemakers, also drive the market. It is, therefore, the intended goal to develop low voltage design techniques and compare them for CMOS, Bipolar, and BiCMOS technologies The conventional techniques for improving performance require revision and adjustment because of reduced headroom in a low voltage environment.

In order to ascertain a low voltage methodology, the design of the Op Amp is partitioned, input and output stages. These are built by current mirrors, gain stages, and differential pairs. Hence, low voltage techniques will be developed first and later applied to input and output stages. Concepts from state of the art Op Amp architectures that are conducive toward lower power supplies are introduced. The considerations involved in reducing the supply voltage are highlighted. Such performance parameters considered include noise, distortion, frequency response, bandwidth, gain, common mode range and ultimate low power supply limit. A brief review of devices and associated limitations is warranted to establish a comparative basis.

I.I Devices

The devices considered are MOSFET's (Metal Oxide Semiconductor Field Effect Transistors), BJT's (Bipolar Junction Transistors), and JFET's (Junction Field Effect Transistors). The structure of a JFET is accomplished by pinching a tub/well with the opposite type material which is readily accomplished if tubs/wells are present thus available in CMOS and Bipolar. However, the characteristics of the JFET in the Bipolar process are more favorable due to lower pinch off voltages.

Those parameters that are important in analog design are reviewed and summarized in Table 1.1. The MOSFET has two strong inversion modes of operation, triode and saturation. The triode

region is characterized by low output impedance making it non-ideal for most analog applications. Under weak inversion, sub-threshold region, the MOSFET is slow due to lower currents; hence, operation in this mode will not be considered. Consequently, the saturation region, $V_{ds} > V_{dssat}$ ~0.3-0.5V, is chosen as the reference region of operation. The design parameters are w/l and either V_{gs} (setting I_{dsat}) or I_{dsat} (setting V_{gs}). The output impedance is modeled through r_{ds} and parametized through λ (Table 1.1). The transconductance, g_m, is directly proportional to the square root of the aspect ratio times the DC current through the device. The maximum gain of a single device then simply becomes $g_m r_o$, which is inversely proportional to the square root of the bias current and directly proportional to the aspect ratio. Thus, in order to increase the gain one must decrease the bias current and/or increase the aspect ratio. Another important parameter in low voltage circuit design is the turn on voltage of the device, V_{gs}, which is ultimately limited by the threshold voltage, V_{th}. This threshold is a process parameter, excluding bulk effect, with a typical value of 0.7V. The ultimate power supply limit in circuits is mainly determined by this turn on voltage, typically ~0.9V. Noise is an important design consideration since the SNR (Signal to Noise Ratio) decreases as the signal swing decreases. The two main contributing factors of noise in a MOSFET are 1/F and white noise. The 1/F noise is caused by the surface irregularities of the gate/channel junction while the white noise is governed by the resistance of the channel [24]. The input referred 1/F noise voltage is inversely proportional to the area (wl) while white noise is inversely proportional to g_m, Table 1.1. The noise current is negligible since the input impedance of the device is quasi infinite.

The JFET is modeled similarly to the MOSFET and its parameters are summarized in Table 1.1. There are two major differences, namely, the JFET is a depletion mode device and it does not exhibit 1/F noise. It does not have 1/F noise because the operation of the device is beneath the surface. This implies that there is no surface irregularity involvement, which was the main source of 1/F noise in the MOSFET. The JFET is therefore conducive toward low voltage applications.

The design parameters for the BJT are the saturation current, I_s (directly proportional to the emitter area), and either V_{be} (setting I_c) or I_c (setting V_{be}). The minimum voltage for V_{ce} must be V_{cesat} to prevent saturation, ~100-200mV. The output impedance is modeled through V_a, $1/\lambda$

equivalent. The g_m of the BJT is directly proportional to the bias current as opposed to the square root relationship of the MOSFET and JFET, thus exhibiting enhanced transconductance behavior. The maximum gain of the device is V_a/V_t, Table 1.1, which is an independent relation, unlike the MOSFET's and JFET's. The turn on voltage is V_{be}, ~0.6-0.8V, implying that it is slightly better suited for low voltage design than the MOSFET, V_{on} is lower by ~100-200mV. The input impedance of the BJT is lower than the MOSFET and JFET counter parts, r_π or B_o/g_m. This leads to a non-negligible input current noise governed by the shot noise of the PN junction at the base [24]. However, the input referred noise voltage is lower than the MOSFET's because the operation is underneath the surface, as is the JFET. The noise voltage is mostly governed by shot noise and the thermal noise generated by the base spreading resistance, Table 1.1.

Over all, the MOSFET has higher input impedance and lower input current noise. Due to its threshold operation it is also better suited for low offset analog switches [23]. The JFET is a depletion mode device having better noise characteristics than the MOSFET. When using low gain devices, like the FET's, caution must be exercised in frequency compensation. In a common source gain stage configuration a RHP (Right Hand Plane) zero [21] exists denoted by

$$RHPZ = \frac{g_m}{2\pi C_{dg}} \tag{1.1}$$

The BJT, on the other hand, exhibits higher transconductance, thus moving the zero to higher frequencies. Furthermore, the BJT has lower noise and lower voltage drops, V_{be} and V_{cesat}, than the MOSFET. Due to the BJT's exponential behavior, V_{be} changes slightly with changing currents thus making it better for referencing voltages [23] and operating under a wide range of currents. As the power supply voltage is reduced the following may be concluded for all devices:

1. Gate/Base drive decreases thus current decreases hence bandwidth decreases.

2. V_{db} and $V_{csubstrate}$ decrease thus their associated junction capacitance increases hence the bandwidth decreases since [19,22]

$$C_{np} = \frac{Cjo}{\left[1+\frac{V_{np}}{\Psi}\right]^{nc}} \tag{1.2}$$

3. Signal swings decrease thus SNR decreases [19].

	MOS	BJT	JFET
I	$I_{dtri}=K'(w/l)[2(V_{gs}-V_t)V_{ds}-V_{ds}^2]$	$I_c=I_s \exp(V_{be}/V_t)$ $\{I_s \alpha A_{emit}\}$	$I_d=(I_{dss}/V_p^2)(V_{gs}-V_p)^2$
	$I_{dsat}=(K'/2)(w/l)(V_{gs}-V_t)^2$		
g_m	$(2BI_{dsat})^{0.5}$ $\{B=K'(w/l)\}$	I_c/V_t $\{V_t=kT/q\}$	$-[4(I_{dss}/V_p^2)I_d]^{0.5}$
r_o	$r_{ds}=(\lambda I_{dsat})^{-1}$	$r_{oq}=V_a/I_c$	$r_{oj}=(\lambda I_d)^{-1}$
$g_m r_o$	$(2B/I_{dsat})^{0.5}/\lambda$	V_a/V_t	$[4(I_{dss}/V_p^2)/I_d]^{0.5}/\lambda$
V_{on}	$V_{gs}=V_{dssat}+V_{th}$	V_{be}~0.6-0.8V	$V_{gs}=V_{jsat}+V_p$ $(V_p<0)$
V_{sat}	$V_{dssat}=(2I_{dsat}/B)^{0.5}$	V_{cesat}~0.1-0.2V	$V_{jsat}=(I_d V_p^2/I_{dss})^{0.5}$
r_{in}	~ infinite	$r_\pi=B_o/g_m$	rev. bias PN junct.
C_{in}	C_{gs}	C_π	C_{gs}
f_t	$g_m/2\pi(C_{gs}+C_{gd}+C_{gb})$	$g_m/2\pi(C_p+C_m)$	$g_m/2\pi(C_{gs}+C_{gd})$
I_{noise}^2	$2qI_{gdc}$	$2qI_b+KI_b/f$	$2qI_{gdc}$
V_{noise}^2	$8kT/(3g_m)+K_{fm}/(fwl)$	$4kTr_b+2qI_c r_e^2+ KI_b r_b^2/f$	

Qualitative Comparison	MOS	BJT	JFET
High Input Impedance	X		
Better Frequency Response		X	
Low 1/F Noise		X	X
Low Current Noise	X		X
Low Voltage Noise		X	X
High DC Gain		X	
Low Turn on Voltage			X
Good Voltage Reference		X	
Zero Offset Analog Switches	X		
Low Saturation Voltage		X	

Table 1.1 Device Comparison [22,23,24,28]

II. CURRENT MIRRORS

The current mirror is widely used as active loads and bias circuit elements. A brief look at the low voltage considerations and design techniques is justified for the evaluation and design of amplifiers. The four important characteristics of the mirror are output impedance, current error, bandwidth, and low power supply limits. Three types of mirrors will be discussed, namely, the simple, cascode, and regulated cascode mirror.

II.I Simple Mirror

The simple CMOS and Bipolar current mirrors have characteristic output impedances that are consistent with the technology, r_{ds} and r_{oq} respectively, Table 1.1. The predominant source of current error in the CMOS version is due to the finite output impedance of the mirroring devices,

$$I_d = I_{dsat}(1+\lambda Vds) \tag{2.1.1}$$

where the effect of r_{ds} is represented by λ. Using this equation the output current, I_o, relationship can be derived as depicted in Table 2.1. The bipolar version has the same source of error in addition to yet another that dominates. This is due to input base currents, B error. By noting that

$$I_c = BI_b \tag{2.1.2}$$

and

$$I_{in} = I_{c1} + 2I_{c1}/B = I_o + 2I_o/B \tag{2.1.3}$$

the relationship in Table 2.1 can be derived for I_o. This B error is usually minimized by connecting another BJT from the collector to the base of Q1, Figure 2.1 (a). This is not a good low voltage technique for the power supply is limited to $2V_{be}$. However, this can be fixed by using complimentary BJT's, Figure 2.1 (a). This comes at the expense of circuit area, complexity, and power dissipation. Care must be taken in the bias of the feedback transistors and frequency compensation because of the high gain nature of the loop.

Over all, the output impedance of the simple mirror is comparable in both CMOS and Bipolar technologies. The bandwidth is greater and noise lower for the Bipolar version. Furthermore, the CMOS circuit's low power supply limit, V_{gs}, is greater than the Bipolar's, V_{be}. However, this is at the expense of greater current error, B effect.

II.II Cascode Mirror

The evolution from the simple mirror to the cascode is readily apparent, Figure 2.1. The simple mirror is simply cascoded so that the output impedance is increased. The arrangement is such that only one turn on voltage plus a saturation voltage [$V_{on4} + V_{sat1}$ in Figure 2.1 (b)] limit the supply rails [17]. Generically, the output impedance can be formulated by the following relationship

$$R_{out} = g_m r_o R \tag{2.2.1}$$

where g_m and r_o correspond to the cascoding device's transconductance and output impedance while R is the effective resistance at the drain of the output mirroring device, M2. Evidently the MOSFET is better suited for cascoding because the BJT's r_π lowers the effective impedance at the drain of the mirroring device, Q2, from r_o to $r_\pi // r_o$, Figure 2.1 (b). Hence, the CMOS circuit typically yields higher output resistance. In terms of power supply limits, current error, and bandwidth the conclusions from the simple mirror apply. The Bipolar implementation yields higher bandwidth, lower supply voltage limits, lower noise, and larger output current error.

A BiCMOS implementation yields a trade off in bandwidth, output impedance, and power supply limitations. For instance, Figure 2.1 (c) has the bandwidth of the CMOS circuit with an improved power supply limit, ($V_{gs}+V_{dssat}$ to $V_{be}+V_{dssat}$). Figure 2.1 (d) has the bandwidth of the Bipolar circuit with improved output impedance, Br_o to $g_m r_{ds} r_{oq}$. The power supply limit is a compromise between CMOS and Bipolar, $V_{gs}+V_{ce}$. Depending on what characteristic is to be optimized the BiCMOS technology offers greater flexibility and enhanced performance.

If the noise generated by the current mirror is important, a cascode mirror can be formulated using passive components. The output current noise of the circuit in Figure 2.1 (b) is

$$I_n^2 = V_{n2}^2 g_{m2}^2 + V_{n3}^2 g_{m3eff}^2 \tag{2.2.2}$$

where V_n^2 is the input referred noise voltage and g_{m3eff} is the effective transconductance from the gate/base of M3/Q3 which can be derived to be

$$g_{meff} = g_m / (1+g_m R) = g_m / (1+g_m r_{ds2}) \tag{2.2.3}$$

Thus, the dominant source of noise is the mirroring device, M2/Q2, since the transconductance of M3/Q3 is degenerated by r_{o2}. Hence, the noise of the circuit is reduced by using a lower noise non-degenerated element. This can be accomplished by using resistors, white noise only elements [24].

This is implemented by using the simple mirror with resistors between source/emitter and the negative power supply. The output impedance is again dominated by equation (2.2.1) and the effective noise is reduced to a degenerated active device and a resistor. The limit of the power supply voltage is now governed by a turn on voltage and the voltage across the resistor. Therefore, the amount of degeneration is a design parameter that compromises power supply voltage, output resistance, and noise. This is a technique that is applicable to any technology.

	CMOS	**Bipolar**	**BiCMOS**
SPL. MIRROR			
R_{out}	r_{ds}	r_{oq}	CMOS or Bip
Lowest V	V_{gs}	V_{be}	CMOS or Bip
I_o	$I_{in}(1+\lambda V_{gs})/(1+\lambda V_{ds})$	$I_{in}[B/(B+2)]$	CMOS or Bip
W_{3db}	$g_m/(C_{gs12}+C_{dg2miller}+C_{db1})$	$g_{mq}/(C_{\pi 12}+C_{miller2}+C_{c1})$	CMOS or Bip
CASCODE			
R_{out}	$\sim g_m r_{ds}^2$	$\sim B r_{oq}$	$\sim g_m r_{ds} r_{oq}$ or $B r_{oq}$
Lowest V	$V_{gs}+V_{ds}$	$V_{be}+V_{ce}$	$V_{be}+V_{ds}$ or $V_{gs}+V_{ce}$
I_o	$\sim I_{in}$	$\sim I_{in}[B/(B+2)]$	~ CMOS or Bip
W_{3db}	~ SPL. MIR.	~SPL. MIR.	~ CMOS or Bip
REG. CASCODE			
R_{out}	$\sim g_m^2 r_{ds}^3$	$\sim g_{mq} B r_{oq}^2$	~ CMOS or Bip or combo
Lowest V	$V_{gs}+2V_{ds}$	$V_{be}+2V_{ce}$	~ CMOS or Bip or combo
I_o	$\sim I_{in}$	$\sim I_{in}[B/(B+2)]$	~ CMOS or Bip
W_{3db}	~ SPL. MIR.	~ SPL. MIR.	~ CMOS or Bip

Qualitative Comparison	**CMOS**	**Bipolar**	**BiCMOS**
High Output Impedance	X		X
Low Current Error	X		X
Low Supply Voltage		X	X
Better Frequency Response		X	X
Low Noise		X	X

Table 2.1 Mirror Comparison in the different technologies [21,22,23,27]

II.III Regulated Cascode Mirror

The Regulated Cascode Mirror is a direct evolution of the cascode implementation with added local feedback to boost the output impedance. This is illustrated in Figure 2.3 (a) where a two step evolution is shown [27,29]. In the final version there is local feedback plus level shifting to assure a low voltage across M1, V_{ds1}. The extra current source added to M2, I_b, is used to match the current through M1, I_b+I_{out}. Transistors M3,4 are designed to have a V_{gs} difference of V_{ds1}. If ideal current sources and matched transistors are assumed, approximate relationships can be derived and the results of which are shown in Table 2.1. In the Bipolar version, Figure 2.3 (b), a resistor is used to define the voltage across the mirroring device, Q1. Other sources of output current error have now been added to the circuit, Q3,5's B errors. Hence,

$$I_o(1+1/B_5) + I_{b2}(1-1/B_3) = (I_{in}+I_{b1})\,(1-2/B_1) \qquad (2.3.1)$$

whose error can be minimized by appropriately adjusting I_{b1} and I_{b2}.

The comparative conclusions are summarized in Table 2.1. The CMOS realizations yield lower output current error and higher output resistance. Bipolar, on the other hand, yields higher bandwidth, lower noise, and reduced power supply limits. Due to the complexity and frequency response of the regulated cascode, its use is limited. This encourages the use of the simple and cascode mirrors in most analog design applications. BiCMOS, again, offers the greatest flexibility yielding maximized performance.

III. DIFFERENTIAL PAIRS

The differential pair is widely used in the input, output, and intermediate stages of Op Amps. This section will briefly review a variety of differential pairs available along with a qualitative conclusion as to their advantages and disadvantages. There are several characteristics that are essential in a low voltage atmosphere such as transconductance, input impedance, matching, voltage offset, frequency response, and noise.

The four basic types of input pairs in the literature include MOS, BJT, JFET, and CJFET (Channel Junction Field Effect Transistor) available in CMOS [26]. The CJFET is simply a

MOSFET with the bulk terminal as the input, biasing the gate to a fixed potential so that an inversion channel may be formed. By modulating the bulk, the depletion layer is modulated along with the channel thereby changing the current through the device. The region of operation is limited by the bulk to source potential, $V_{bs} < V_{be}$~.6V. The CJFET is operated as a depletion mode device which makes it attractive for low voltage design. An expression can be derived for the effective transconductance as follows

$$g_{mbs} = g_m \frac{-\gamma}{\sqrt{2\phi - Vbs}} = \mathrm{B}(V_{gs} - V_t)\frac{-\gamma}{\sqrt{2\phi - Vbs}} \tag{3.1}$$

where g_m is the transconductance of the normally gate driven MOSFET, and γ and ϕ are process parameters. The behavior of the device is similar to the JFET.

Over all, the CJFET differential pair is conducive for a good CMR (Common Mode Range) due to its low turn on voltage. However, the device suffers from high input capacitance and low transconductance. The only advantage of the CJFET over the MOS device is its depletion mode operation. The CJFET, however, adds flexibility to the design process and may prove to be useful in certain applications. The noise of the CJFET is equivalent to the MOSFET. Generally, noise performance can be optimized by using PFET's, lower noise due to the lower bulk resistance [24]. Furthermore, natural devices (without threshold implant adjustment) have lower noise [5]. Thus, the least noise conducive FET's for low voltage are PFET's and Natural NFET's; the natural PFET is excluded because its threshold voltage is typically higher than the adjusted version.

The MOS input pair has the advantage of high input impedance over its bipolar counterpart. The BJT pair, on the other hand, has lower noise, higher transconductance, and better frequency response. The BJT also exhibits higher matching and therefore lower offset voltage. However, the BJT has lower input impedance which can be ameliorated by emitter degeneration. This increases the input impedance to

$$R_{in} = r_\pi + (1+B)R \tag{3.2}$$

but degenerates the transconductance as shown in equation (2.2.3). Due to the low gain nature of the CMOS input pair a RHP zero may arise, equation (1.1). The JFET pair has the advantage of being a

depletion mode device, as the CJFET, and low noise, as the BJT, due to its below the surface operation. Over all, the BJT is more advantageous, Table 3.1, and therefore suited for the task of high performance low voltage design.

There are several techniques to improve matching of the input pair which translate to lower input offset voltage. One way is to use a common centroid configuration where the devices are symmetrically arranged so that their center of mass lies in the center. One typically implements this in combination with cross coupling multiple transistors in parallel. The use of multiple transistors yields better matching. Emitter/Source degeneration is yet another technique for improving matching [23] at the expense of transconductance degradation. Matching of resistors is improved by placing extra resistors on the edge of the real ones so that etching mismatches are minimized.

Qualitative Comparison	**MOS/CJFET**	**BJT**	**JFET**
High g_m		X	
High R_{in}	X		X
Matching		X	
Voltage Offset		X	
Better Freq. Response.		X	
Noise		X	X
Low Turn On Voltage	X		X

Table 3.1 Differential Pair Comparison .

IV. GAIN STAGES

Techniques such as cascoding, emitter/source followers, and Darlingtons are not appropriate in low voltage design because of headroom limits [10]. The use of diode connected transistors must be limited to one per transistor stack due to its high voltage drop. This intimates that the ultimate limit on low voltage supply is the actual turn on voltage of the device available in the process plus the head room associated with its load. Common source/emitter configurations are encouraged [23] for gain and maximized voltage swings. The predominant source of noise in an Op Amp lies in the first stage, given a high input stage gain. This makes the noise of the intermediate stages less important. There are four different gain stages that are applicable in low voltage design; these are a

single stage, complimentary two stage, level shifted two stage, and differential pair gain stage. Since the gain per stage can not be enhanced by the conventional techniques, multiple stages may be necessary. This adds poles to the circuit making it difficult to compensate and maintain a decent UGF/GBW (Unity Gain Frequency/Gain Bandwidth Product). Therefore, techniques for compensation become intrinsic to the design process.

IV.I Single, Two, and Level shifted Two Stage

A common source/emitter configuration is used for the single and two stage gain cells. Thus, the input voltage swing is maximized to a turn on voltage below the supply rail. CMOS realizations minimize loading to the previous stages. On the other hand, Bipolar has higher g_m, lower noise, lower supply voltage limit, and better frequency response. A BiCMOS design gives greater flexibility yielding combined characteristics. For instance, Figures 4.1 (a,b) effectively yield the MOS's high input impedance with the BJT's high g_m and current handling capability. Furthermore, frequency compensation is dominated by a miller BJT gain stage.

A gain stage can also be accomplished through the use of a differential pair, Figure 4.1 (c), in CMOS, Bipolar, or BiCMOS. The disadvantage of this stage is that the input signal is limited to

$$V_{in} > V_{on}+V_{sat}+V_{\text{-}power} \qquad (4.1.1)$$

which is a V_{sat} greater than the ones in Figures 4.1 (a,b). The simple mirror added to the schematic of Figure 4.1 (c) is not necessary but added to illustrate a possible folding configuration that is consistent with the low voltage design techniques developed. Table 4.1 summarizes the conclusions derived.

Qualitative Comparison	**CMOS**	**Bipolar**	**BiCMOS**
High R_{in}	X		X
High Gain		X	X
Better Frequency Response		X	X
Low Power Supply Limit		X	X

Table 4.1 Gain Stage Comparison in the Different Technologies .

IV.II Frequency Compensation

A technique for compensating multi-stage Op Amps is the Multi-path Hybrid Nested Miller Compensation [16]. This is the evolutionary culmination of the Nested Miller Compensation described in [4]. A simplified model of a four stage Op Amp and associated compensation are shown in Figure 4.2 (a). There are three miller capacitors and their effects on the circuit are as follows:

1. C_{m1} pushes P4 to higher frequencies while pulling P3 down to lower frequencies.
2. C_{m2} pushes P2 to higher frequencies while pulling P1 down to lower frequencies.
3. C_{m3} pushes P3 to higher frequencies, due to feedback path, and further pulls P1 down to lower frequencies.

Disregarding the multi-path bypass, the following applies:

$$GBW \sim g_{m1}/C_{m3} \tag{4.2.1}$$

$$P2 \sim g_{m2}/C_{m3} \tag{4.2.2}$$

$$P3 \sim g_{m3}C_{m3} / (C_{m1}C_{m2}) \tag{4.2.3}$$

$$P4 \sim g_{m4}/C_L \tag{4.2.4}$$

Thus, GBW < P2,3,4 yields the practical implementation of

$$GBW \sim \frac{g_{m1}}{C_{m3}} \sim \frac{g_{m3}\,C_{m3}}{2C_{m1}\,C_{m2}} \sim \frac{g_{m4}}{4\,C_L} < \frac{g_{m2}}{4\,C_{m3}} \quad [16] \tag{4.2.5}$$

The heart of the operation of the multi-path concept lies in adding two signals whose effective frequency response yields a higher GBW, Figure 4.2 (b). The bypass path has its first pole where the second pole of the main path lies. The single pole response GBW of both signals must be equal for proper pole/zero matching. It is important that the latter condition is met and it may be accomplished circuit-wise by duplicating the input differential pair and feed forwarding its output to the last stage as implemented in [16], illustrated in Figure 4.2 (a) with the G_{mx} stage (dashed lines), creating the following necessity,

$$GBW \sim g_{m1}/C_{m3} \sim g_{mx}/C_{m1} \tag{4.2.6}$$

and relaxing the relation from (4.2.5) to P3 < P2 < GBW < P4

$$GBW \sim \frac{g_{m1}}{Cm3} \sim \frac{10 g_{m3} Cm3}{Cm1\, Cm2} \sim \frac{g_{m4}}{2 C_L} <\sim \frac{5 g_{m2}}{Cm3} \qquad [16] \quad (4.2.7)$$

Each time a stage is added the GBW has to decrease and the amount it decreases is minimized by the aforementioned technique better than the conventional compensating techniques [16].

V. INPUT STAGES

The input stage of an Op Amp is a key issue for it must follow several design specifications, such as CMR (Common Mode Range), high gain, low noise, constant g_m over the CMR, and low offset voltage [1,4,5,23,24]. In low voltage design the restrictions become more acute. For instance, the SNR (Signal to Noise Ratio) tends to decrease as the power supplies decrease thus requiring low noise circuits. This behavior elucidates the necessity to have rail to rail input stages with constant g_m over the CMR. The next intrinsic limitation lies in transistor stacking and associated turn on voltages. Taking the premise that a differential pair must be used, the lowest supply voltage limitation will be achieved if the voltage drop to either supply from the input pair is only ~ $V_{ds}(V_{ce})$. These voltage drops correspond to the headroom of the tail current source and the load. The only topology that achieves this is the folded architecture. Therefore, the literature survey is limited to folded topologies with constant g_m rail to rail input stages. The techniques used to achieve rail to rail operation with constant g_m will be discussed first followed by the folding considerations.

V.I Rail to Rail Operation with Constant g_m over the CMR

The CJFET is excluded as an input pair possibility because of its low g_m and associated limit, $V_{bs} < V_{be}$, for proper operation. Furthermore, complimentary CJFET's are not usually available in standard CMOS technologies. Therefore, MOS, BJT, and JFET are the chosen candidates for the input pair. The JFET can readily have a good CMR because of its inherent depletion mode operation, typically utilized as the input in low noise BiFET Op Amps. To achieve a rail to rail CMR using the MOSFET or BJT a complimentary differential pair configuration is used, Figure 5.1.1.1,2 and 5.1.2. The N type pair operates when the common mode input, V_{cm}, is close to the positive power supply while the P type operates when V_{cm} is close to the negative power

supply. When V_{cm} is at mid range of power supplies both differential pairs are active. The transconductances for the three regions of operation are g_{mn}, $g_{mp} + g_{mn}$, and g_{mp}. In order to maintain a constant transconductance over the CMR the following relation must be maintained

$$g_{mp} + g_{mn} = Constant \tag{5.1}$$

V.I.1 CMOS Implementation

A. Mirror: Through the addition of some mirrors the three independent regions can yield the same transconductance as shown in Figure 5.1.1.1 [1]. This is the evolutionary culmination of circuits implemented by [7,12]. When $V_{cm} > V_{b1}$ (~$V_{ss}+V_{gs}+V_{ds}$) and $V_{cm} > V_{b2}$ (~$V_{dd}-V_{sg}-V_{sd}$), Mb1 is off, Mb2 is on, and Mp1,2 are off, then $I_n = 4I_b$ or

$$g_{mn}+g_{mp} = g_{mn} = [2(4I_b)B]^{0.5} = 2[2(I_b)B]^{0.5} \tag{5.1.1.1}$$

where B_n and B_p are designed to be B. When $V_{b2} > V_{cm} > V_{b1}$, Mp1,2 and Mn1,2 are on and Mb1 and Mb2 are off thus Ip=In=Ib or

$$g_{mn}+g_{mp} = [2(I_b)B]^{0.5} + [2(I_b)B]^{0.5} = 2[2(I_b)B]^{0.5} \tag{5.1.1.2}$$

When $V_{cm} < V_{b1}$ and $V_{cm} < V_{b2}$, Mb2, Mn1,2 are off & Mb1, Mp1,2 are on, thus $I_p = 4I_b$ or

$$g_{mn}+g_{mp} = g_{mp} = [2(4I_b)B]^{0.5} = 2[2(I_b)B]^{0.5} \tag{5.1.1.3}$$

Evidently the transconductance is the same in all three regions of operation, Figure 5.1.1.1 (b) illustrates the resulting g_m. The non-ideality is due to the transition from one region of operation to the other. During this transition the sum of the currents is constant but not the square root of the effective tail currents, necessary for constant g_m. The power supply rail is limited by the input pairs, CMR = Power Supply > $V_{onn}+V_{onp}$ (defined in Table 1.1).

B. MTL: Applying the MTL (MOS Translinear Loop) Theory [6] keeps the sum of the square root of the currents constant. The theory is based on the relation for V_{gs}, Table 1.1,

$$V_{gs}=(2I/B)^{0.5}+V_{th} \tag{5.1.1.4}$$

Thus, in a V_{gs} loop

$$\Sigma V_{gsccw} = \Sigma V_{gscw} = \Sigma[\,(2I/B)^{0.5}+V_{th}\,]_{ccw} = \Sigma[\,(2I/B)^{0.5}+V_{th}\,]_{cw} \tag{5.1.1.5}$$

where ccw denotes "counter-clockwise" and cw "clockwise." If V_{th} and B match

$$\Sigma I^{0.5}{}_{ccw} = \Sigma I^{0.5}{}_{cw} \tag{5.1.1.6}$$

In the mean time, equation (5.1) may be rewritten (if B's match) as

$$I_p^{0.5} + I_n^{0.5} = constant \qquad (5.1.1.7)$$

Thus, equation (5.1.1.6) is of the appropriate form to achieve the conditioning equation (5.1.1.7).

This technique was used successfully for the implementation of a rail to rail input stage with constant g_m by [1,2,15]. It is noteworthy to mention that matching of B and V_{th} are key parameters in maintaining proper operation. Second order effects, like bulk effect, must also be taken into consideration. Furthermore, the MTL theory holds true only if all transistors are on, above V_{th}. The topology that seems best suited for matching and low voltage is implemented by [2] and shown in Figure 5.1.1.2. Transistors M1 through M4 form the MTL yielding the following equation

$$2I_o^{0.5} = I_p^{0.5} + I_n^{0.5} \qquad (5.1.1.8)$$

where I_p and I_n are simply translated to the complementary input pairs via mirrors. The differential pair Mb1,2 is used for common mode feedback as well as to limit the tail currents to less than $4I_o$. A current limit is necessary when one of the transistors in the loop is off, dropping out of MTL operation. Suppose V_{cm} is low enough so that the N type input pair is off ($I_n = 0$) and $4I_o$ goes through Mb1, then the following is true (1:1 mirror)

$$I_o+I_n+4I_o = I_o+4I_o = I_o+I_p \quad or \quad I_p = 4I_o \qquad (5.1.1.9)$$

The same happens in the other direction for I_n. The power supply limit of this circuit becomes CMR = Power Supply > $2V_{on}+V_{sat}$, worst than approach A.

V.I.II Bipolar Implementation

Since the transconductance of the BJT is directly proportional to the current, the complimentary input pair currents' sum must be constant for constant g_m sum. This restriction is less harsh than previously for CMOS. The topology of Figure 5.1.2 [11] encompasses the circuit implemented by [18] and an improvement for achieving lower voltages than $2V_{on}$. The basic theory is graphically demonstrated in Figure 5.1.2 (a). To get constant g_m a current subtracting technique is applied by a simple 1:1 mirror and Qb. By means of a nodal equation the following relation can be obtained,

$$I_{b1} = constant = I_p+I_n \qquad (5.1.2.1)$$

hence maintaining a constant g_m. The resistors and common mode dependent current sources, I_x, are used to decrease the supply voltage limit.

Suppose that V_{cc}-V_{ee} is 1V and V_{cm} (common mode) is at 0.5V, then neither the N nor the P type input pairs are on if the resistors and I_x were not there, V_{on}~0.6V. However, by placing I_x through the resistors the effective input voltage to the P type is below 0.5V by I_xR and the N type is above 0.5V by I_xR. If I_xR is greater than 0.1V then both pairs would be on. When V_{cm} is near either rail then I_x turns off and only one pair is on. The resulting condition is that the new power supply limit has now been reduced to below V_{onn}+V_{onp} by approximately $2I_xR$ while maintaining rail to rail operation with constant g_m. However, the ultimate limit is V_{on}+$2V_{sat}$, limited by the transistor stack of the simple current mirror, Qb, and current source I_b. The implementation of the common mode dependent I_x is illustrated in Figure 5.1.2 (b). When V_{cm} (V_{cmn} and V_{cmp}) is low, Qn1 is off thus I_x is 0. When V_{cm} is at midrange, Qn1 and Qp1 are both on thus I_x starts to reach its maximum value. Finally, when V_{cm} is high Qp1 is off thus I_x is again 0. This technique of decreasing the power supply voltage can also be applied to CMOS thereby achieving the ultimate power supply limit of V_{gs}+$2V_{ds}$, somewhat greater than the Bipolar version.

V.II Folding

The topology that yields the highest gain is that of generic Folded Cascode structures. This can be achieved in a number of different ways with respect to device choice and whether or not double to single ended conversion is done at the differential pair site, at the cascode site, or in a later stage. At the input pair site, double to single ended conversion is achieved by adding an extra transistor for the simple version and a mirror for the more complex, eliminating systematic offset voltage, Figure 5.2 (a) [2]. Only the two in phase signals are fed to the folding stage thereby creating the paths necessary to drive the two output transistors. The conversion can also be implemented at the folding stage as illustrated in Figure 5.2 (c) with Q1,2. The basic topology of the Folded Cascode is depicted in Figures 5.2 (b,c,d) and its performance will be studied generically from Figure 5.2 (b), the basic CMOS version [3].

The Folded Cascode input stage can be segmented into the input pair/pairs and the folding stage making it a two stage structure having a gain of [3,9]

$$A_v = G_{m1} R_{o1} G_{m2} R_{o2} \tag{5.2.1}$$

where 1 and 2 denote the corresponding stages. G_{m1} would simply be the transconductance of the differential input pair as calculated in section V.I. The impedance of the first stage is simply the parallel combination of the output impedance of the input pair, r_{ds1}, and R_{11} [Figure 5.2 (b)]. R_{11} is the impedance seen at the source of M3 and M4 which can be calculated to be

$$R_{11} = \frac{ro3 + Ro2}{1 + g_{m2}\, ro3} \sim \frac{ro3 + Ro2}{g_{m2}\, ro3} = \frac{1}{G_{m2}} \tag{5.2.2}$$

and substituting,

$$A_v = G_{m1} \frac{\dfrac{g_{m2} r_{o3}}{r_{o3} + R_{o2}}}{\dfrac{1}{r_{o1}} + \dfrac{1}{r_{odiff}} + \dfrac{g_{m2} r_{o3}}{r_{o3} + R_{o2}}} R_{o2} \tag{5.2.3}$$

The dominant and second pole are at the output and cascode nodes respectively,

$$P_1 = \frac{-1}{C_L \left\{ \left[g_{m3} r_{o3} (r_{odiff} // r_{o1}) \right] // \left[g_{m5} r_{o5} r_{o7} \right] \right\}} \tag{5.2.4}$$

and

$$P_2 = \frac{-g_{m3}}{C_{parasitic} + C_{f1}} \tag{5.2.5}$$

where $C_{parasitic}$ is the collection of all parasitic capacitances at the cascode node. The purpose of C_{f1} is to introduce a zero to cancel the second pole [8],

$$Z_1 = \frac{-g_{m3}}{C_{f1} + C_{bd3}} \tag{5.2.6}$$

where C_{bd3} is added presuming that the bulk terminal of M3 is connected to the source for bulk effect prevention. If C_{f1} is large enough, P_2 and Z_1 effectively cancel each other.

The input referred noise contribution of the cascoding elements M1,3,5,7 is calculated and denoted by E_n,

$$E_n^2 (G_{m1} R_{o1} G_{m2})^2 = \frac{E_{n3}^2 g_{m3}^2}{\left[1+g_{m3}(r_{o1}/\!/r_{odiff})\right]^2} + \frac{E_{n5}^2 g_{m5}^2}{\left[1+g_{m3} r_{o7}\right]^2} + E_{n7}^2 g_{m7}^2 + E_{n1}^2 g_{m1}^2 \quad (5.2.7)$$

Therefore, the dominant sources of noise in the folded cascode are M1 and M7 plus the contribution of the input pair, E_{ndiff}^2. A technique to minimize the noise would be to change M1 and M7 with resistors (done in [11]), Figure 5.2 (b), but this is at the expense of gain. A higher G_{m1} would then be required to keep the gain at a reasonable value.

Figure 5.2 illustrates different possible realizations of the folded cascode in the three pertinent technologies, CMOS, Bipolar, and BiCMOS. On the basis of equation (5.2.3) the gain is optimized if G_{m1} and R_{o2} are increased. This is best achieved by the Bipolar version, active elements in place of resistors [Figure 5.2 (c)]. R_{o2} can be increased by using a regulated cascode structure as discussed in section II.III. The GBW (G_{m1}/C_L) is optimized by increasing G_{m1} making the Bipolar version a better choice. Feed forward compensation may not be necessary in the Bipolar version since the second pole is further out. Furthermore, the MOS device yields a RHP zero that may be low enough in frequency to cause problems. If high gain and low noise are desired, the Bipolar version is best suited because of its inherent high g_m and low noise, section I.I. However, if current noise is more of a concern the CMOS is best. The technique of using resistors to minimize noise is best suited for the Bipolar circuit due to the innate g_m of the BJT. The low power supply limits lie in the differential stage as discussed in section V.I, Bipolar being better. All implementations include rail to rail input stages that yield good CMR. The input referred offset voltage is a function of the input pair and, as discussed in section III, the Bipolar version is better suited for the task. Finally, high input impedance is best achieved by an MOS input pair.

It is evident that BiCMOS yields the best performance for it can accomplish both CMOS and Bipolar versions plus further ameliorate certain specifications. For instance, if high input impedance and frequency response is to be optimized, the input pair would be CMOS and the folding stage would be as shown in Figure 5.2 (d), a spin off from [10,20]. This would maintain the high input impedance of MOS while moving P_2 further out (BJT dominated) hence decreasing C_L and increasing the GBW. Several other different combinations can be achieved for optimizing different

parameters such as noise, dc gain, etc. Table 5.1 summarizes the qualitative results derived in this section.

Qualitative Comparison	CMOS	Bipolar	BiCMOS
High Gain		X	X
High GBW		X	X
Ease of Compensation		X	X
Low Voltage Noise		X	X
Low Current Noise	X		X
Low Power Supply Limit		X	X
CMR	X	X	X
Low Voltage Offset		X	X
High Input Impedance	X		X

Table 5.1 Qualitative Comparison for Input Stages

VI. OUTPUT STAGES

The output stage of an Op Amp delivers a specified signal power to the output load with an acceptable level of distortion and frequency degradation. This stage should also be power efficient. Output stages are typically realized through the use of emitter/source followers yielding low output impedance and high current gain. However, at low voltages this is not a practical implementation since the output swing is seriously limited. For example, using an emitter follower in a 1V power supply would limit the signal swing to a V_{be} below the rail (~0.4V). It is because of this reason that a common source/emitter output stage is the recommended course of action [23]. Through this method a rail to rail output stage is achieved, a necessary condition [4]. Furthermore, a class AB output stage is best suited in a low voltage environment for optimized power efficiency and distortion performance [4,23]. Classical circuit techniques such as darlington configurations, transistor stacking (especially diode connected), and frivolous cascoding are greatly discouraged in low voltage [10]. Instead, stacking should not exceed $V_{on}+2V_{sat}$ (defined in Table 1.1) which yields a maximum of only one diode connected transistor per stack. Rail to rail operation is

essentially achieved by complimentary output devices in a common source/emitter configuration; thus, emphasis will be placed in the class AB control circuitry.

VI.I CMOS Output Stage

A. Current Sense: The intrinsic idea is to sense the output currents of the P and N type output transistors and feed a signal back to the ac path for AB control, Figure 6.1 (a) [1]. I_p and I_n are the sensed currents for the output transistors and easily achieved through mirrors. Nodes P and N are signals fed back to the ac path of the respective output transistors. To ensure class AB behavior, the current through the output transistors, when there is no current load, must be some non-zero value. This is achieved in Figure 6.1 (a) when everything is balanced, the voltage at nodes "a" and "b" are equal and "c" equals Vb1. When unbalanced, I_n or $I_p < I_{min}$, the circuit feeds back a signal to recuperate balance. The voltage at node "c" decreases which causes the voltage at N to increase and P to decrease corresponding to an increase and decrease to the output transistors' gate drive respectively. This effectively increases I_n and I_p until balance is achieved. The feedback acts in such a way so as to prevent the output transistors from ever turning off.

B. MTL: Figure 6.1 (b) shows a circuit achieving AB control through an MTL (MOS Translinear Loop) [2,15]. The loop is implemented with M1,2,3,4 and the fed back signal is achieved through the differential pair M5,6. The basic idea is the same as before, the output currents are sensed through mirrors and a feedback signal is generated ensuring a minimum current at the output. The loop implements the following equation

$$(I_n-0.5I_{min})^{0.5}+(I_p-0.5I_{min})^{0.5}=(I_n+I_p-I_{min})^{0.5}+(0.5I_{min})^{0.5} \qquad (6.1.1)$$

This equality ensures a non-zero minimum current through the output transistors, Figure 6.1 (c). The differential pair, M5,6, feeds back a signal to restore balance when equation (6.1.1) is not met.

VI.II Bipolar Output Stage

Another way of implementing class AB feedback control is through voltage feedback. This is implemented in Figure 6.2 through Qp2,3 and R2,3 [18]. The basic idea is to sum the base emitter voltages of the output transistors, compare them with a reference, and feed back a correction signal. The summation is done by reflecting V_{bep} on top of V_{ben}. Qp2 and R2 have V_{bep} across it from

the power supply to the base. Since Qp3 and R3 are replicas of Qp2 and R2 with equal current going through, the resulting voltage across R3 and V_{bep3} is V_{bep}. Hence, the voltage at node "a" is $V_{ben}+V_{bep}$ which is then compared to a reference voltage. By using the resistors, the current through Qp2,3 is a transcendental relation of the P type output current

$$V_t \ln\left[\frac{I_p\, A_{p2}}{I_{p2}\, A_p}\right] = I_{p2}\, R2 \quad \text{or} \quad I_p = \frac{I_{p2} A_p}{A_{p2}} \exp\left[\frac{I_{p2} R_2}{V_t}\right] \tag{6.2.1}$$

where A corresponds to the emitter area. This relation is important for power efficiency since I_{p2} will never be as large as the output current, I_p. This efficiency is similarly implemented in CMOS through source degenerating resistors, effectively degrading V_{gs}. However, the power supply of this topology is ultimately limited to $2V_{on}+V_{sat}$.

VI.III BiCMOS Output Stage

The class AB control circuitry can also be realized by a buffer amplifier, Figure 6.3 (modification of [14]). The output stage is a finite gain stage (Gain = 1+R2/R1) with quiescent output current control. When everything is balanced and there is no current load, equal current is flowing through Mp1 and Mp2. This current is then translated to their corresponding output transistors through transcendental current mirrors, equation (6.2.1), thereby ensuring a non-zero quiescent current along with push/pull behavior, class AB.

The current sense and buffer gain approaches for obtaining class AB control are the most conducive toward low voltage design. A technique like the multi-path can also be utilized to enhance the frequency response performance, as realized in [4,23] and discussed in section IV.II.. The MTL approach is not apparently translatable but a similar BJT translinear loop [25] can be formulated and realized. The basic advantages and disadvantages of the technology lies in the choice of active elements and summarized in Table 6.1. For instance, due to the wide range of current capability of the BJT, Bipolar technology is better suited for the implementation of the push/pull complementary output transistors. Moreover, the BJT is inherently faster hence making Bipolar technology well suited for speed performance. In terms of power supply reduction, Bipolar

has a slight advantage due to the V_{be} behavior for a wide range of currents and its inherent large gain. However, at high loads, a B offset voltage error arises in Bipolar circuits,

$$V_{os} = \frac{I_{o\max}}{B^{nstages} G_{m-input}} \tag{6.3.1}$$

where $G_{m\text{-}input}$ and nstages correspond to the input pair and the number of gain stages after it. This value can be significant at worst case B (~ 20 or 30) and high output current. BiCMOS can use, as in Figure 6.3, a MOS buffer to effectively reduce the effect of equation (6.3.1) to

$$V_{os} = \frac{I_{o\max}}{B\, G_{m-mos}\, A_n} \tag{6.3.2}$$

where A_n corresponds to the voltage gain of the previous stages. Here B per stage is replaced by a voltage gain per stage, which is typically larger, thereby reducing the effective offset voltage.

Qualitative Comparison	**CMOS**	**Bipolar**	**BiCMOS**
Wide Range of Currents		X	X
Low V_{offset} Due To I_{outmax}	X		X
Better Frequency Response		X	X
Low Power Supply Limit		X	X
High Input Impedance	X		X
High Gain		X	X

Table 6.1 Qualitative Comparison of Output Stages .

VII CONCLUSION

Design techniques for low voltage Op Amps have been investigated and developed. Conventional techniques for enhanced performance, such as frivolous cascoding, emitter/source followers, and darlington configurations, do not readily apply in a low voltage environment. The design convention is then limited to a V_{on} per transistor stack to minimize voltage drops. The ultimate limit would then be $V_{gs}+V_{dssat}$ and $V_{be}+V_{cesat}$ for CMOS and Bipolar respectively. Bipolar is better suited for ultimate supply voltage reduction due to its inherent lower voltage drops. The performance suffers when these limits are approached, namely gain (due to lack of cascoding

and degradation of output impedance) and bandwidth. Bandwidth is sacrificed because of increased junction capacitance (decreased reverse bias voltages) and reduced currents (degraded gate/base drive). Moreover, since the gain decreases more stages are needed which further degrades bandwidth. Dynamic range is also reduced by a decrease in signal swings which consequently places emphasis on low noise design and rail to rail operation.

The tools by which an amplifier is designed are current mirrors, differential pairs, and gain stages. Mirrors can be implemented with the simple, cascode, and regulated cascode circuits. The Bipolar technology yields the best frequency response and noise performance at the expense of current error, unlike CMOS. Except for input current error, the BJT provides the best input pair for it provides higher gain, lower noise, lower supply voltage limit, and low input offset voltage. A technique for optimally compensating a multi-stage Op Amp, the likely case in low voltage, was introduced and whose applicability extends to all three technologies. However, each time a gain stage is added the bandwidth is still degraded.

The most conducive architecture for low supply voltages is the folded topology. For optimum SNR the input and output signal swings must be rail to rail. This is coupled with constant g_m over CMR input stages and class AB output stages for power efficiency and low distortion. The Bipolar implementation of the constant g_m input stage (switched current) is simpler yielding a higher gain and better frequency response than the CMOS versions (switched current and MTL). The power supply is limited to $V_{on}+2V_{sat}$, optimally achieved by switched currents. With respect to folding, CMOS yields a higher R_{in} and lower RHP zero (creating compensating difficulties). Bipolar, on the other hand, achieves better frequency response, gain, and power supply reduction. The two conducive low voltage design strategies for class AB output stages involve sensing the output current and using a buffered stage. Sensing the output voltage drive is discouraged because it requires stacking two V_{on}'s.

The design methodology in low voltage design would start at device choice on through mirror and gain stage topology to their final implementations in input and output stages. The best performance is achieved by BiCMOS for it can combine the high input impedance of the MOSFET and the high gain, low noise nature of the BJT. The only drawback is its high cost. Over all,

BiCMOS is the best technology for the design of an Op Amp in all aspects except for money combining the benefits of Bipolar (lower noise, higher gain, higher GBW, easier compensation, lower power supply limit) and those of CMOS (higher input impedance, less power, less chip area, and zero offset analog switches).

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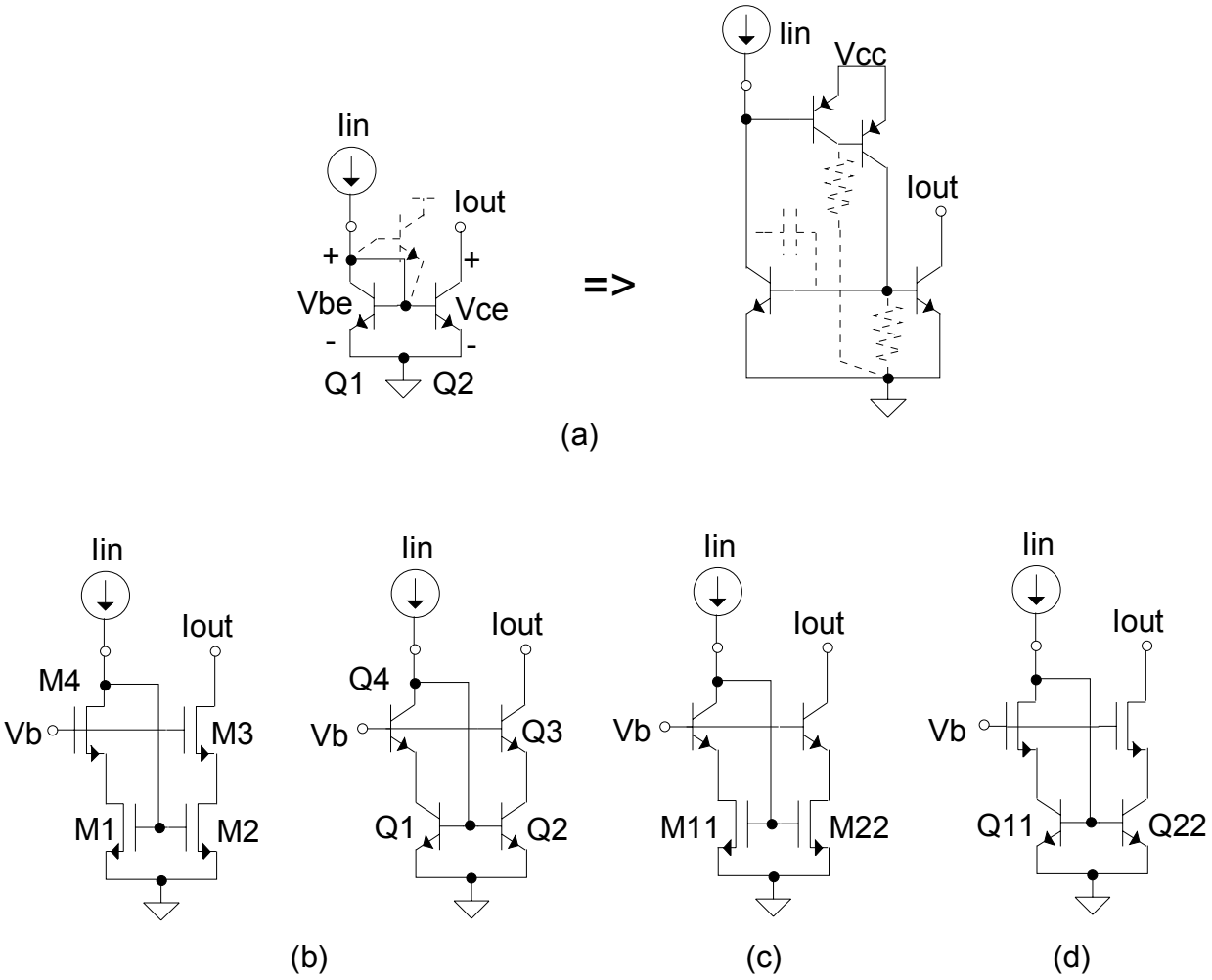


Figure 2.1 Simple and Cascode Current Mirrors

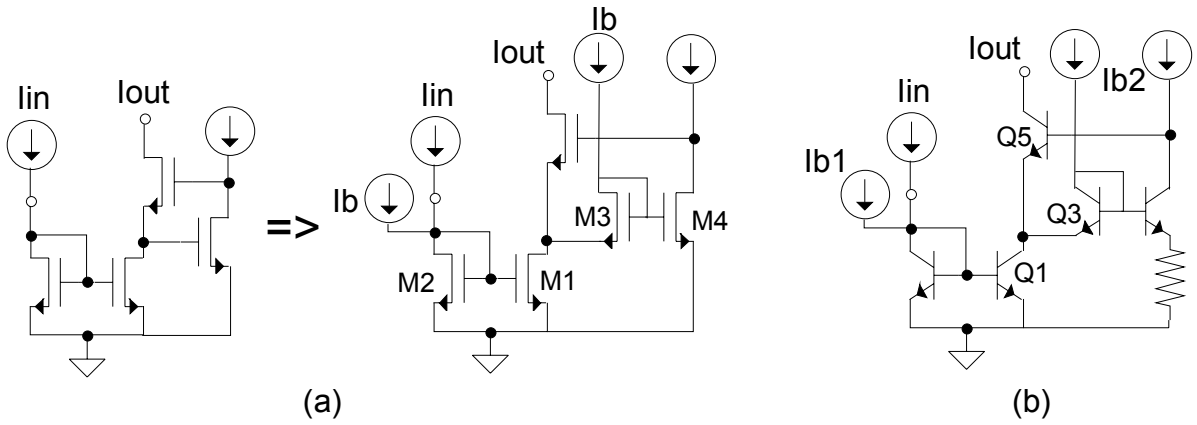


Figure 2.3 Regulated Cascode Current Mirrors

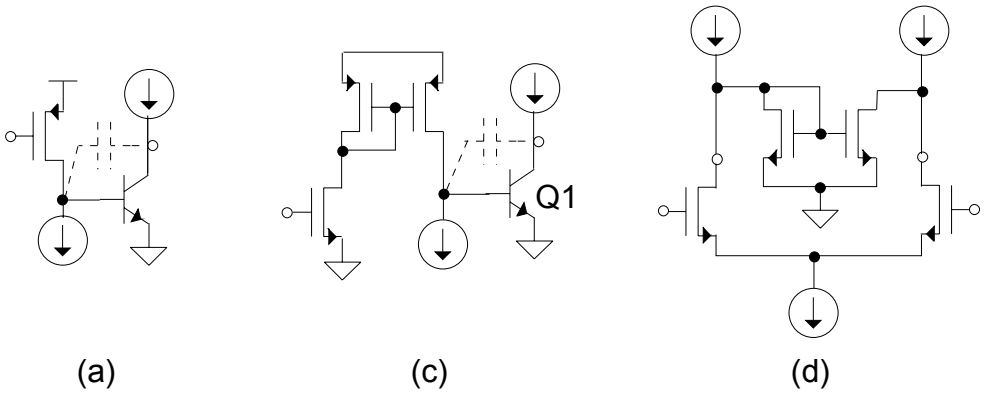


Figure 4.1 Gain Stages [10,13]

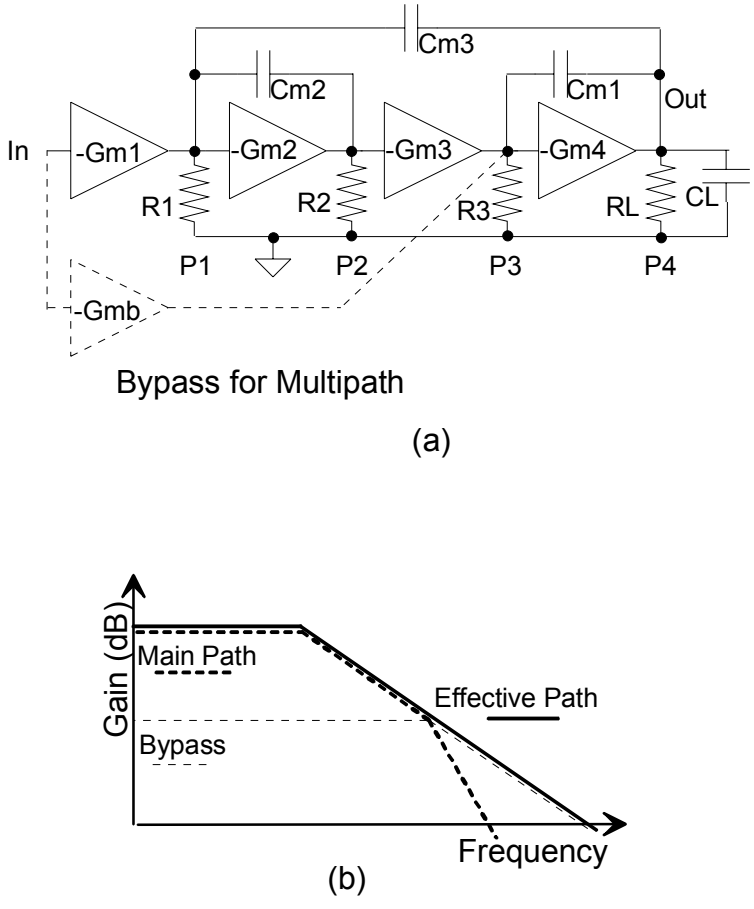


Figure 4.2 Multipath Hybrid Nested Miller Compensation

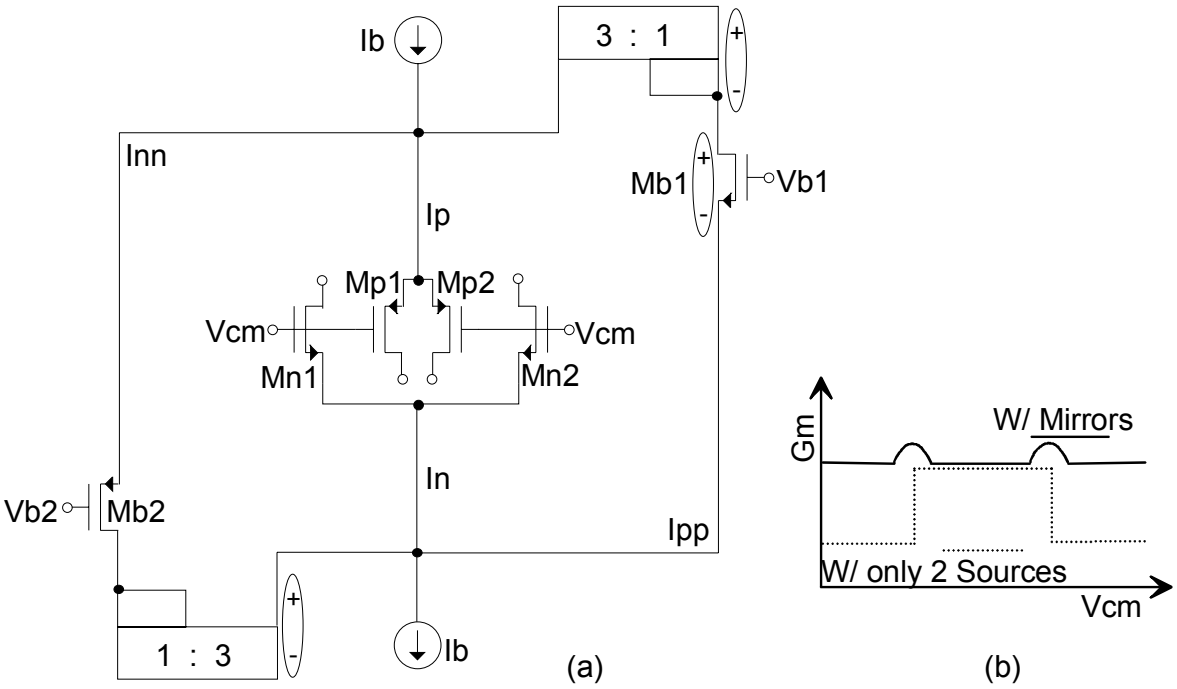


Figure 5.1.1.1 CMOS Constant Gm Input Stage using mirrors [1]

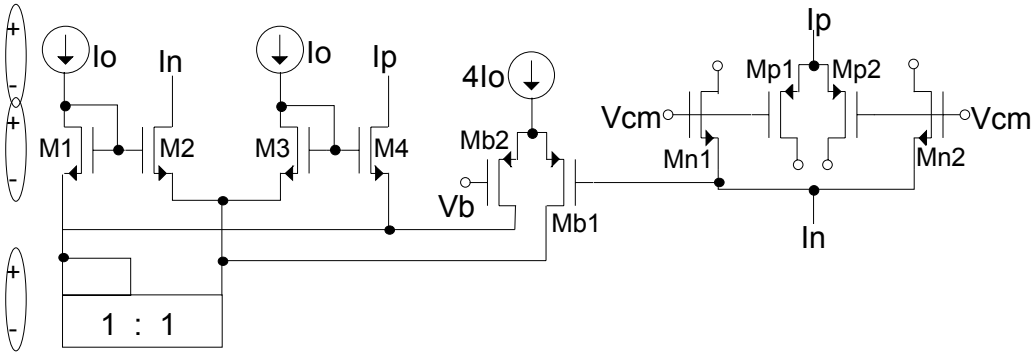


Figure 5.1.1.2 CMOS Constant Gm Input Stage using the MTL approach [2]

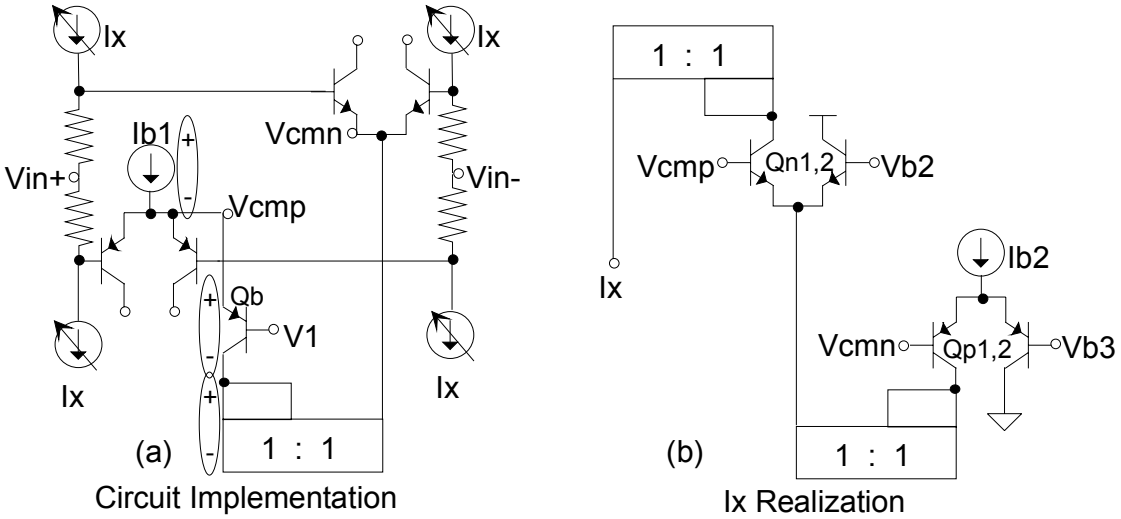
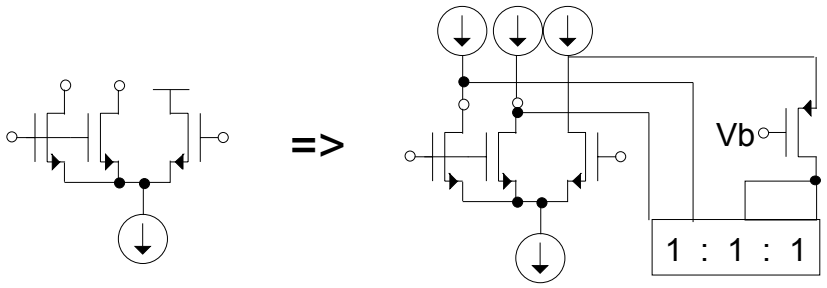
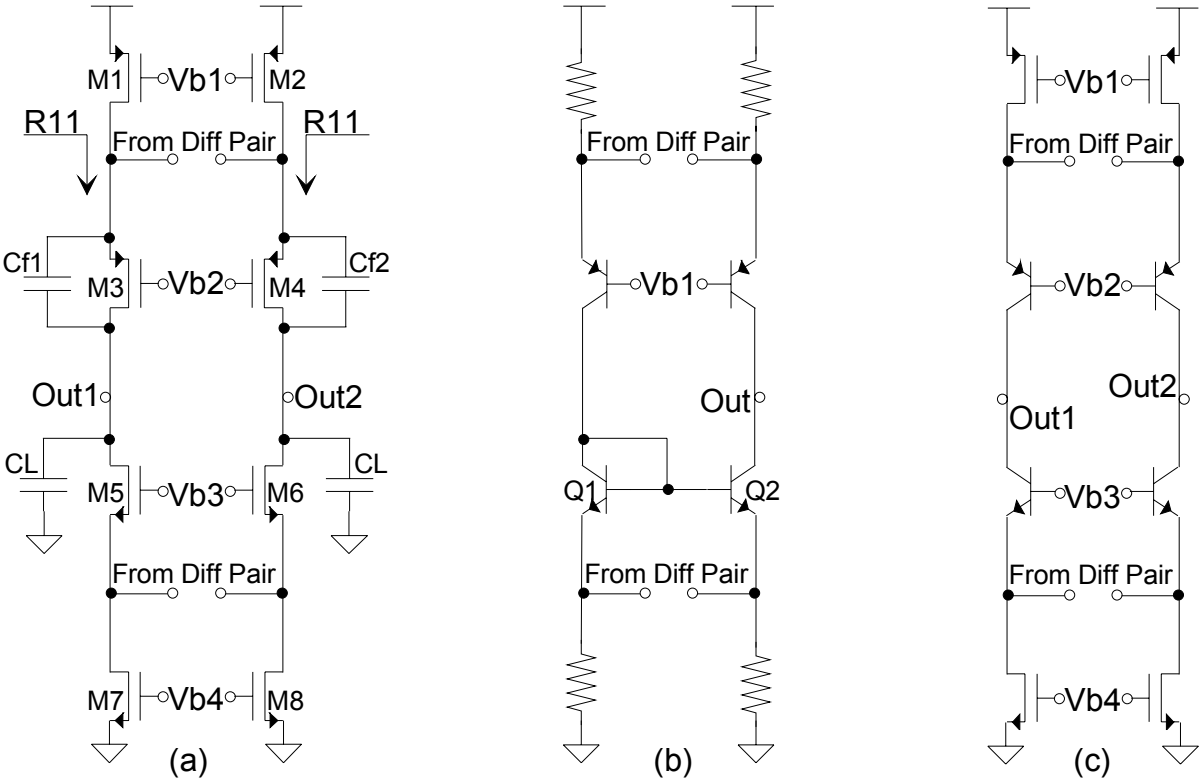


Figure 5.1.2 Bipolar Constant Gm Input Stage [11]



(a)



(b) (c) (d)

Figure 5.2 Input Stage - Folding Design [2,3,11]

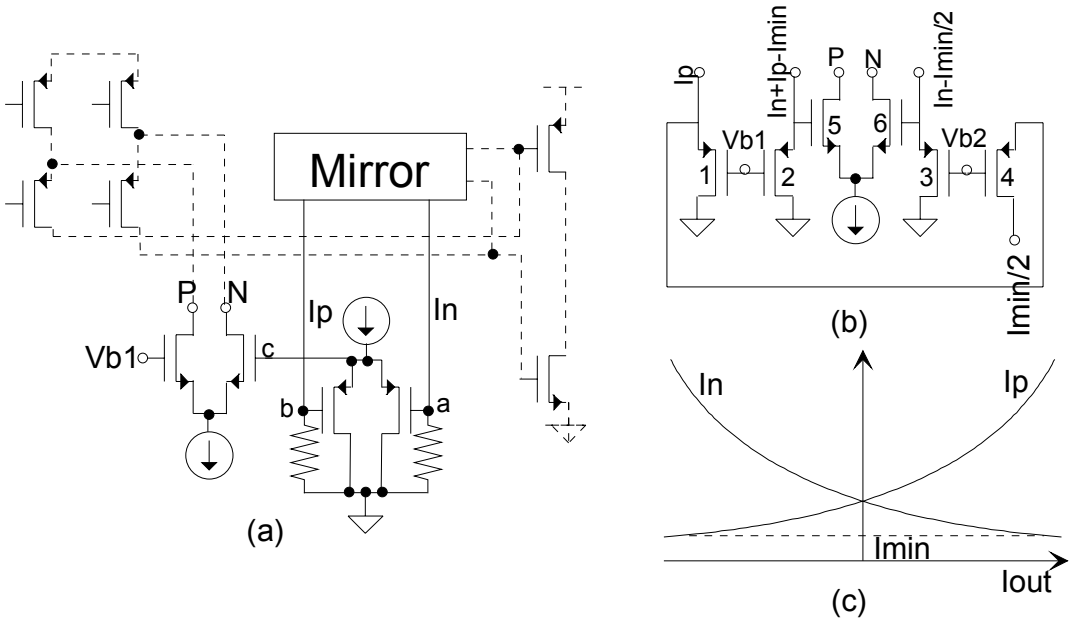


Figure 6.1 CMOS Class AB Control Circuitry [1,2]

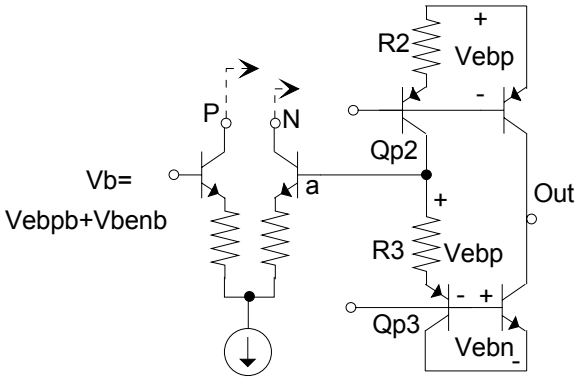


Figure 6.2 Bipolar Voltage Feedback Class AB Control Circuit [18]

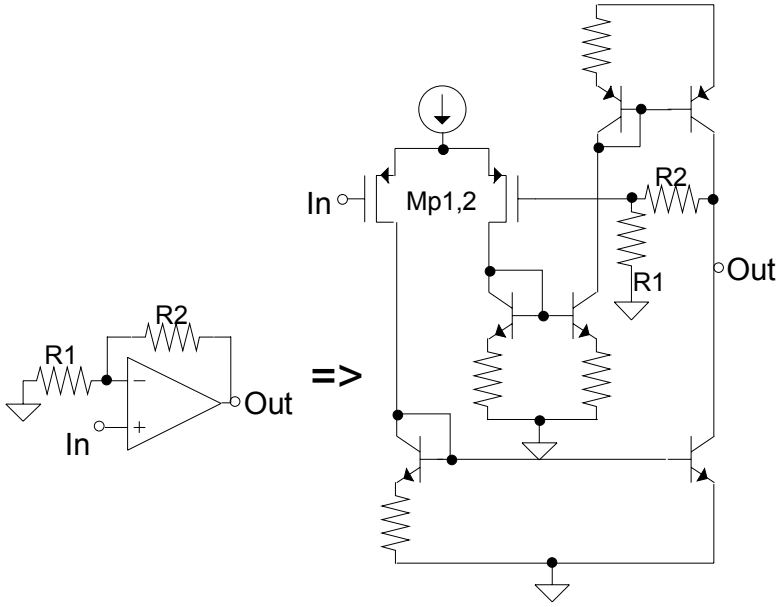


Figure 6.3 BiCMOS Class AB Buffer Output Stage