Li-Ion battery chargers -- not just another design

By Gabriel A. Rincón-Mora, Senior Member, IEEE, and Min Chen, Student Member, IEEE, The Georgia Tech Analog & Power IC Design Laboratory

The use of lithium-ion (Li-Ion) batteries in portable wireless electronics is a growing reality today. High energy density and long charge-discharge cycle life are two driving reasons for this, in addition to overcoming some of the shortcomings of previous technologies, like memory effects [1]. Typically, these batteries are charged to within ±1% of their full-charge voltage, for maximum capacity and long cycle life (that is, highest energy) [2], but overcharging them is destructive and therefore prohibitive. As a result, the charging process is often relatively slow and cumbersome, requiring the charger to monitor and carefully manage a winning tradeoff between reliability and capacity.

The Charging Process

The Li-Ion battery usually draws power from an AC wall outlet or existing DC supplies via a charger, which is nothing more than a combination of linear and switching regulator circuits, as generally shown in Fig. 1(a). For safety, efficiency, and long operational life, the charger must carefully traverse through a series of charging phases. First, it may have to pre-condition the battery, if for instance, the battery voltage is below its minimum rated value (for example, below 2.7 V); in which case, a low charging current is driven into the battery until it reaches an acceptable low charge voltage. Then, it enters the charging phase, sourcing a larger, well-regulated current. Both of these steps are realized with what amounts to a constant, but dependent, current-source charging circuit, as represented by IC in Fig. 1(b).

When the battery voltage nears the full- or end-of-charge voltage limit, the charging current decreases to whatever value is necessary to ensure the battery voltage reaches its targeted value. This is achieved by transitioning from a constant and dependent current source into a voltage-source circuit, as shown in Fig. 1(b), wherein, as the battery voltage approaches the targeted $V_{\text{Ref}}$, the charging current gradually decreases. Finally, when the charge current decreases below a pre-determined end-of-charge limit, the charging sequence stops and the charger is disengaged. This foregoing charging scheme is referred in literature as the constant-current to constant-voltage (CC-CV) technique [1].

![Diagram of Li-Ion charging scheme](http://www.powermanagementdesignline.com/showArticle.jhtml;jsessionid=K4LT3MRD... 5/18/2006)
Reaching the end-of-charge voltage target accurately (for maximum energy) and smoothly traversing between the various phases of the charging process are key features of the charger. In practice, interconnecting current and voltage feedback loops manage the entire charging process, giving rise to three operational regions: constant current, intermediate current-to-voltage, and constant voltage region. A benign interplay between these two feedback loops is critical for a safe and uninterrupted charge. Relatively complex digital and bootstrapped switching circuits are normally used for this purpose, both in academic and commercial circles [3-5], and the foregoing presentation addresses all these features in a relatively simple and effective form.

The charger

The basic mechanism through which any source is designed is feedback. Current loop I-Loop in Fig. 2, for instance, implements the current source because it senses and regulates charge current \( I_C \), which is another way of saying a series feedback loop exists around \( I_C \). Neglecting, for the time being, the effects of voltage loop V-Loop, in other words, assuming diode \( D_{SW} \) is off, the current is sensed by mirroring a fraction of charge current \( I_C \), which flows through PMOS transistor \( M_P \), into sense resistor \( R_S \) via mirroring device \( M_{PS} \). Amplifier \( A_{Mirror} \) ensures the drain-source voltages of \( M_P \) and \( M_{PS} \) are equal, thereby improving the mirroring quality of their respective currents. The end result is that the sense voltage across \( R_S \) is linearly proportional to charge current \( I_C \). Therefore, because of negative feedback, transconductor \( G_{mi} \) drives whatever gate-drive voltage is necessary to ensure sense voltage \( R_S I_C / 1,000 \) is equal to \( V_C \), to ensure charge current \( I_C \) is set to a controlled, pre-determined value.

In terms of stability, I-Loop contains two separate feedback loops, both of which must be stable. The first, the mirror loop, which is comprised of \( A_{Mirror} \) and the cascode PFET, is self-compensating because there is only one dominant high impedance pole and that is inside amplifier \( A_{Mirror} \) at the gain-setting node. Pulling the location of this pole to lower frequencies improves the phase- and gain-margin performance of this loop, but this would be at the cost of bandwidth. Since the other current-regulating loop is dependent on this mirror loop to sense charge current \( I_C \), the mirror bandwidth must be relatively high, which is why \( A_{Mirror} \) is designed to have a relatively high bandwidth.

The current-regulating loop is comprised of transconductor \( G_{mi} \) mirroring PMOS devices \( M_P \) and \( M_{PS} \), the mirror loop, and \( R_S \). As just mentioned, the mirror loop's bandwidth is high and the pole associated with the drain of \( M_{PS} \) is consequently located at high frequencies, leaving only two other poles, one across resistor \( R_S \) and another one at the gates of \( M_P \) and \( M_{PS} \). Between these latter two poles, the highest impedance is at the gates of \( M_P \) and \( M_{PS} \), since the

Figure 2. Compact Li-Ion charger circuit
impedance across $R_S$ is designed to be significantly lower than $G_{mi}$'s output impedance, which means the gates of $M_P$ and $M_{PS}$ introduce the dominant, compensating low frequency pole ($p_{\text{Gate}}$) of the current-regulating loop. Since all other poles are beyond the unity-gain frequency, the phase-margin is 90°, as shown in Fig. 3(a). DC loop-gain $LGI$ is the gain across transconductor $G_{mi}$ and common-source stage $M_{PS}$ (gate of $M_{PS}$ to $R_S$), that is to say,

$$LGI \propto -s_{ME} R_S \left[ 1 \parallel \left( \frac{1}{sC_g} \right) \right] = \frac{-K_I}{1+sC_g(R_o \parallel R_D)}$$  \hspace{1cm} (1)$$

where $C_g$ is the total parasitic capacitance present at the gates of $M_P$ and $M_{PS}$, $R_0$ is $G_{mi}$’s output resistance, and $K_I$ is the combined DC gain of $LG_I$.

**Figure 3. Simulated Bode plot response of the charger as it traverses through the various operational regions**

Voltage loop V-Loop in Figure 2 implements the voltage source because, unlike the current source, it senses and regulates the battery voltage through shunt feedback. Again, neglecting the effects of the current loop by assuming its loop gain is relatively low, the voltage loop is comprised of operational amplifier $A_v$, charging device $M_P$, and the battery, the latter of which is low impedance, by definition. Basically, because of shunt feedback, $A_v$ drives whatever gate-drive $M_P$ requires to source just enough current to charge the battery to $V_{Ref}$. With regard to frequency response, outside of the high frequency pole across the battery, there are two poles in this loop, at the gate of $M_P$ and inside the op-amp, the latter of which is dominant, as shown in Fig. 3(c), because the output of $A_v$ is designed to have low impedance (for
example, emitter or source follower). The loop gain of this loop (LGV) is the voltage gain across AV, common-source gain stage MP, and voltage divider comprised of diode DSW and the impedance at the gates of MP and MPS (i.e., $R_o \parallel 1/sC_g$), or

$$LGV = \frac{K_V}{1 + sC_g (R_o \parallel R_D)}$$

where $R_{Bat}$ and $R_D$ are the ac-resistances across the battery and diodes DSW. $pAV$ is the internal pole of op-amp AV, and $K_V$ is the combined DC gain of the loop.

Diode DSW is the key analog-mixing device in this circuit because it determines which loop is active and dominant. If $V_{Bat}$ is well below $V_{Ref}$ at the beginning of the charging process, AV attempts to sink current but diode DSW prevents it, allowing the current loop to dominate (that is, DSW is off). When $V_{Bat}$ nears $V_{Ref}$, AV attempts to decrease MP's gate-drive by sourcing current into the gate through DSW, slowly decreasing the impedance at the gate from $R_o$ to $R_{AV} + R_D$, in the process decreasing the gain and increasing the bandwidth of the current loop. As a result, the voltage loop dominates the charging process, because LGV increases, now that DSW starts to close the voltage feedback loop. The overlap of these two responses effectively introduces a left-hand plane (LHP) zero into the $p_{Gate}-p_{AV}$ mix, as illustrated in Fig. 3(b).

The combined loop gain of the circuit is determined by “breaking” the loop at the gates of MP and MPS, which results in two parallel feedback paths, LGI and LGV, and whose total loop gain LG is simply their sum. When plotted in dB (that is, logarithmic scale), the sum of LGI and LGV is approximately the maximum of the two (that is, $LG \approx \text{Max}(LG_I, LG_V)$), as shown by the solid, dotted, and dashed traces in Figure 3. Consequently, assuming $R_{AV}$ and $R_o$ are low and high, respectively, the combined open-loop gain is

$$LG = LG_I + LG_V \approx \left[ \frac{K_I + K_V}{1 + sC_g (R_o \parallel R_D)} \right] \left[ 1 + \frac{sK_I}{(K_I + K_V) p_{AV}} \right]$$

As $R_D$ changes from infinity (DSW is off) to a negligibly small value (DSW is on) and therefore gain $K_V$ increases from zero to a relatively high value, the LHP zero moves from $p_{AV}$ to infinity and $p_{Gate}$ also shifts to infinity, leaving behind $p_{AV}$. This pole-zero-pole staircase yields 90° of phase margin, which guarantees stability throughout the transition.

Charging the battery

Figure 4 illustrates the charging performance of a prototype circuit of the foregoing topology on an 850 mAh Li-Ion battery. The constant charge current, end-of-charge voltage, and end-of-charge current were 850 mA, 4.2 V, and 10 mA, respectively. The current-to-voltage transition, which is best shown in Figure 4b, is smooth and stable, slowly increasing the battery voltage from 4.206 to 4.207 V while gradually decreasing the charge current from 850 to 10 mA. The 5 to 7 mV end-of-charge error voltage is the result of line and load regulation, loop-gain error, and tolerance (for example, reference and input-referred offset performance of feedback error amplifier AV). In all, however, the compact prototype circuit is accurate and robust (that is, reliably stable).
Efficiency

Charging efficiency is of course another important parameter. When considering the power path, that is to say, the charge PMOS transistor connected from input supply \( V_{DD} \) to the battery, the efficiency performance of the circuit is similar to that of a low dropout regulator: linearly dependent on battery voltage \( V_{Bat} \) and input supply \( V_{DD} \).

\[
\eta = \frac{P_{Out}}{P_{In}} = \frac{I_C V_{Bat}}{I_C V_{DD}} = \frac{V_{Bat}}{V_{DD}} \quad (4)
\]

where the quiescent current flowing through the rest of the circuit is assumed to be much lower than charge current \( I_C \).

In practice, most charging applications derive power from a seemingly endless supply, a wall outlet, which de-rates the importance of efficiency performance. This scenario, however, is quickly changing in the advent of portable electronics, where batteries now charge other batteries. A laptop, for instance, can now be used to charge a cellular phone through its USB port. Similarly, an emergency battery pack can be used to bootstrap a PDA or another hand-held device. More importantly, in going forward, it is important to realize high energy density technologies, like fuel cells and nuclear batteries, cannot supply the high power densities Li-Ion and ultra-capacitors can. Small, hybrid, energy-exchanging sources are therefore emerging as increasingly appealing alternatives, demanding the charging efficiencies that most of today’s solutions are incapable of achieving, which is currently on-going research work.

For additional details, questions, and/or comments on this article, please contact us, the Georgia Tech Analog and Power IC Design Laboratory, at gtap@ece.gatech.edu. More information about our research can be found at http://www.rincon-mora.com/research.

References:
[5] Charger ICs: LM3621 (National Semiconductor), ADP3806 and ADP3820 (Analog Devices), BQ2057 (Texas Instruments), and LTC4054L (Linear Technology).