HOW-TO : Power Supplies

Inside the Belly of the Beast: A Map for the Wary Bandgap Reference Designer when Confronting Process Variations

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"Fast is fine, but accuracy is everything," said Wyatt Earp, famous lawman and prospector of the West. While the statement may have referred to his skill with a gun or his search for gold, it particularly rings true for design of integrated reference circuits. Whether used in an A/D converter to establish a standard to compare voltages against, or in an operational amplifier to set up a bias condition, or with a linear regulator to build a voltage source, the accuracy of the reference, across process, temperature, and supply voltages, directly influences and often dictates the overall performance of a system.

The bandgap reference circuit has been the most elegant way to fashion an integrated circuit reference. A "bandgap" produces a voltage that is temperature independent by adding a voltage that increases with temperature, i.e., has proportional-to-absolute-temperature or PTAT dependence, to a voltage that decreases linearly with temperature, i.e., has complementary-to-absolute-temperature or CTAT dependence, as shown in Figure 1. The generation of CTAT voltage V_{CTAT} is simply obtained by tapping the forward-biased base-emitter junction of a bipolar transistor. PTAT voltage V_{PTAT} is generated by using the difference in the base-emitter voltages of two bipolar transistors, one of which is larger than the other but both carrying the same total current, a manifestation of the well-known Gilbert principle.

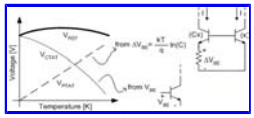

Figure 1. Temperature behavior of a typical bandgap reference circuit

Most bandgap references are based on the circuit presented in the classical paper by Brokaw in 1974 [1]. A simple example of such an implementation is shown in Figure 2(a), where a current mirror is used to force currents into a pair of bipolar transistors and whose base-emitter voltage difference is used to establish a ΔV_{BE} and consequently a PTAT voltage. Since standard digital CMOS processes often lack the vertical n-p-n bipolar transistors required by the Brokaw topology, they use available p-n-p substrate devices in diode configuration in place of the n-p-n transistors, and an op-amp to implement the current-mirror function, as shown in Figure 2(b) [2].

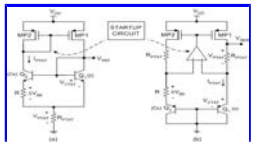

Figure 2. Simplified schematics of (a) a conventional Brokaw and (b) a CMOS bandgap reference circuit

While a number of effective design techniques have been developed to protect the reference voltage from variations in supply [3-4] and temperature [5-6], the approach to combating process variations is at times somewhat passive, in other words, tackle mismatch and process-induced variations through careful, but conventional layout techniques and ultimately use brute-force trimming to meet the dreaded "spec." As market demand for better accuracy rises, however, blindly increasing the number of trim bits requires more silicon area, increased test times, and possibly higher manufacturing costs, and still not meet the accuracy desired.

Therefore, even though the importance of judicious layout cannot be overstated nor the effectiveness of trimming denied, a designer is encouraged to (a) quantify process-induced errors to gauge the number of trim bits he shall require and (b) explore alternate strategies for obtaining high accuracy and minimizing his dependence on expensive trimming solutions.

So, which accuracy-degrading error sources warrant attention? Where do they originate and how can a circuit designer address them? Let us start with the basic foundation of a bandgap voltage reference, the expression of which is derived from Figs. 2(a) and 2(b) and is as follows:

$$V_{REF} = V_{CTAT} + V_{PTAT} = V_{BE1} + \frac{\Delta V_{BE}}{R} R_{PTAT} = V_{BE1} + V_T \ln(C) \frac{R_{PTAT}}{R} \quad \text{.....} \quad (1)$$

where ΔV_{BE} is the difference in the base-emitter voltages of Q_1 and Q_2 and C is the ratio of their emitter areas. Any process variation that produces a deviation in either the PTAT or CTAT component of the reference voltage given by (1) degrades the accuracy of the "bandgap" -- a quantitative analysis of these error sources is found in [7].

Errors Affecting V_{PTAT}

Operational Amplifier Offset
An offset at the input of the op-amp in Figure 2(b) is superimposed onto resistor R_{PTAT}, in addition to the desired ΔV_{BE}, and is therefore amplified by the same factor: R_{PTAT}/R. Typical values of this ratio lie in the range of 8-10, and consequently an offset of even ±1 mV produces a spread of 20 mV at the output of the reference, a 1.7% degradation, which makes the op-amp offset the dominant source of process-induced error in CMOS bandgap references. Since MOS devices are typically used in the input differential pair of these CMOS op-amps, the inherent random offset in their gate-source voltages, typically the result of mismatches in threshold voltages, W/L ratios, electron and hole mobilities, etc., has non-linear temperature dependence and cannot be easily trimmed as a result. The effects of these offsets on reference accuracy can, however, be significantly reduced through switching techniques, like chopper stabilization and dynamic-element matching (DEM) [8-9], but at the cost of complexity and switching noise.

Current-mirror Mismatch
Current-mirror errors arise from a mismatch in the MOS devices in the mirror, MP1 and MP2 in Figures 2(a) and 2(b), and manifest themselves in the reference as a difference in the current flowing through the two critical bipolar devices of the bandgap reference circuit, Q_1 and Q_2. This is one of the largest error sources in the Brokaw cell. The effects of this error can be reduced through layout by employing techniques such as common-centroid layout, dummy devices, cross-coupling, etc., and when warranted, trimming. A DEM [8] strategy virtually eliminates the effect of mismatch in the MOS devices, but at the cost of switching noise, which is a significant drawback, especially in high performance, densely integrated solutions.

Resistor Mismatch
Also obvious from (1), any deviation in the desired ratio of R_{PTAT} and R, in other words, any mismatch between these resistors, degrades accuracy performance. The impact of this error source, however, is very small since resistors can be matched to within 1% with careful layout. Since electric fields and temperature variations across the die may also affect the two resistors differently, choosing a material that exhibits a low voltage and temperature coefficient, such as poly-silicon film, as opposed to n-well diffusion, also helps to reduce this source of error. Since the error has a linear temperature coefficient, trimming is an effective method to compensate for their mismatch.

Bipolar Mismatch
Bipolar transistor mismatches result from a current-density mismatch in the two critical bipolar devices and originates from a difference in their reverse saturation currents and fabricated emitter areas. Like resistors, the effect of mismatch in the bipolar devices can be reduced through careful layout and trimming.

Errors Affecting V_{CTAT}

V_{BE} spread
The base-emitter voltage of the Q_1 in Figures 2(a) and 2(b), which is approximately between 0.6V and 0.7V, typically accounts for nearly half the bandgap reference voltage output of 1.2V. Any variation in this base-emitter voltage has therefore a direct impact on the accuracy of the reference. This variation is mostly due to the variation of the reverse-saturation current across process, from die to die and wafer to wafer. Given a typical 3-σ spread of approximately ±12 mV, this error source can produce a total error of 2% in the reference voltage. Though this effect is large, it can be significantly mitigated by conventional trimming techniques.

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Errors Affecting V_{PTAT} and V_{CTAT}

Package Shift
Package shift is the package-induced offset of the reference voltage relative to its original, unpackaged value. This shift is caused by stresses imposed by the package on the die surface. These stresses affect the bandgap reference voltage by effectively changing the value of the base-emitter voltage of the bipolar transistor, a phenomenon otherwise known as piezo-junction effect. The dominant component of these stresses is systematic and arises from a difference in the thermal coefficient of expansion (TCE) of the silicon die and the plastic package in which it is encapsulated. As the plastic and silicon cool down from roughly 175°C, the two materials contract at different rates, producing lateral thermo-mechanical stresses on the die surface.

The second component of the stress is due to the presence of filler particles suspended randomly in the plastic package. Ironically, these are added to reduce the difference in the TCE of the die and package, and therefore prevent the die from cracking, that is, the fillers increase reliability. As the die and plastic cool, however, these filler particles exert vertical stresses on the die surface, thereby affecting the base-emitter voltage of the bipolar transistors. Since these particles have a random distribution in shape, size, and location, the stresses they produce not only vary from die to die but also from one location to another on the die. Moreover, since this random variation is a post-package phenomenon, it cannot be trimmed by conventional wafer-level techniques. This shift can be mitigated, however, by introducing a mechanically compliant layer between the package and die surface to absorb the die stresses [10], but that is usually a costly proposition.

In summary, as illustrated in Table 1, although V_{BE} spread and current-mirror mismatch are large sources of error, they have linear temperature dependence and can, in the absence of other strategies, be trimmed. However, op-amp offsets not only have a large 3-σ errors but also non-linear temperature coefficients, which make them difficult to trim. Package shift, though not the largest contributor to the overall inaccuracy of a bandgap reference, is an important source of error because it results after the device is packaged, requiring exotic packaging solutions and/or post-package trimming techniques. These two latter errors may, in the end, warrant the use of dynamic-element matching (DEM) techniques and the switching noise they incur, but that will be up to the designer to decide.

In our laboratory, we are currently investigating how to attenuate these package-induced errors without resorting to post-trimming, exotic packaging, or DEM solutions. Our approach is to look at device-level and "smart" circuit-level solutions, in other words, design circuits that learn and adapt to their process. We are still in the process of evaluating plausible avenues.

ERROR Source		**ITS IMPACT**			**HOW CAN A DESIGNER FIGHT IT?**			
Origin	**3-σ value**	**How much?**	**On V_{PTAT}**	**On V_{CTAT}**	**Layout**	**Trimming**	**Dynamic Element Matching**	**Packaging**
Op amp offset	±5 mV	Very Large	Yes	No	Yes	No	Yes	No
Package Shift	±7 mV	Large	Yes	Yes	No	No	No	Yes
V_{BE} Spread	±24 mV	Very Large	No	Yes	No	Yes	No	No
Current mirror mismatch	±5%	Large	Yes	No	Yes	Yes	Yes	No
Resistor mismatch	±1%	Large	Yes	No	Yes	Yes	Yes	No
Transistor mismatch	&plusmn1%	Small	Yes	No	Yes	Yes	Yes	No
Resistor Tolerance	&plusmn20%	Small	Yes	No	No	Yes	No	No

Table 1. Various sources of error in bandgap reference circuits

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