Fast Energy-Harvesting TEG-Supplied Charging Regulator Microsystem

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***Abstract*—This paper presents a fast hysteretic switched-inductor charging regulator (SLCR) microsystem. It is powered by on-chip thermoelectric generators (TEGs) to supply Internet-of-Things (IoT) wireless microsensors. On-chip TEGs are appealing because they are 12–1400× smaller than off-chip ones. IoT sensors mostly idle in low-power mode and transmit data wirelessly only in high-power mode on demand. This requires CMOS SLCRs to respond quickly to abrupt load dumps caused by IoT sensors. State-of-the-art (SoA) SLCRs respond to load dumps in 100 µs–2.5 ms. This time duration amounts to a significant portion of the IoT sensor's data transmission time (500 µs–7 ms). This slow response time jeopardizes the quality of data transmission. This paper presents a fast hysteretic control that responds in 9.6 µs. This control adopts nested hysteretic architecture and requires only three comparators and simple combinational logics, which is appealing, considering the low power budget limited by on-chip TEGs. Moreover, this paper contributes detailed stability analysis, derives response time and accuracy and provides intuitive and accurate system design equations. Measured results of a 180-nm CMOS prototype validate that the proposed system shortens response time by 10–260× compared to the SoA.**

***Keywords*—Switched inductor, charging regulator, fast, response time, stability, design, energy harvesting, thermoelectric, CMOS.**

I. Powering IoT Microsensors with CMOS TEGs

Internet-of-Things (IoT) wireless microsensors can save money, energy, and lives [1]. Because of volume constraints, tiny IoT sensors usually carry small onboard batteries. These tiny batteries carry limited energy and shorten IoT sensors' lifetimes. Recharging batteries manually is labor intensive since these sensors are usually deployed at hard-to-reach locations. One possible solution is harvesting thermal energy to supply IoT sensors [2]. A thermoelectric generator (TEG) converts thermal gradients to electricity, which can be used to supply IoT sensors.

Typical TEGs are made of bismuth telluride or lead telluride (Bi-/Pb-Te), which are difficult to integrate on chip. Thus, typical TEGs are off chip and bulky, occupying 9–42 cm^2 [3–6]. Because an IoT sensor can be as tiny as 1.5 mm^3 [7], using bulky centimeter-scale off-chip TEGs to power such tiny sensors is unacceptable.

State-of-the-art (SoA) TEGs can be integrated on chip using micro-electro-mechanical systems (MEMS) technology. On-chip TEGs are made of Si, poly-Si, or poly-SiGe, using CMOS or BiCMOS processes and MEMS post-processing [8–11]. They occupy 3–70 mm^2, which is 12–1400× smaller than off-chip ones.

Unfortunately, the internal source resistance R_S of on-chip TEGs (shown in Fig. 1) is much higher than that of off-chip TEGs. On-chip TEG's R_S can be 0.7–1.3 MΩ [8–11], whereas off-chip TEGs' R_S is 0.16-4 Ω [3–6]. This high R_S limits on-chip TEG's maximum available power P_{MPP} to 1.8–17 nW/°C^2 [8–11], which is 3300–22000× lower than that of off-chip ones. Table I compares on-chip and off-chip TEGs. v_S is the open-circuit source voltage provided by the TEG.

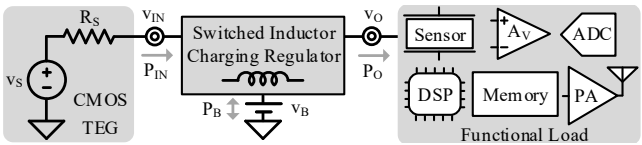

Fig. 1. A CMOS-TEG sourced microsystem.

While IoT sensors consume nanowatts (nW) [1] when sensing, they burn milliwatts (mW) [12] during data transmission [13–14]. Thus, when sensors idle, the CMOS switched inductor charging regulator (SLCR) in Fig. 1 draws input power P_{IN} from the TEG and directs a fraction of P_{IN} to supply load power P_O. The SLCR charges battery v_B with the remaining fraction of P_{IN} to store this extra energy. When the sensor demands higher power during data transmission, the SLCR draws battery power P_B from v_B to supply the load. This load profile requires the SLCR to respond quickly to load dumps to secure proper sensor function.

Table I: Comparison of On-Chip and Off-Chip TEGs

Material	Size [mm^2]	On-Chip	v_S [mV/°C]	R_S [Ω]	P_{MPP} [W/°C^2]	Ref.
Bi-Te	29 × 29	OFF	30	4.0	56 µ	[3]
Bi-Sb-Te	63 × 63	OFF	15	160 m	350 µ	[4]
Bi-Te	61 × 71	OFF	40	1.0	400 µ	[5]
PbTe-BiTe	56 × 56	OFF	28	970 m	210 µ	[6]
Poly-Si	3 × 3	ON	160	1.3 M	4.9 n	[8]
Poly-Si	3 × 1	ON	150	700 k	8.0 n	[9]
Si	11 × 1.5	ON	250	900 k	17 n	[10]
Poly-SiGe	*14 × 5	ON	74	760 k	1.8 n	[11]

* Estimates.

Previous studies in [16–20] rarely report load dump responses. For those that do, reported response time t_R is 100 µs–2.5 ms [21–24]. This slow t_R amounts to a significant fraction of the duration of data transmission (0.5–7 ms [13–14]) and may jeopardize data quality. Moreover, prior arts rarely analyze control stability.

Thus, this paper presents a fast hysteretic SLCR microsystem achieving 9.6 µs t_R. With detailed theory, this paper analyzes control stability, derives t_R and accuracy, and provides closed-form design equations. Moreover, in catering to the high R_S and low P_{MPP} of on-chip TEGs, this control employs only three comparators and combinational logics. This implies lower controller power for on-chip implementations. Contributions of this paper include the following:

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1) A fast hysteretic SLCR microsystem with 9.6-µs t_R.
2) Stability, t_R, and accuracy analysis with design equations.
3) Extensive measurements verifying theory, design expressions, and transient performance.

Section II introduces the SLCR system and analyzes stability and t_R. Sections III and IV derive system design equations and present measured performances. Section V concludes this paper.

II. Proposed Battery-Charging Voltage Regulator

The proposed CMOS SLCR system is shown in Fig. 2. When the on-chip TEG's P_{MPP} exceeds the demand of the IoT load (i.e., sensor idles), this SLCR is in harvest mode. In harvest mode, M_I always closes, and M_{GB} closes to energize L_X from v_{IN}. Output hysteretic comparator CP_O dictates whether L_X's energy is drained into output v_O or v_B. When v_O drops to CP_O's lower hysteretic trip point $v_{H(O–)}$, CP_O trips low. Then, every time L_X drains, switching logic closes M_{OB} to supply v_O, so v_O rises. When v_O rises to CP_O's upper hysteretic trip point $v_{H(O+)}$, CP_O trips high. Then, every time L_X drains, switching logic closes M_B to charge v_B. This way, CP_O limits v_O within its hysteretic window $\Delta v_{H(O)}$ and charges v_B with excess available power.

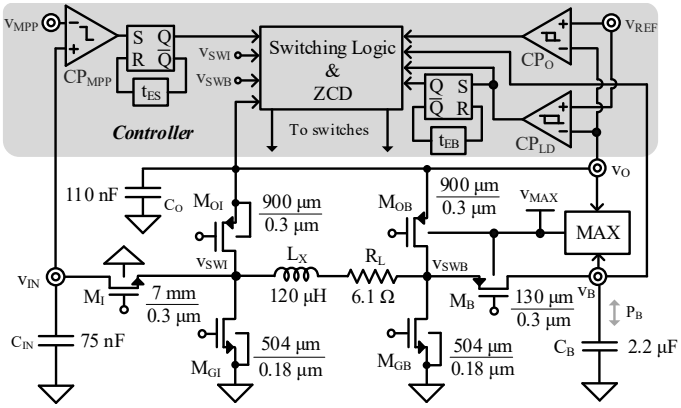

Fig. 2. A CMOS switched-inductor charging regulator system.

If the IoT load demands a power higher than P_{MPP}, v_O will drop below $v_{H(O–)}$. When v_O hits the load-dump hysteretic comparator CP_{LD}'s lower trip point $v_{H(LD–)}$, CP_{LD} trips low, and the SLCR enters battery-assist mode. In this mode, M_I always opens, and L_X, M_B, M_{GB}, M_{GI}, and M_{OI} buck or boost v_B to v_O. The maximum voltage selector (the "MAX" block in Fig. 2) outputs the higher voltage between v_O and v_B, which is called v_{MAX}. Its schematic is shown in Fig. 3 [25]. When v_O is lower than v_B, switch M_{VB} closes to short v_B to v_{MAX}, and vice versa.

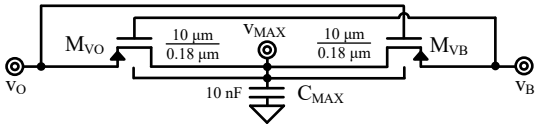

Fig. 3. Schematic of the maximum-supply selector.

SLCR is in discontinuous conduction mode (DCM) and adopts the constant-energy-packet scheme described in [25], which fixes the peak inductor current by fixing the energizing time under given v_{IN}. The constant energy packet scheme keeps each energy packet the same and only adjusts the duration of energy delivery to adjust the power delivered (i.e., in Fig. 12 the harvester delivers energy for 260 ms each time with 20 nA load, whereas it delivers energy for 830 ms each time with 40 nA load). Thus, its efficiency stays optimally flat across power level and is the same as the efficiency of each energy packet. Fixing the energizing time eliminates the need for an inner current loop. All energy packets E_S drawn from v_{IN} are identical in harvest mode (i.e., identical harvest-mode peak current $i_{L(S.PK)}$, as in Fig. 4). In battery-assist mode, all energy packets that E_B draws from v_B are also identical (i.e., identical battery-assist mode peak current $i_{L(B.PK)}$). i_L is negative in battery-assist mode because it reverses direction. In Fig. 4, $i_{L(S.AVG)}'$ and $i_{L(B.AVG)}'$ are the average i_L across one E_S and E_B, respectively. Optimal $i_{L(S.PK)}$ and $i_{L(B.PK)}$ varies across v_{IN} and v_O, and the design of optimal packets is analyzed in detail in [25].

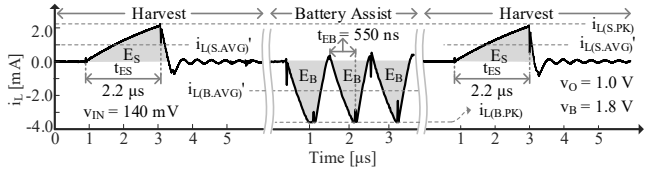

Fig. 4. Measured inductor current across operation modes.

If v_{IN} hits the TEG's maximum-power-Point (MPP) voltage v_{MPP} in harvest mode, MPP comparator CP_{MPP} trips, and the SLCR draws one E_S from v_{IN}. v_{IN} drops after drawing each E_S and recovers to v_{MPP} before drawing the next, as in Fig. 8. In battery-assist mode, E_S is intentionally skipped because supplying IoT load with enough power is a priority over harvesting energy from TEG. TEG outputs P_{MPP} if v_{IN} equals half v_S. v_{MPP} is chosen such that the average input voltage $v_{IN(AVG)}$ equals half v_S.

Delay t_{ES} loops SR latch in Fig. 2 to generate energize time t_{ES}. In harvest mode, L_X energizes across t_{ES} to harvest one E_S from v_{IN}, as in Fig. 4. t_{ES} is optimized across v_{MPP}, so the SLCR is optimally efficient across v_S. Fig. 5 shows optimal $i_{L(S.PK)}$ across v_S. With higher R_S, the TEG avails less power, and the MOS switches' leakage loss signifies. Thus, the channel widths of MOS switches are narrow with higher R_S to reduce leakage. This raises their conduction resistance and thus lowers the optimal peak current. The work does not need a current limit, as $i_{L(PK)}$ is at mA level. Loss analysis and measured efficiency of this proposed SLCR are in [25], and the max efficiencies in harvest and battery-assist mode are 77% and 88%, respectively. Delay t_{EB} loops SR latch to generate energize time t_{EB}. L_X energizes across t_{EB} in battery-assist mode to draw one E_B from v_B. t_{EB} is optimized for nominal v_B and v_O, which are 1.8 V and 1 V, respectively.

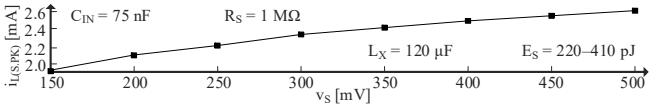

Fig. 5. Optimally efficient $i_{L(S.PK)}$ across v_S.

A. Output Loop

Operation and Model: CP_O, output capacitor C_O, IoT load, v_B, and SLCR power stage close the output loop in harvest mode. Given the constant-energy-packet scheme, the output loop does not adjust $i_{L(S.PK)}$ in harvest mode, as the i_L profile in Fig. 4 and 6 shows. Thus, although i_L varies at every time instance, the average i_L across one energy packet (labeled $i_{L(S.AVG)}'$ by

the dashed line in Fig. 4) is independent of the output loop. Given this independence, the SLCR power stage, on average, should be modeled as a current source in the output loop equivalent model in Fig. 7. This current source models the average current the SLCR outputs to v_O or v_B, which is a $D_{O(S)}$ fraction of $i_{L(S.AVG)}$'. $D_{O(S)}$ is M_{OB}'s or M_B's duty cycle in harvest mode. $i_{L(S.AVG)}$' nears half $i_{L(S.PK)}$. In harvest mode, the idling IoT load sources nA output current $i_{O(S)}$. The STDP switch is only a behavioral model that depicts CP_O directing energy to either v_O or v_B.

The model in Fig. 7 clearly shows that the output loop is fundamentally a relaxation oscillator. The current difference between $i_{L(S.AVG)}$ '$D_{O(S)}$ and $i_{O(S)}$ charges v_O when CP_O trips low, so v_O rises as its profile in Fig. 6 shows. Rise time t_{RISE} is

$$t_{RISE} = \frac{C_O \Delta v_{H(O)}}{i_{L(S.AVG)}\,'D_{O(S)} - i_{O(S)}} + t_P, \tag{1}$$

where t_P is the comparator propagation delay. When v_O reaches $v_{H(O+)}$, CP_O trips high, and the oscillator "relaxes" to let $i_{O(S)}$ drain v_O. Consequently, v_O's fall time is

$$t_{FALL} = \frac{C_O \Delta v_{H(O)}}{i_{O(S)}} + t_P. \tag{2}$$

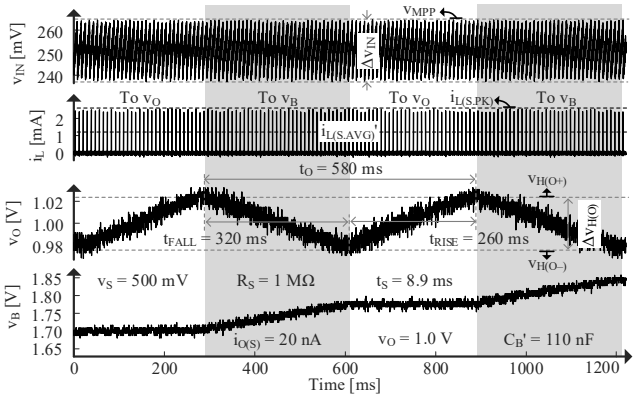

Fig. 6. Measured output loop large-signal oscillation waveforms.

When v_O hits $v_{H(O-)}$, CP_O trips low, and the control logic demands that the SLCR charge v_O again. This marks the start of the next oscillation cycle. Thus, v_O's oscillation period t_O is

$$t_O = t_{RISE} + t_{FALL}. \tag{3}$$

v_{IN} and i_L profiles in Fig. 6 show that v_{IN} drops by Δv_{IN} every time L_X draws one E_S from v_{IN} and recovers thereafter. More importantly, Fig. 6 shows that the output loop does not adjust $i_{L(S.PK)}$, so $i_{L(S.PK)}$ is independent of the output loop. Thus, Fig. 6 justifies the validity of modeling the SLCR power stage as a current source in the output loop model. v_B charges up when v_O falls, and E_S packets reach v_B. v_B profile in Fig. 6 is measured using a small 110-nF storage capacitor C_B for testing purposes only, to show discernable rise in v_B. The system charges v_B while keeping TEG at its MPP until v_B hits the CMOS breakdown voltage, which is 1.8 V for this work. Afterward, the harvester only draws power from the TEG to supply P_O without charging the v_B. Thus, the TEG would deviate from its MPP. In this prototype, an off-chip FPGA monitors v_B. Once v_B hits V_{BD}, the FPGA tells the SLCR to stop charging v_B. Breakdown protection, as in [16], can be applied to this work as well.

Stability: An oscillation is stable and sustaining if the total phase shift and gain are 360° and 1 at the oscillation frequency f_O [26]. Negative feedback with an additional 180° phase shift at f_O provides a 360° phase shift. CP_O reverses v_O's direction whenever it engages (trips). Because of this reversal effect, CP_O closes a negative feedback loop and offers 180° phase shift $\angle A_{CPO}$.

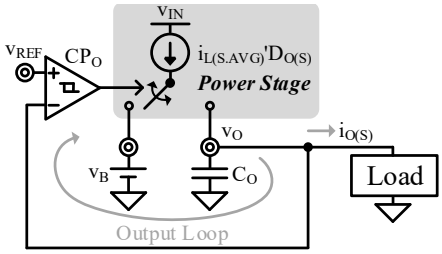

Fig. 7. Output loop large-signal oscillator model.

C_O delays the rise and fall of v_O and thus offers an additional phase shift at f_O. After CP_O engages and reverses v_O's direction when v_O hits $v_{H(O-)}$ at 600 ms in Fig. 6, CP_O "relaxes" and cannot keep engaging. This is because CP_O's trip point has risen from $v_{H(O-)}$ to $v_{H(O+)}$, and C_O delays the rise of v_O. CP_O re-engages and reverses v_O's direction at 900 ms after v_O rising delay t_{RISE}. After CP_O re-engages at 900 ms, it "relaxes" again and cannot keep engaging. It engages again at 1200 ms after v_O's falling delay t_{FALL}. Thus, the average delay $t_{DLY(AVG)}$ created by C_O is the average of the rising and falling delays:

$$t_{DLY(AVG)} = \frac{t_{RISE} + t_{FALL}}{2} = \frac{t_O}{2}. \tag{4}$$

The effective phase shift $\angle A_{DLY}$ caused by $t_{DLY(AVG)}$ at f_O is

$$\angle A_{DLY}\big|_{f_O} = \left(\frac{t_{DLY(AVG)}}{t_O}\right) \times 360° = 180°. \tag{5}$$

The output loop's total phase shift $\angle A_{LG(O)}$ at f_O therefore is

$$\angle A_{LG(O)}\big|_{f_O} = \angle A_{CPO} + \angle A_{DLY}\big|_{f_O} = 360°. \tag{6}$$

CP_O's hysteretic window sets v_O's oscillation amplitude and effectively forces the output loop's loop gain $A_{LG(O)}$ to 1 at f_O:

$$A_{LG(O)}\big|_{f_O} = 1. \tag{7}$$

Equations (6) and (7) justify that v_O oscillation is stable.

B. MPP Loop

Operation and Model: On-chip TEG, input capacitor C_{IN}, CP_{MPP}, SR latch and delay block t_{ES}, and SLCR power stage close the MPP loop. In harvest mode, if v_{IN} hits v_{MPP}, as in Fig. 8, CP_{MPP} trips high and triggers the SR latch in Fig. 2 to generate a pulse that closes M_{GB} to energize L_X. The fractional open-circuit voltage (FOCV) method [18] is applied to generate v_{MPP}. Pulse width is set by the v_{MPP}-dependent delay t_{ES}. Fig. 8 shows a zoomed-in i_L profile. For this particular E_S, L_X drains to v_O across drain time t_{DO}.

The input voltage v_{IN} rises every time after it plummets because the 250-mV source voltage v_S charges the input capacitor C_{IN} through the source resistance R_S. The v_S and R_S

are defined in Fig. 1. After v_{IN} rises to v_{MPP}, the MPP loop sends out an energizing command t_{ES} so that the SLCR draws one energy packet from the source. Therefore, the input voltage v_{IN} drops. After drawing one energy packet, v_{IN} drops below v_{MPP}, so CP_{MPP} dictates the SLCR to stop drawing energy from the source. Therefore, the input voltage v_{IN} can recover as v_S charges C_{IN} through R_S. After a duration of t_S, v_{IN} recovers to v_{MPP} again, and CP_{MPP} trips to dictate the SLCR to draw the next energy packet. C_{IN} suppresses the ripple of the v_{IN}, which is denoted as Δv_{IN} in Fig. 8. This way, the input voltage could be as close to a dc voltage as possible.

The optimal energizing time t_{ES} that gives the highest efficiency is the result of balancing ohmic loss, charge loss, and leakage loss. The details of designing the optimal t_{ES} are described in [25]. The 2.2-µs delay cell t_{ES} loops the SR latch to generate this 2.2-µs energizing time pulse, which is ultimately triggered by the Maximum-Power-Point (MPP) comparator CP_{MPP}. Once the input voltage v_{IN} hits v_{MPP} and causes CP_{MPP} to trip, the output of the SR latch is set to high. After a delay of t_{ES}, the reset signal of the SR latch trips high and then resets the output of the SR latch. As a result, a pulse of width t_{ES} is generated.

Similarly, because of the constant-energy-packet scheme, the MPP loop does not adjust $i_{L(S.PK)}$, as the i_L profile in Fig. 8 shows. Thus, although i_L varies at every time instance, the average i_L across one energy packet (labeled as $i_{L(S.AVG)}$' by the dashed line in Fig. 4) is independent of the MPP loop. Therefore, the current source in Fig. 9 models the average current drawn by the SLCR from v_{IN} across one E_S, which is the $i_{L(S.AVG)}$' labeled in Fig. 4. This current source is enabled for a preset duration (t_{ES}) every time CP_{MPP} trips high.

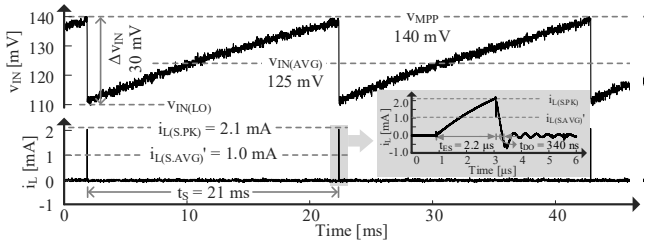

Fig. 8. Measured MPP loop large-signal oscillation waveforms.

The model in Fig. 9 shows that the MPP loop can also be interpreted as a relaxation oscillator. CP_{MPP}'s trip point v_{MPP} sets the upper bound of v_{IN}. Current source $i_{L(S.AVG}$' discharges v_{IN} from a designed C_{IN} for a preset duration t_{ES}. Thus, C_{IN}, $i_{L(S.AVG}$', and t_{ES} together set Δv_{IN}, which consequently sets v_{IN}'s lower bound $v_{IN(LO)}$ as labelled in Fig. 8. Therefore, the MPP loop is also a hysteretic relaxation oscillator.

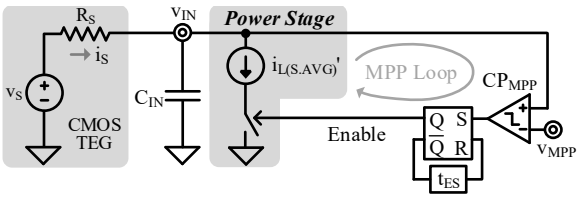

Fig. 9. MPP loop large-signal oscillation model.

After drawing one E_S from v_{IN} at 2 ms, as Fig. 8 shows, source current i_S charges C_{IN}, and therefore v_{IN} rises. When v_{IN} hits the hysteretic upper bound v_{MPP} again, the SLCR draws one E_S again and discharges v_{IN} to the lower hysteretic bound $v_{IN(LO)}$ once more at 23 ms. This marks the start of the next oscillation cycle. The SLCR draws one E_S per v_{IN} oscillation period t_S. To harvest the most power, the power drawn from v_{IN} should be close to P_{MPP}. Therefore, t_S is

$$t_S = \frac{E_S}{P_S} \approx \frac{E_S}{P_{MPP}} = \left(\frac{i_{L(S.PK)}{}^2}{2}\right)\left[\frac{R_S}{(0.5v_S)^2}\right], \tag{8}$$

where the optimal $i_{L(S.PK)}$ across v_S is shown in Fig. 5.

Stability: CP_{MPP} reverses the direction of v_{IN} every time it engages (discharges v_{IN}). i_S always reverses v_{IN}'s direction (charges v_{IN}) after the SLCR draws one E_S. Therefore, given this reversal effect, CP_{MPP} and i_S establish negative feedback. C_{IN} delays the rising of v_{IN} as i_S requires about 21 ms to charge v_{IN}, as Fig. 8 shows. C_{IN} also delays the falling of v_{IN} because it takes the SLCR one t_{ES} to discharge C_{IN}. Thus, for reasons similar to those stated for the output loop, C_{IN} also adds a 180° phase shift at v_{IN}'s oscillation frequency f_S. $i_{L(S.AVG)}$, t_{ES}, and C_{IN} set v_{IN}'s oscillation amplitude Δv_{IN}. Thus, the MPP loop's gain is 1 at f_S. Therefore, for the same reasons stated for the output loop, the MPP loop oscillation is also stable.

C. Load-Dump Loop

Operation and Model: The CP_{LD}, C_O, IoT load, and SLCR power stage close the load-dump loop. When the IoT load draws high load-dump current $i_{O(LD)}$, v_O drops to $v_{H(LD–)}$ at 27 µs, as in Fig. 10. Then, CP_{LD} trips low, and the SLCR enters battery-assist mode to deliver consecutive E_B packets to v_O. When CP_{LD} trips low, CP_{LD} is designed to override CP_O to prevent racing between the output loop and the load-dump loop. When v_O hits $v_{H(LD+)}$, CP_{LD} trips high, and the SLCR stops drawing E_B from v_B, so v_O falls. This way, CP_{LD} limits v_O within its hysteretic window $\Delta v_{H(LD)}$.

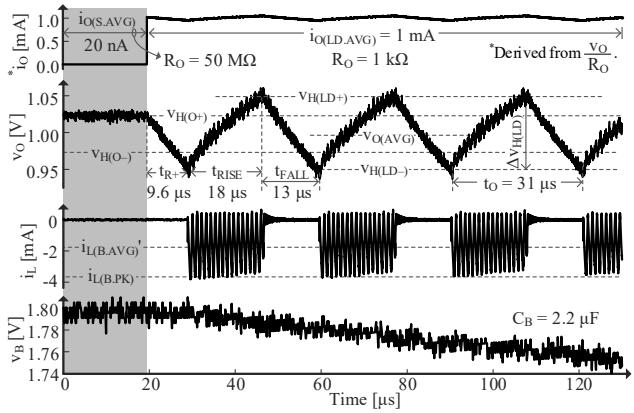

Fig. 10. Measured positive load dump transient waveforms.

Given the constant-energy-packet scheme, the load-dump loop does not adjust $i_{L(B.PK)}$ and E_B as in Fig. 10. Thus, during t_{RISE}, the average current the SLCR delivers to v_O is independent of the load-dump loop. Thus, although i_L varies at every time instance, the average i_L across one energy packet (labeled as $i_{L(B.AVG}$' by the dashed line in Fig. 4) is independent of the output loop. Similarly, because of this independency, the SLCR power stage is also modeled as a current source in

the load-dump loop equivalent model in Fig. 11. During t_{RISE}, the load-dump loop current source is enabled, and the current that the SLCR outputs from v_B to v_O is a $D_{O(B)}$ fraction of $i_{L(B.AVG)}$', where $i_{L(B.AVG)}$' is the average i_L across one E_B packet, as the i_L profiles show in Fig. 4 and 10, which is half $i_{L(B.PK)}$. $D_{O(B)}$ is the SLCR's output duty cycle. It is 1 if the SLCR bucks v_B to v_O; and $D_{O(B)}$ is M_{OI}'s duty cycle if the SLCR boosts v_B to v_O.

The model in Fig. 11 shows that the load-dump loop is also fundamentally a relaxation oscillator. The current difference between $i_{L(B.AVG)}$ '$D_{O(B)}$ and $i_{O(LD)}$ charges v_O when CP_{LD} trips low, so v_O rises, as in Fig. 10.v_O's rise time t_{RISE} is

$$t_{RISE} = \frac{C_O \Delta v_{H(LD)}}{i_{L(B.AVG)}\,'D_{O(B)} - i_{O(LD)}} + t_P, \tag{9}$$

where t_P is CP_{LD}'s propagation delay. When v_O hits $v_{H(LD+)}$, CP_{LD} trips high, and the SLCR stops delivering E_B packets, so $i_{O(LD)}$ drains v_O. Fall time t_{FALL} is

$$t_{FALL} = \frac{C_O \Delta v_{H(LD)}}{i_{O(LD)}} + t_P. \tag{10}$$

When v_O falls to $v_{H(LD-)}$, CP_{LD} trips low, and SLCR draws E_B to charge v_O again, which marks the start of the next oscillation cycle. The load-dump loop's t_O is the same as in (3).

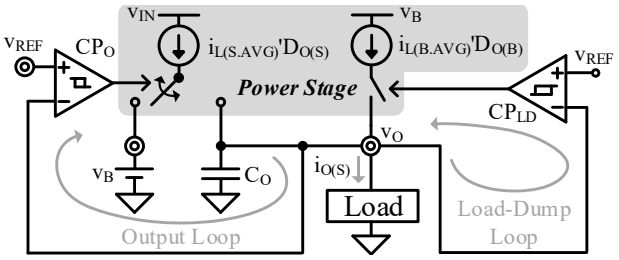

Fig. 11. Load-dump loop large-signal oscillator model.

Stability: The load-dump loop, if alone, is stable for reasons similar to those stated for the output loop. However, the load-dump loop is not alone, as the output loop parallels it. Fig. 11 shows this parallel arrangement. If v_{IN} hits v_{MPP} when a falling v_O falls between $v_{H(O-)}$ and $v_{H(LD-)}$, the output loop tries to deliver one E_S to v_O. However, because P_{MPP} is too low to supply P_O when the load current is high, v_O keeps falling and would inevitably drop below $v_{H(LD-)}$. This means the output loop is railed out so that v_O keeps dropping despite the output loop's actions. Because it has been railed out, the output loop's gain $A_{LG(O)}$ is effectively zero:

$$A_{LG(O)}\Big|_{RAILED-OUT} = 0. \tag{11}$$

When the load-dump loop relaxes as v_O falls, it leaves only a railed-out output loop with zero loop gain. Thus, the load-dump loop dominates the output loop in battery-assist mode, and no instability would arise from paralleling two loops.

D. Response Time

Light Load Dump: If P_{MPP} can supply the variation of P_O, the SLCR stays in harvest mode, and this paper calls this light P_O variation a "light load dump." Fig. 12 shows measured responses of rising and falling light load dumps when $i_{O(S)}$ steps between 20 nA and 40 nA. A higher i_O demands more E_S to charge v_O from $v_{H(O-)}$ to $v_{H(O+)}$, so t_{RISE} increases from 260 ms to 830 ms. t_{FALL} decreases from 320 ms to 160 ms because a higher $i_{O(S)}$ discharges v_O faster. Because less E_S reaches v_B with a higher $i_{O(S)}$, v_B charges with shorter charging interval t_{CHG}, as the v_B profile shows. Because the SLCR needs not activate the load-dump loop for light load dumps, it responds within one t_O.

Heavy Load Dump: If P_{MPP} is insufficient to supply the increase of P_O, the SLCR must activate the load-dump loop and enter battery-assist mode. Similarly, if there is a drastically falling load dump, the SLCR must deactivate the load-dump loop and re-enter harvest mode. This paper calls this drastic P_O variation a "heavy load dump." Fig. 10 shows measured waveforms of a heavy rising 1-mA load dump.

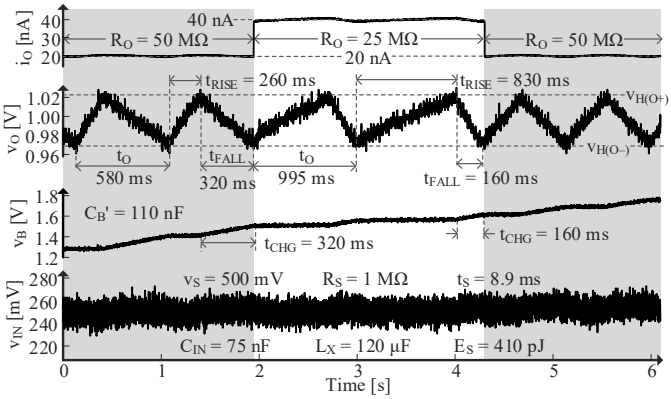

Fig. 12. Transient waveforms of a light load dump.

Confronting a heavy rising load dump when v_O is nearing $v_{H(O+)}$ results in the worst-case response time t_{R+}. As Fig. 10 shows, v_O is nearing $v_{H(O+)}$ when i_O steps from 20 nA to 1 mA at 20 µs. To activate the load-dump loop, v_O must fall from $v_{H(O+)}$ to $v_{H(LD-)}$. This means $i_{O(LD)}$ must discharge v_O across the widest voltage range, which is the most time-consuming and results in the worst-case t_{R+}. In Fig. 10, v_O hits $v_{H(LD-)}$ at about 29 µs, and the measured t_{R+} is about 9.6 µs. Worst-case t_{R+} is v_O's worst-case discharge time plus CP_{HYS}'s t_P, as in (12).

$$t_{R+} = \frac{C_O\left(0.5\Delta v_{H(O)} + 0.5\Delta v_{H(LD)}\right)}{i_{O(LD)}} + t_P. \tag{12}$$

Confronting a heavy falling load dump when v_O is nearing $v_{H(LD-)}$ results in worst-case response time t_{R-}. Fig. 13 shows measured waveforms under a heavy falling 1-mA load dump. When v_O is nearing $v_{H(LD-)}$ at 90 µs, i_O steps from 1 mA to 20 nA. To de-activate the load-dump loop and exit battery-assist mode, v_O must reach $v_{H(LD+)}$ from $v_{H(LD-)}$. This means the SLCR must charge v_O across the widest voltage range, which is the most time-consuming and results in the worst-case t_{R-}. CP_{LD} reacts a t_P after v_O hitting $v_{H(LD+)}$, and therefore causes an overshoot. Measured overshoot voltage v_{OVSHT} is 35 mV with 1.6-µs t_P, and the resulting t_{R-} is 9.3 µs. Worst-case t_{R-} is v_O's worst-case charging time plus CP_{HYS}'s t_P, as in (13).

$$t_{R-} = \frac{C_O \Delta v_{H(LD)}}{i_{L(B.AVG)}\,'D_{O(B)} - i_{O(S)}} + t_P \approx \frac{C_O \Delta v_{H(LD)}}{i_{L(B.AVG)}\,'D_{O(B)}} + t_P. \tag{13}$$

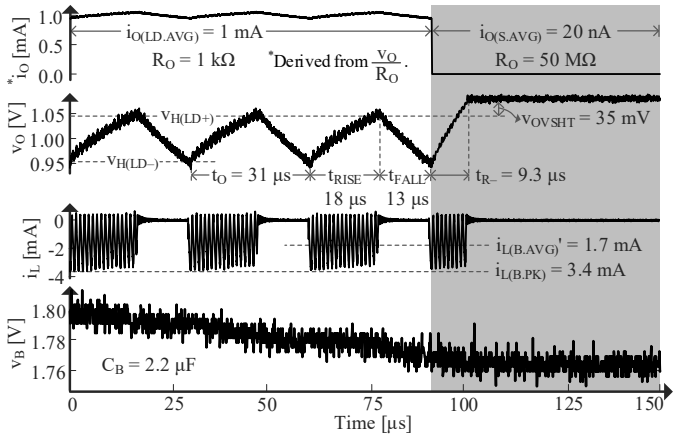

Fig. 13. Measured negative load dump transient waveforms.

Because the switching logic skips E_S packets in battery-assist mode, v_{IN} may reach beyond v_{MPP}. After a falling heavy load dump, the MPP loop and v_{IN} must resettle to steady state. As Fig. 14 shows, when the SLCR exits battery-assist mode at 23.5 ms, the MPP loop immediately draws consecutive E_S packets from v_{IN} until v_{IN} drops below v_{MPP}. Because v_{IN}'s valley value at 23.5 ms is higher than v_{IN}'s steady state valley value, it takes v_{IN} only 4.4 ms (less than steady state t_S, which is 8.9 ms) to recharge to v_{MPP} again. Thus, v_{IN} hits v_{MPP} again at 28 ms, and MPP loop draws another E_S. After 28 ms, the MPP loop settles to steady state. As a result, the MPP loop settles within one t_S.

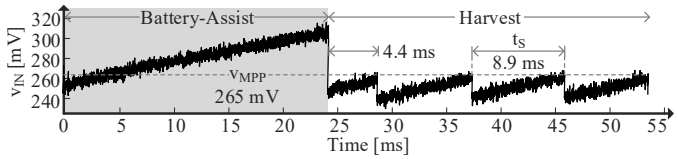

Fig. 14. Measured v_{IN} recovery during a negative load dump.

III. Prototype Design

A. IoT Wireless Microsensor

To reduce power consumption, IoT wireless microsensors mostly idle and sense and transmit data only on demand. Fig. 15 shows the load current profile of a typical IoT wireless microsensor. When idling, state-of-the-art (SoA) sensors may consume sub-nW standby power [27]. Some sensors adopt always-on wake-up receivers (Rx), and SoA wake-up Rx may consume sub-nW [28], leading to sub-nW total standby power. Thus, idle load current $i_{O(IDLE)}$ in Fig. 15 is sub-nW.

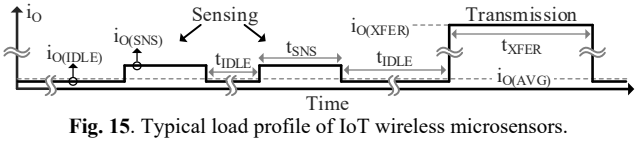

Fig. 15. Typical load profile of IoT wireless microsensors.

When sensing, SoA sensors consume 10–100 nW [1, 25], so the sensing load current $i_{O(SNS)}$ is on the order of nA. During transmission, SoA transmitters (Tx) may consume 1.2 mW from 0.8–1.0 V supply voltages [12]; thus, transmission load current $i_{O(XFER)}$ is on the order of 1 mA. The duration of each transmission (t_{XFER}) is 500 µs–7 ms [13–14]. Practical IoT sensors may transmit only four times per day [15], so idling time t_{IDLE} is much longer than sensing time t_{SNS} and t_{XFER}. As a result, average load current $i_{O(AVG)}$ is nearing $i_{O(IDLE)}$. Table II lists typical performances of SoA IoT wireless microsensors.

Table II: SoA Low-Power IoT Wireless Microsensors

Item	Value	Item	Value	Item	Value
v_O	0.8–1.0 V	t_{XFER}	0.5–7 ms	–	–
$P_{O(IDLE)}$	410–810 pW	$P_{O(SNS)}$	6.4–43 nW	$P_{O(XFER)}$	0.63–1.2 mW
$i_{O(IDLE)}$	410–810 pA	$i_{O(SNS)}$	6.4–43 nA	$i_{O(XFER)}$	0.63–1.2 mA

B. Hystereses

$\Delta v_{H(O)}$ and $\Delta v_{H(LD)}$ must overcome noise floor v_N^* so that CP_O and CP_{LD} can trip properly. Therefore, CP_O's hysteretic window $\Delta v_{H(O)}$ should be much greater than v_N^*, as in (14).

$$\Delta v_{H(O)} >> v_N^* . \tag{14}$$

CP_{LD}'s hysteretic window $\Delta v_{H(LD)}$ must be amply separated from $\Delta v_{H(O)}$ so that CP_{LD} does not misfire in the presence of noise, as in Fig. 10. Thus, $\Delta v_{H(LD)}$ 'ss design constraints is

$$\Delta v_{H(LD)} - \Delta v_{H(O)} >> v_N^* . \tag{15}$$

C. Input Capacitor

C_{IN} suppresses Δv_{IN}. When drawing E_S from v_{IN}, C_{IN} supplies energy ΔE_{CIN} temporarily, and v_{IN} drops from v_{MPP} to (v_{MPP}–Δv_{IN}). Because R_S is on the order of MΩ, C_{IN} temporarily supplies most E_S energy, so E_S is roughly ΔE_{CIN}, as in (16).

$$E_L \approx \Delta E_{CIN} = 0.5 C_{IN}\left[v_{MPP}{}^2 - \left(v_{MPP} - \Delta v_{IN}\right)^2 \right]. \tag{16}$$

Therefore, Δv_{IN} is

$$\Delta v_{IN} \approx \frac{E_L}{C_{IN} v_{MPP}} >> v_N^* . \tag{17}$$

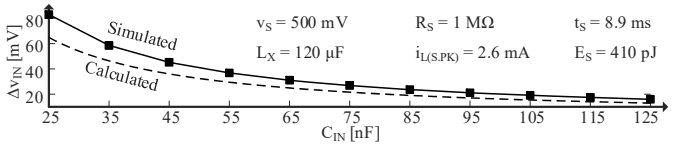

Fig. 16. Δv_{IN} across C_{IN}.

However, Δv_{IN} must be large enough to overcome v_N^* so CP_{MPP} can trip properly, as (17) depicts. Fig. 16 shows calculated and simulated Δv_{IN} across C_{IN}. This work sets Δv_{IN} to 30 mV to overcome v_N^*, and the resulting C_{IN} is 75 nF.

D. Output Capacitor

t_R dictates C_O selection. This design aims at fast response against rising heavy load dumps. t_{R+} is set to be less than 5% of the 500-µs minimum transmission duration $t_{XFER(MIN)}$ [13]:

$$t_{R+} < 5\% t_{XFER(MIN)} . \tag{18}$$

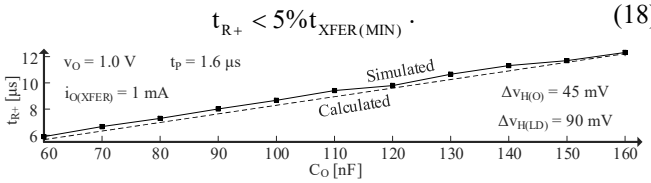

Fig. 17. t_{R+} across C_O.

For a Tx that draws 1-mA $i_{O(XFER)}$ from 1-V v_O, forcing (12) less than 5% $t_{XFER(MIN)}$ results in (19), which demands C_O < 350 nF. Fig. 17 shows simulated and calculated t_{R+} across C_O. For design margin, this work uses a 110-nF C_O.

$$C_O < \frac{\left(5\%t_{XFER(MIN)} - t_P\right) i_{O(XFER)}}{0.5\Delta v_{H(O)} + 0.5\Delta v_{H(LD)}}. \quad (19)$$

E. Storage Capacitor

When the ambient energy source disappears, IoT sensors become offline. IoT sensors must transmit all data previously acquired, in addition to sending an off-line report [29]. Each transmission event requires energy E_{XFER}:

$$E_{XFER} = P_{O(XFER)} t_{XFER}. \quad (20)$$

Therefore, storage capacitor C_B must hold enough energy to sustain two E_{XFER}. To minimize the size of C_B, C_B must hold the highest energy with lowest capacitance. This means v_B should start at its maximum voltage, which is the CMOS breakdown voltage V_{BD}. Assuming two E_{XFER} discharge C_B by Δv_B, the energy ΔE_{CB} drawn from C_B is

$$\Delta E_{CB} = 0.5C_B\left[V_{BD}{}^2 - \left(V_{BD} - \Delta v_B\right)^2\right] \approx 2E_{XFER}. \quad (21)$$

Therefore, Δv_B is

$$\Delta v_B = V_{BD} - \sqrt{V_{BD}{}^2 - \frac{2E_{XFER}}{0.5C_B}}. \quad (22)$$

Simulated and calculated Δv_B across C_B are illustrated in Fig. 18. To prevent crashing v_B, this design chooses a 2.2-µF C_B, and the resulting Δv_B is about 400 mV. SPICE simulation generated the simulation results shown in Fig. 16–18.

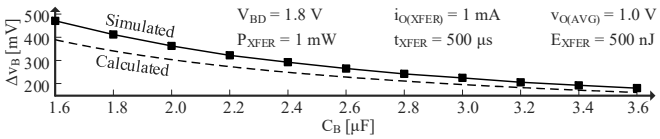

Fig. 18. Δv_B across C_B.

IV. Measured Performance

The 180-nm CMOS prototype in Fig. 19 integrates the power switches, gate drivers, and max block (Fig. 2). The printed circuit board (PCB) shows the 5 × 5 mm^2 IC package and the 3 × 3 × 1 mm^3 inductor. C_{IN}, C_O, and C_B are multi-layer ceramic capacitors. Their total leakage loss, measured by Keithley 6485 Pico-Ammeter with ±10-fA accuracy, is 60–70 pW. Like [25, 30], an onboard voltage source emulates on-chip TEG's v_S, and a 1-MΩ onboard resistor emulates R_S. A field-programmable gate array (FPGA) controls the SLCR. State-of-the-art on-chip controllers consume around 50 pJ / cycle, as in [25]. In harvest mode, this translates to a current consumption of 1.25–5 nA, given t_S is around 10–40 ms, as in Fig. 23, and the controller supply v_{MAX} could be as low as 1 V. The impact of the controller power consumption is presented in detail in [25] and shows that the controller power would decrease the overall efficiency by 8%.

A grounded metal noise shield encloses the PCB and reduces noise at low power level for all measurements. Additionally, all measurements were conducted in a noise-shielded metal chamber. Onboard off-the-shelf unity-gain buffers with 2-fA input current drives all voltage probes to prevent them from loading the Device Under Test (DUT) directly.

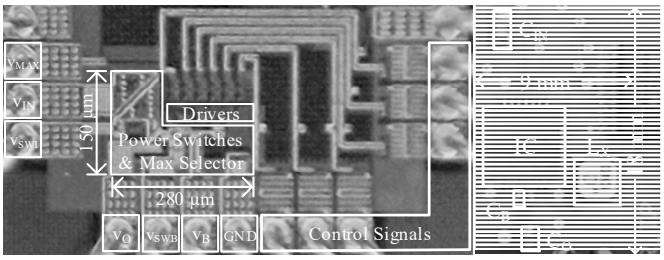

Fig. 19. 180-nm CMOS die and PCB photograph.

A. Response Time

Measured and calculated t_{R+} and t_{R-} across load dump current $i_{O(LD)}$ are shown in Fig. 20. For increasing $i_{O(LD)}$, t_{R+} shortens because $i_{O(LD)}$ discharges v_O faster from $v_{H(O+)}$ to $v_{H(LD-)}$. For falling heavy load dumps, pre-determined constant E_B packets charge C_O from $v_{H(LD-)}$ to $v_{H(LD+)}$. Constant E_B packets are independent of $i_{O(LD)}$; therefore, t_{R-} is approximately independent of $i_{O(LD)}$. Assuming a $i_{O(XFER)}$ of about 1 mA, as Section III. A. justifies, t_{R+} is 9.6 µs when the IoT sensor abruptly activates data transmission.

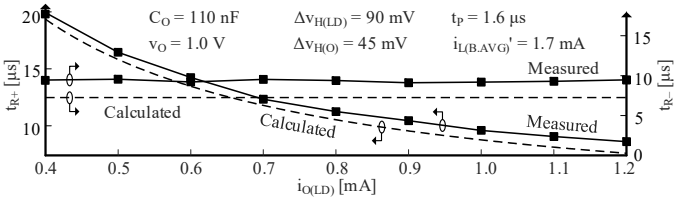

Fig. 20. $t_{R\pm}$ across load-dump current $i_{O(LD)}$.

B. Accuracy

Static: When the SLCR reaches steady state in harvest mode, v_O ripples within $\Delta v_{H(O)}$. Because millisecond t_O is much greater than microsecond t_P in harvest mode, t_P's effect on static v_O error $v_{OE(S)}$ is negligible. Therefore, $v_{OE(S)}$ is approximately half the hysteretic window $\Delta v_{H(O)}$ as in (23).

$$v_{OE(S)} = \pm\left[0.5\Delta v_{H(O)} + t_P\left(\frac{dv_O}{dt}\right)\right] \approx \pm 0.5\Delta v_{H(O)}. \quad (23)$$

Dynamic: Dynamic v_O error $v_{OE(D)}$ gauges v_O accuracy under rising and falling heavy load dumps. Because t_P is comparable to t_{R+} and t_{R-}, t_P's effects on $v_{OE(D)}$ are noticeable. t_P exacerbates dynamic v_O error $v_{OE(D)+}$ under rising heavy load dumps because $i_{O(LD)}$ keeps discharging v_O below $v_{H(LD-)}$ before CP_{LD} can react. Therefore, $v_{OE(D)+}$ is half $\Delta v_{H(LD)}$ plus the extra drop caused by t_P as in (24).

$$v_{OE(D)+} = 0.5\Delta v_{H(LD)} + t_P\left(\frac{i_{O(LD)}}{C_O}\right). \quad (24)$$

t_P exacerbates dynamic v_O error $v_{OE(D)-}$ under falling heavy load dumps as extra E_B would overcharge v_O beyond $v_{H(LD+)}$ before CP_{LD} can tell the SLCR to stop delivering E_B packets. $v_{OE(D)-}$ is half $\Delta v_{H(LD)}$ plus the extra overcharge caused by t_P:

$$v_{OE(D)-} \approx 0.5\Delta v_{H(LD)} + t_P\left(\frac{i_{L(B.AVG)}{}' D_{O(B)}}{C_O}\right). \quad (25)$$

Measured and calculated $v_{OE(D)+}$ and $v_{OE(D)-}$ are shown in Fig. 21. As $i_{O(LD)}$ increases, v_O drops faster under falling heavy load dumps. Therefore $v_{OE(D)+}$ increases because with higher

$i_{O(LD)}$, v_O would drop lower during a given t_P. Like t_{R-}, $v_{OE(D)-}$ is roughly independent from $i_{O(LD)}$ because the pre-determined constant E_B packets overcharge v_O.

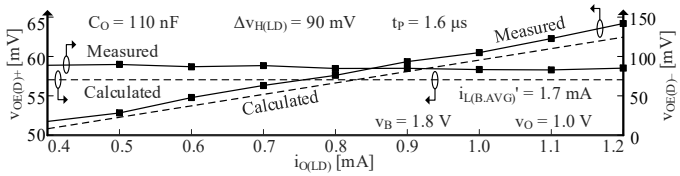

Fig. 21. Dynamic output error.

C. Oscillation Periods

Output Loop: Measured and calculated harvest-mode t_O across static load current $i_{O(S)}$ is shown in Fig. 22. As $i_{O(S)}$ increases, t_{FALL} shortens with increasing $i_{O(S)}$ because a higher $i_{O(S)}$ discharges v_O faster. Therefore, t_O shortens at first because t_{FALL} decreases. As $i_{O(S)}$ keeps increasing, charging v_O from $v_{H(O-)}$ to $v_{H(O+)}$ requires more E_S. Therefore, t_{RISE} increases with increasing $i_{O(S)}$, and t_O eventually starts to increase as $i_{O(S)}$ increases. The measured shortest t_O is about 580 ms, so the maximum harvest-mode oscillating frequency f_O is 1.7 Hz. As v_S rises, the TEG avails more power so the SL charges the output faster as each energy packet becomes larger (i.e., higher $i_{L(PK)}$ as Fig. 5 shows). Thus, t_{RISE} decreases as v_S rises. Comparators execute system operation without a clock. So, the system automatically adjusts its frequency according to R_S and can offset non-idealities such as R_S variation.

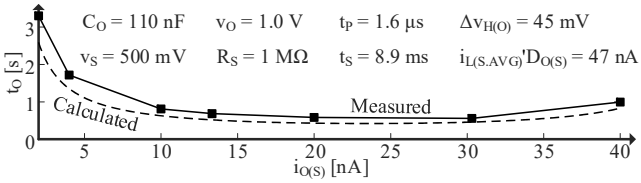

Fig. 22. t_O across static load current $i_{O(S)}$.

MPP Loop: Measured and calculated t_S across v_S are shown in Fig. 23. The energy source avails more power as v_S rises. Therefore, the MPP loop draws more frequent E_S packets from v_{IN} so t_S drops. Calculated t_S deviates more from measured t_S when v_S is low. This is because with lower v_S, Δv_{IN} becomes comparatively more significant, while (8) neglects Δv_{IN}. As Δv_{IN} becomes more significant, the power drawn by the SLCR becomes less and less than P_{MPP}. Therefore, calculated t_S deviates more from measured t_S as v_S decreases.

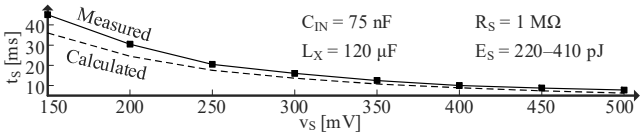

Fig. 23. t_S across v_S.

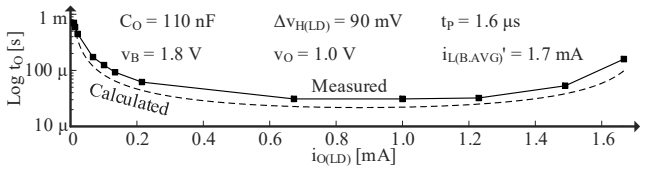

Fig. 24. t_O across load-dump current $i_{O(LD)}$.

Load Dump Loop: Measured and calculated load-dump loop t_O across load dump current $i_{O(LD)}$ is shown in Fig. 24. Similarly, there exists a minimum for the t_O of the load-dump loop. The measured shortest load-dump loop t_O is about 31 µs, so the maximum load-dump loop f_O is about 32 kHz.

D. Charging Profile

Fig. 25 measures the charging profile across 76 seconds to let v_B charge to V_{BD}. CP_O's hysteretic window sustains and bounds v_O's oscillation. v_{IN} is about 0.5 v_S with 30-mV Δv_{IN}.

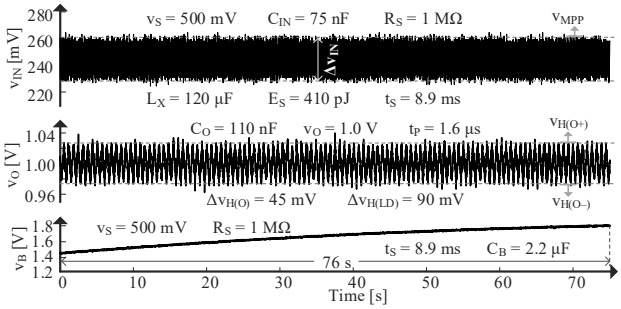

Fig. 25. Charging profile.

E. Efficiency

Fig. 26 measures the efficiency of the fast energy-harvesting SLCR prototype in harvest mode [25]. The harvest-mode efficiency η_I stays flat at the optimal level across load power P_O as mentioned in Section II, thanks to the constant energy packet scheme. η_I decreases as the maximum available power P_{MPP} decreases, given that the leakage loss of the MOSFET switches does not scale with P_{MPP}. As P_{MPP} decreases, leakage loss becomes more dominant, and thus η_I plummets. The peak efficiency in harvest mode is around 77%.

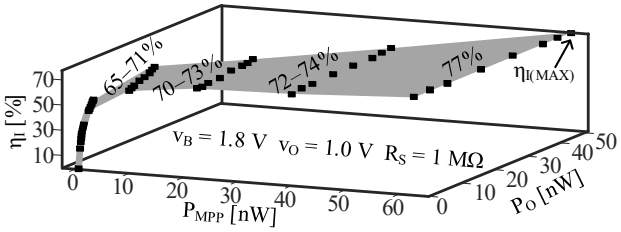

Fig. 26. Measured harvest-mode efficiency across P_{MPP} and P_O.

Fig. 27 measures the efficiency of the fast energy-harvesting SLCR prototype in battery-assist mode [25]. Similarly, because of the constant energy packet scheme, the battery-assist mode efficiency η_C stays flat at the optimal level across load power P_O as well. As load power P_O scales down, the leakage loss of the MOSFET switches (which does not scale with P_O) similarly starts to dominate, so η_C drops. The peak efficiency in battery-assist mode is around 88% when bucking and around 59% when boosting. Switch M_B's conduction resistance rises as v_B lowers, therefore the efficiency in boost mode is lower than that in buck mode. This paper focuses on control loop analysis but not on efficiency analysis. Detailed efficiency analysis is available in [25].

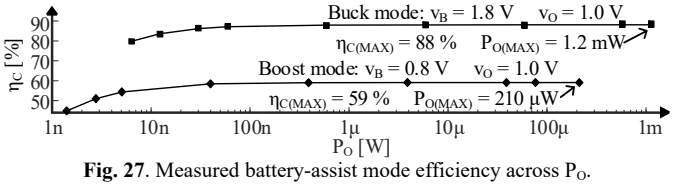

Fig. 27. Measured battery-assist mode efficiency across P_O.

F. Relative Performance

Table III compares SoA CMOS SLCRs. The design in [17] is an energy-harvesting charger that incorporates a low dropout (LDO) regulator to supply the 1.2-V load. Its fundamental drawback is that if v_B is lower than v_O, the design in [17] cannot supply the load.

The designs in [21–24] report 100 µs–2.5 ms t_R. The design in [21] uses a clocked pulse frequency modulation (PFM) scheme, which adjusts switching frequency f_{SW} according to the load demand. But the design in [21] must wait two clock cycles before it increases f_{SW} to react to load dumps, which leads to a slow 2.5 ms t_{R+} under a 180 µA rising load dump. 2.5 ms t_{R+} is too slow given that t_{XFER} is 500 µs–7 ms. Similarly, in [22], the converter must wait until the clock's falling edge before it reacts to rising load dumps. So, the resulting t_{R+} is still 100 µs. Designs in [23–24] use voltage mode pulse width modulation (PWM) in battery-assist mode. These designs need 2.2- or 10-µF C_O to establish a low-frequency dominant pole to stabilize the voltage loop. The drawback is that a higher C_O results in a longer time for v_O to discharge below $v_{H(LD-)}$ (or charge beyond $v_{H(LD+)}$). Consequently, t_R is 100 µs to 2.5 ms.

Thanks to the proposed self-oscillating nested hysteretic control, capacitor selection does not affect loop stability, as Section II justifies. Therefore, the C_{IN}, C_O, and C_B selected for this design are 1.3–1300×, 9.1–91×, and 45× smaller than the SoA. This not only reduces system size but also accelerates loop response. The measured response time is 9.6 µs, which is 10–260× faster than the SoA. Although this proposed system creates large and frequency-varying output voltage ripples, the frequencies of such ripples are no higher than 32 kHz in battery-assist mode and 1.7 Hz in harvest mode. An LDO usually provides good power supply rejection (PSR) up to 100 kHz bandwidth and can be added to suppress the output voltage ripple if necessary. This specific implementation excludes a cold-start feature, but a cold-start sequence similar to [30] is applicable to this work. It uses a starter circuit to build up high voltage on a small capacitor from which it bootstraps the SL afterwards. With this control, power supplies can respond faster to IoT sensor's power demands.

V. Conclusions

This paper proposes a fast self-oscillating nested hysteretic CMOS switched-inductor charging regulator microsystem that harvest energy from resistive on-chip thermoelectric generators to power IoT sensors. The principle is to analyse the proposed hysteretic control as relaxation oscillators. This paper contributes detailed theory and insightful expressions on hysteretic loop stability, oscillation period, response time, and accuracy. This paper also contributes intuitive expressions that guide system level design (i.e., input, output, and storage capacitors, and hysteretic windows). A 180-nm CMOS prototype validates the proposed control. The measured response time is 9.6 µs, which is 10–260× faster than prior arts.

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Table III: Relative Performance

Parameter	[21]	[22]	[16]	[17]	[18]	[19]	[20]	[23]	[24]	This work
Tech. [nm]	180	500	180	180	28	180	180	180	210	180
v_S [V]	–	–	–	0.05–1	0.2–0.8**	0.06–0.18**	0.1–0.6**	–	–	0.15–0.5
R_S [MΩ]	–	–	–	0.16	0.00053	0.00021	–	–	–	***1.0***
v_O [V]	1.0 and 1.8	1.0–3.3	1.0	1.2 V from LDO	0.4–1.4	1.0, 1.3, and 1.6	0.5 and 1.2	1.0	1.0	1.0
i_O [mA]	–	–	10^{-5}–10^{-3}	< 2	0.001–60	–	0.01–2.5	0–1.0	0–10	0–1.6
v_B [V]	3.0	–	2.9–4.1	1.3	1.8	2.4	1.2	1.8	1.8	1.8
C_{IN} [nF]	10000	4700	–	10000	–	10000	10000	220	100	***75***
C_O [nF]	10000	10000	–	10000	1000	2200	1000	2200	10000	***110***
C_B [nF]	–	–	–	100	–	–	100	–	–	***2.2***
$v_{OE(S)}$ [mV]	15*	25*	–	–	40	35*	13*	25	28	25
$v_{OE(D)}$ [mV]	50*	100*	–	–	40	35*	25*	77	72	80
Δi_O [mA]	0.18	20	–	–	1.0	4.5	1.0	1.0	10	1
t_R [µs]	2000*	100*	–	–	–	–	–	2500	100	***9.6***
Max Efficiency [%]	83	95	87	87	89	90.2	84.4	86	88	***88***
FoM [s^{-2}] ***	180 k	200 M	–	–	–	–	–	2.4 M	140 M	***1.2 G***

*Estimates from transient waveforms. **Estimates assuming $v_S = 0.5v_{IN}$, $P_S = v_S^2/4R_S$.

***The system desires small C_O, t_R, and dynamic error $v_{OE(D)}$ even under drastic Δi_O, so the Figure of Merit (FoM) is defined as: $FoM = \Delta i_O / (C_O \times t_R \times v_{OE(D)})$.

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