Lowest-v_{IN} CMOS Single-Inductor Boost Charger: Design, Limits, and Validation

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***Abstract*—The lowest input voltage for a single-inductor switched-inductor (SL) boost charger to draw power is critical for energy-harvesting applications. When a battery is fully discharged, the charger solely relies on the millivolt input-source voltage v_S to wake the system. When the charger is awake and operates in static mode, it needs to draw power from low-voltage v_S efficiently. Thus, the major contribution of this paper is theorizing the fundamental limits of SL converters, and experimentally validating the lowest v_S possible for a single-inductor boost to operate, both in wake and static mode. This paper derives closed-form design expressions for all circuit components and validates the design theory with a 1.6-µm CMOS prototype. When source resistance is 350 Ω, this prototype validates that the lowest-possible v_S for SLs in wake mode is 225–285 mV. In static mode, the lowest-possible v_S for SLs is 40 mV. Despite recent literature shows that switched-capacitors (SCs) can wake with lower v_S, theorizing and experimentally validating the lowest v_S possible for SL converters can prove the fundamental limits of SL chargers. Moreover, since this paper also validates that SLs operate with lower v_S than SCs in static mode, thus, SC-SL hybrids are the best system.**

Keywords—Switched inductor, CMOS, boost charger, low-voltage, low-power, wake, static, design theory, experimental validation.

I. Low-v_{IN} Microsystems

Internet-of-Things (IoT) technologies can save money, energy, and lives [1]. Powering these low-voltage, energy-limited tiny microsystems is challenging because their tiny on-board batteries v_B drain quickly. Also, these IoT micro-systems are often placed at hard-to-reach locations, so replacing batteries is prohibitively expensive. One solution is to harvest ambient energy to recharge their batteries. Energy sources like thermoelectric generators (TEGs), photovoltaic (PV) cells, and microbial fuel cells (MFCs) [2] can collect energy from temperature gradient, light, and biochemical reactions to power IoT microsystems.

One challenge brought by these energy sources is that source voltage v_S may become unavailable. When ambient energy is absent for a prolonged duration, v_S stays at 0 V and tiny on-board battery v_B can get fully discharged. When v_S recovers to 40–350 mV again, the switched-inductor (SL) charger shown in Fig. 1 must solely rely on this 40–350-mV v_S to wake the system and charge v_B when v_B is initially 0 V [3].

Despite recent literature like [7] shows Switched Capacitors (SCs) requires lower v_S to wake the system, theorizing and experimentally validating the lowest-possible v_S to wake a SL charger can help understand the fundamental limits of SL converters during the wake-up process.

Another challenge is with only 40–350-mV v_S, chargers must be highly efficient when the system is awake and operates in static mode. SL chargers are superior to SCs in static mode because SLs are more efficient and requires lower v_S to harvest power. Therefore, this paper also theorizes and experimentally validates the optimal peak inductor current so that SLs can charge v_B to the targeted battery voltage $v_{B(TAR)}$ with the lowest-possible v_S in static mode.

The third challenge is compactness. The volume of tiny IoT microsensors is often in millimeter-scale [11]. This means IoT microsystems can only use one tiny off-chip inductor [4], which is often lossy [10]. Thus, this paper theorizes single-inductor SLs. Moreover, for miniaturization, millimeter-scale thin-film TEGs are much more appealing than patch TEGs, because bulky patch TEGs may occupy 49–115× larger area [6–7, 17]. However, millimeter-scale TEG's internal source resistance R_S can be 29–70× higher than the R_S of patch TEGs. This high R_S further limits available power.

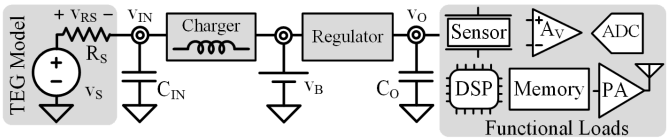

Fig. 1. DC-sourced low-v_{IN} microsystem.

To distinguish this paper from [3], this paper provides experimental data that validate the proposed design theory and adds complete closed-form design expressions. This paper focuses on the wake-capable single-inductor SL boost charger in Fig. 1. Compared with [3], major contributions of this paper are:

1) Experimental validation: with a 1.6-µm CMOS prototype, the lowest v_S for a single-inductor SL charger to operate in both wake and static mode are measured across all design variables (i.e., inductor, power switch channel width, ring oscillator design, & peak inductor current). Results prove the theory and experimentally validates the fundamental limits on the lowest-possible v_S for SL chargers.
2) Closed-form design expressions: in addition to theoretical derivations presented in [3], this paper directly provides closed-form design expressions for every component in a wake-capable single-inductor SL charger, while taking the voltage drop across the high R_S into account.

This paper is organized as follows: Section II derives closed-form design formulas for every circuit block of the wake-capable single-inductor boost charger, so that it can operate with the lowest-possible v_S. Section III validates the theory across all design variables using a 1.6-µm CMOS prototype. Section IV compares and discusses prior arts. Section V draws conclusions.

II. Lowest-v_{IN} Switched-Inductor Design

A. Boost Charger

Wake-capable single-inductor SL boost charger is shown in Fig. 2. When v_S rises above 0 V after a prolonged absence, v_B is fully

This paper provides additional experimental data and closed-form expressions to a previous conference paper which has been presented at IEEE 62nd International Midwest Symposium on Circuits and Systems, Dallas, TX, USA, 2019.

discharged to 0 V and the highest voltage available is this 40–350-mV v_S. Thus, the v_B-supplied static control shown in Fig. 2 & 5 is inactive, and the SL solely relies on v_S to charge v_B in wake mode. Headroom voltage V_{HR} is the lowest voltage required to supply the static control and fully turn on power switches. Static control detects when v_B reaches V_{HR} and transits the system into static mode to operate with much higher efficiency.

Wake: In wake mode, the lowest-possible v_S such that the SL can boost voltage and output net power to v_B is called wake output threshold $v_{W(O)}$ in this paper. An integrated low-voltage ring oscillator (R.O.) in Fig. 2 generates gate control signal for ground switch M_G since static control is inactive. An R.O. is preferred over an LC oscillator because it is fully integrated and needs no additional inductor. M_G closes to energize L_X from v_{IN}, and inductor current i_L starts to increase. When M_G opens, i_L charges parasitic C_{SW} until v_{SW} rises and diode-connected MOSFET D_B forward-biases to steer i_L into v_B. The SL is asynchronous in wake mode. Therefore, when i_L reaches 0 in wake mode, D_B will be reverse-biased to stop reverse i_L flow.

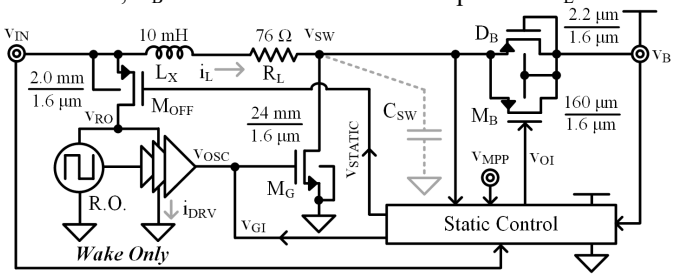

Fig. 2. Wake-capable single-inductor low-v_{IN} SL CMOS charger.

Design target in wake mode is not high efficiency, but to minimize $v_{W(O)}$ so the SL charger can transit out of wake mode with the lowest-possible v_S. To minimize $v_{W(O)}$, L_X must carry as much energy as possible to charge C_{SW} and forward-bias D_B. So, M_G should close for a long-enough period until i_L maxes to maximize L_X's energy. Thus, unlike a conventional SL boost, i_L should flat out in wake mode for a wake-capable SL boost as shown in Fig. 3. Consequently, wake-mode i_L profile resembles a square wave. Fig. 3 labels the R.O.'s oscillation period t_{OSC}, energizing time t_E and drain time t_D of the inductor L_X, and rise time t_R and fall time t_F of the inductor current i_L. Because t_R and t_F are small fractions of t_{OSC}, i_L's square-wave approximation is valid.

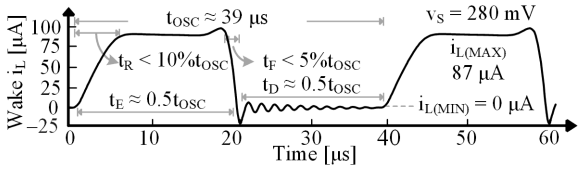

Fig. 3. Simulated inductor current profile in wake mode.

Static: In static mode, the lowest-possible v_S so the SL boost can output enough power to charge v_B to its target voltage $v_{B(TAR)}$ is called static output threshold $v_{S(O)}$ in this paper. Because v_S avails little power, the static-mode SL is in Discontinuous Conduction Mode (DCM). Thus, L_X delivers discrete energy packets to v_B, as Fig. 4 shows, where t_{SW} is the switching period of the SL boost, and conduction time t_C is the time when i_L is non-zero. To minimize $v_{S(O)}$, efficiency of the SL charger needs to be maximized. In DCM, this means maximizing the efficiency of individual energy packets. Static control sets peak inductor current $i_{L(PK)}$ to maximize each energy packet's efficiency. Across different power levels, static control fixes each energy packet and only adjusts the frequency of energy delivery. Trade-off between L_X's ohmic loss and converter's charge loss dictates the optimal $i_{L(PK)}$. This is discussed in Section II.H.

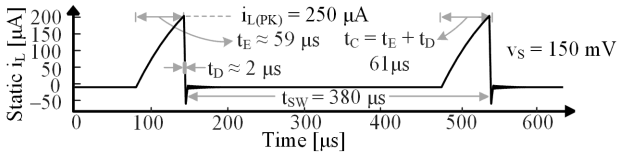

Fig. 4. Simulated inductor current profile in static mode.

Static Control: Block-level diagram of the static control is shown in Fig. 5, and v_B supplies all the blocks. As Fig. 6 shows, once v_B is higher than V_{HR}, the level detector LD_{HR}, similar as in [5], senses this event and signal v_{STATIC} trips from 0 V to v_B. $v_{STATIC(BAR)}$, which is an inverted version of v_{STATIC}, trips from v_B to 0 V. v_{STATIC} shuts off M_{OFF} in Fig. 2 once v_B reaches V_{HR}, so the R.O. and the wake driver are disabled in static mode. $v_{OS(INT)}$ is the intentional offset added to the Zero-Current Detection (ZCD) comparator CP_{ZCD}. which will be discussed in detail in Section IV.

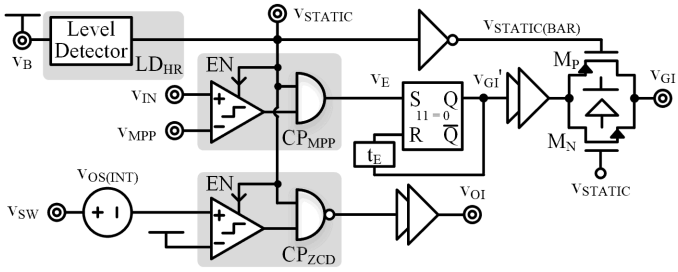

Fig. 5. Block-level diagram of the static control.

v_{STATIC} enables comparator CP_{MPP}, which regulates v_{IN} to the Maximum Power Point (MPP) voltage v_{MPP} of the energy source [15]. Once v_{IN} reaches v_{MPP}, v_E trips high to trigger M_G's gate control signal v_{GI}'. This demands L_X to draw an energy packet from v_{IN}. The delay block t_E sets the pulse-width of v_{GI}', and consequently sets $i_{L(PK)}$. A look-up table externally sets v_{MPP}. In static mode, switches M_P and M_N are closed, and the gate driver in the static control drives the ground switch M_G.

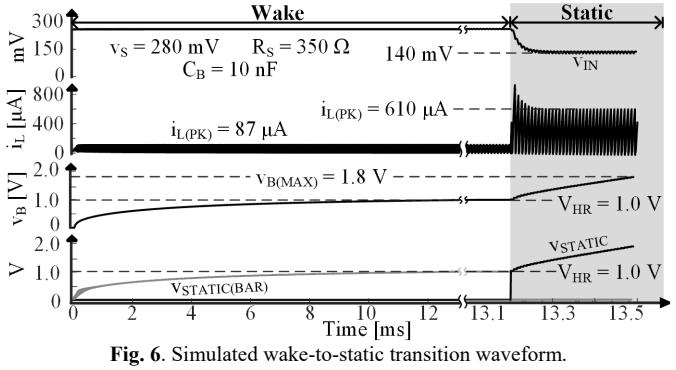

Fig. 6. Simulated wake-to-static transition waveform.

v_{STATIC} also enables comparator CP_{ZCD}, which generates v_{OI} to turn off M_B when i_L reaches zero in DCM. LD_{HR}, CP_{MPP}, CP_{ZCD} can be implemented in similar methods as in

[5]. Fig. 7 further summarizes the control sequence.

Typical Zero-Current-Detection (ZCD) comparator CP_{ZCD} adds offset voltage v_{OS} to compensate for its propagation delay, so that it turns off M_B accurately when i_L reaches 0 [10]. v_{OS} of CP_{MPP} makes v_{IN} deviate from v_{MPP}. Fortunately, near the MPP, input power P_{IN} (from the TEG to the SL boost) is less sensitive to v_{IN} (specifically, 10% error in v_{IN} causes 1% reduction in P_{IN}). Thus, there is enough margin for error. Moreover, with enough power budget, typical v_{OS} reduction techniques such as auto-zeroing, chopping, and dynamic element matching also apply. A detailed discussion on the effects of comparator offset voltage is provided in Section IV.

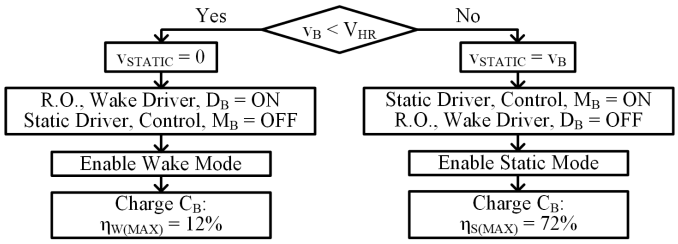

Fig. 7. Control flow chart.

B. Switched Inductor

For energy harvesting applications, SL chargers often operate in wake mode [9]. Thus, designers should select this single inductor L_X to minimize $v_{W(O)}$. For this purpose, L_X should carry the highest energy possible. In wake mode, M_G's gate-drive voltage is no higher than the 40–350-mV v_S. So, M_G is in sub-threshold and presents kilo-ohm channel resistance R_{MG}. This wake-mode R_{MG} is much higher than L_X's Equivalent Series Resistance (ESR) R_L. Thus, R_L's effect is negligible in wake mode. Therefore, for highest inductor energy, L_X is chosen to be the highest one within system volume constraint, regardless of its ESR. This design uses a 10-mH, 6 × 6 × 2.4 mm^3 inductor with 76 Ω ESR. Maximum L_X energy is:

$$E_L = \left(\frac{L_X}{2}\right) i_{L(MAX)}{}^2 = \frac{L_X}{2}\left(\frac{v_{IN}}{R_{MG}+R_L}\right)^2 \approx \frac{L_X}{2}\left(\frac{v_{IN}}{R_{MG}}\right)^2. \quad (1)$$

C. Ring Oscillator

The R.O. comprises a closed ring with odd number of inverters [3]. In wake mode, the 40–350-mV v_S supplies the R.O. The lowest v_S so a R.O. can start oscillations and prevent the SL boost from halting is called wake functional threshold $v_{W(F)}$ in this paper. P/NFETs in the R.O. are sized to minimize $v_{W(F)}$.

For this purpose, designers should size PFETs and NFETs to counter the device differences in mobility μ, sub-threshold slope factor n, and threshold voltage v_{TH} to balance their strengths [3]. The optimal ratio for PFET & NFET width W_P & W_N is [3]:

$$\frac{W_P}{W_N} = \frac{I_{S(N)}}{I_{S(P)}} = \frac{\mu_N n_N}{\mu_P n_P} \exp\left[\left(\frac{v_{TH(P)}}{n_P V_t}\right) - \left(\frac{v_{TH(N)}}{n_N V_t}\right)\right]. \quad (2)$$

To reduce oscillator loss, all FETs in the R.O. should have minimum channel length L_{MIN}. The smaller FET between the P/NFET should have minimum channel width. In this design, L_{MIN} is 1.6 μm. Because PMOS threshold $v_{TH(P)}$ is about 50 mV less than NMOS threshold $v_{TH(N)}$ in this process, therefore W_P is set to the 2.2-μm minimum channel width, and W_N is 4.3 μm.

For a R.O. with balanced P/NFETs, its duty cycle is about 50%. Therefore, t_E in Fig. 3 is about 50% t_{OSC}. For an R.O. with N_{INV} stages, t_{OSC} is about $2t_PN_{INV}$. t_P is about $2\ln2\times\tau_{INV}$ (about $1.4\times\tau_{INV}$) [16], with τ_{INV} being the RC time-constant of inverter's channel resistance R_{INV} & inter-stage capacitance C_{INV}. As mentioned in Section II.A, to maximize L_X's energy, i_L should flat out. Thus, t_E should be much longer than i_L's LR time-constant τ_{LR}. For i_L to reach 98% of its maximum, t_E must be longer than $4 \times \tau_{LR}$:

$$t_E \approx \frac{t_{OSC}}{2} = \frac{2t_PN_{INV}}{2} \approx (1.4\tau_{INV})N_{INV} >> 4\tau_{LR}, \quad (3)$$

Solving equation (3) reveals that N_{INV} must be greater than:

$$N_{INV} >> \frac{4\tau_{LR}}{t_P} = \frac{4\tau_{LR}}{1.4\tau_{INV}} \approx \frac{4(L_X/R_{MG})}{1.4(R_{INV}C_{INV})}. \quad (4)$$

To guarantee a long-enough t_E across process variation, N_{INV} is set to 25 as a design choice. Designed t_{OSC} is longer than 39 μs.

D. Ground Switch

In wake mode, v_S not only need to rise above $v_{W(F)}$ so the R.O. is functional and controls M_G, v_S also need to rise above $v_{W(O)}$ as defined in Section II.A so the SL can output net power to v_B. Designers should size M_G's width $W_{MG,}$ so that the SL achieves the lowest $v_{W(O)}$. As shown in Fig. 2, for a SL boost to output power in wake mode, L_X must charge switch-mode parasitic capacitance C_{SW} until D_B turns on. This means L_X must charge C_{SW} to one diode voltage v_D above v_B. Thus, v_{IN} must be high enough to provide L_X with enough energy to charge C_{SW}. L_X's energy E_L must be higher than:

$$E_L = \frac{L_X i_{L(MAX)}{}^2}{2} \approx \frac{L_X}{2}\left(\frac{v_{IN}}{R_{MG}}\right)^2 \geq E_{CSW} = \frac{C_{SW}}{2}(v_B + v_D)^2. \quad (5)$$

To reduce ohmic loss, M_G has minimum channel length L_{MIN}. A wider M_G has less channel resistance R_{MG} and allows L_X to hold a higher current and more energy. But a wider M_G has higher drain-bulk capacitance C_{DB} and needs more energy to charge C_{SW}. Since E_L rises quadratically with $i_{L(MAX)}$ and W_{MG}, but C_{DB} only rises linearly with W_{MG}, so as W_{MG} rises the lowest v_{IN} required to provide L_X with enough energy reduces. Solving equation (5) reveals that $v_{IN(MIN)}$ drops with $W_{MG}{}^{-0.5}$:

$$v_{IN(MIN)} = (v_B + v_D)R_{MG}\sqrt{\frac{C_{SW}}{L_X}} \approx (v_B + v_D)R_{MG}\sqrt{\frac{C_{DB}}{L_X}} \equiv \frac{k_{VIN}}{\sqrt{W_{MG}}}, \quad (6)$$

where k_{VIN} is a coefficient that lumps all factors other than W_{MG} together. k_{VIN} is:

$$k_{VIN} = (v_B + v_D)\rho_{MG}L_{MIN}\sqrt{\frac{C_{DB}'}{L_X}}, \quad (7)$$

where ρ_{MG} is M_G's channel sheet resistance, and C_{DB}' is the C_{DB} per channel width. Consequently, the lowest input voltage $v_{IN(MIN)}$ is inversely-proportional to the square-root of W_{MG}.

Most energy sources have significant source resistance R_S. For tiny TEGs, R_S can be 180–350 Ω [5, 8, 20]. Moreover, R_S can drop 14–127 mV in wake mode [20]. Thus, v_{RS} (labeled in Fig. 1) is significant for a 40–350-mV energy source. As shown in Fig. 2, a larger M_G demands a higher wake driver current i_{DRV} to drive its gate, and thus incurs more v_{RS} drop. Approximately, average inductor current $i_{L(AVG)}$ and average wake driver current $i_{DRV(AVG)}$ flows through R_S and creates v_{RS} drop. Wake driver charges M_G's gate capacitance C_{MG} per t_{OSC},

so $i_{DRV(AVG)}$ is roughly M_G's gate charge Q_{CMG} per t_{OSC}. Wake mode i_L resembles a square wave as Fig. 3 shows, thus $i_{L(AVG)}$ is roughly the t_E/t_{OSC} fraction of $i_{L(MAX)}$. Therefore, v_{RS} is:

$$\begin{aligned} v_{RS} &\approx R_S\left(i_{DRV(AVG)} + i_{L(AVG)}\right) \\ &\approx R_S\left[\left(\frac{Q_{CMG}}{t_{OSC}}\right) + i_{L(MAX)}\left(\frac{t_E}{t_{OSC}}\right)\right] \\ &\approx R_S\left[\frac{C_{MG}"L_{MIN}W_{MG}v_{IN(MIN)}}{t_{OSC}} + \frac{v_{IN(MIN)}}{R_{MG}}\left(\frac{t_E}{t_{OSC}}\right)\right], \\ &\equiv k_{VRS}\sqrt{W_{MG}} \end{aligned} \tag{8}$$

where $C_{MG}"$ is C_{MG} per unit channel area. Since $v_{IN(MIN)}$ is inversely-proportional to $W_{MG}^{0.5}$, so $i_{DRV(AVG)}$ is proportional to $W_{MG}^{0.5}$. Also, since R_{MG} is inversely-proportional to W_{MG}, so $i_{L(MAX)}$ and $i_{L(AVG)}$ are roughly proportional to $W_{MG}^{0.5}$. As a result, v_{RS} is also proportional to $W_{MG}^{0.5}$ and k_{VRS} is a coefficient that lumps all factors other than W_{MG}. k_{VRS} is:

$$k_{VRS} = \frac{R_S k_{VIN}}{t_{OSC}}\left(C_{MG}"L_{MIN} + \frac{t_E}{\rho_{MG}L_{MIN}}\right), \tag{9}$$

Therefore $v_{W(O)}$, which refers to the source voltage v_S, thus is:

$$v_{W(O)} = v_{IN(MIN)} + v_{RS} = \frac{k_{VIN}}{\sqrt{W_{MG}}} + k_{VRS}\sqrt{W_{MG}}\ . \tag{10}$$

Rising W_{MG} reduces the lowest v_{IN} required to energize L_X and charge C_{SW}, but this increases v_{RS}. To minimize $v_{W(O)}$, W_{MG} should be optimized so that low v_{IN} can provide L_X with enough energy, and v_{RS} is also not prohibitively high. As a result, optimal width W_{MG} (denoted as W_{MG}') is derived as:

$$W_{MG}' = \frac{k_{VIN}}{k_{VRS}}\ . \tag{11}$$

By substituting k_{VIN} and k_{VRS} expressed in (7) and (9) into (11), the calculated and designed W_{MG}' is 24 mm.

E. Output Switch

The output switch consists of an asynchronous diode D_B and a synchronous PMOS M_B in Fig. 2. Asynchronous diode D_B only operates in wake mode to steer i_L into v_B without feedback control. Synchronous PMOS M_B only operates in static mode and is turned off by the static control when i_L reaches zero.

Asynchronous Diode: PMOS threshold voltage $v_{TH(P)}$ (i.e., 300–400 mV) can be lower than the voltage v_D dropped across a junction diode (i.e., 600–700 mV). If PMOS with a $v_{TH(P)}$ that is lower than v_D is available, a diode-connected PMOS D_B in Fig. 2 can be used as the output diode in wake mode. This reduces D_B's forward voltage drop and ohmic loss. Leakage loss P_{LK} is non-negligible in wake mode. When a switch is off, P_{LK} scales quadratically with the voltage v_{LK} across the switch. For a low-v_{IN} boost, M_G's v_{LK} is less than the 40–350-mV v_S while D_B's v_{LK} can be close to the 1.0–1.8-V v_B, which is 2.9–45× higher. Thus, minimizing D_B's leakage is the most crucial design concern, and D_B's width W_{DB} should be minimum:

$$W_{DB} \equiv W_{MIN}\ . \tag{12}$$

Synchronous PMOS: In static mode, high v_B supplies gate drivers, so M_B can be fully turned on and its channel resistance R_{MB} is much smaller than the tiny L_X's high ESR. So, M_B's conduction loss is negligible compared to R_L's loss P_{RL}. Moreover, M_B's width W_{MB} should be optimally sized so that its loss is minimum. M_B's loss consists of ohmic loss $P_{MB(R)}$ and gate-drive loss $P_{MB(C)}$. $P_{MB(R)}$ is Root-Mean-Square (RMS) current squared times R_{MB}, which is inversely proportional to W_{MB}. $P_{MB(C)}$ scales with W_{MB}:

$$P_{MB(R)} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 R_{MB}\left(\frac{t_D}{t_{SW}}\right) \equiv \frac{k_{MB(R)}}{W_{MB}}\ , \tag{13}$$

$$P_{MB(C)} = C_{G(MB)}v_B{}^2 f_{SW} \equiv k_{MB(C)}W_{MB}\ , \tag{14}$$

where t_D is the drain time as labeled in Fig. 4 and $C_{G(MB)}$ is M_B's gate capacitance. $k_{MB(R)}$ and $k_{MB(C)}$ are W_{MB}-independent coefficients that lump all factors other than W_{MB} together:

$$k_{MB(R)} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 \rho_{MB}L_{MIN}\left(\frac{t_D}{t_{SW}}\right), \tag{15}$$

$$k_{MB(C)} = C_{G(MB)}"L_{MIN}v_B{}^2 f_{SW}\ , \tag{16}$$

where ρ_{MB} is M_B's channel sheet resistance and $C_{G(MB)}"$ is $C_{G(MB)}$ per channel area. So, for an optimally sized M_B, its conduction loss should be equal to its gate-drive loss [10]. The minimum loss P_{MB}' is:

$$P_{MB}' = P_{MB(R)}' + P_{MB(C)}' = 2\sqrt{k_{MB(R)}k_{MB(C)}}\ , \tag{17}$$

where $P_{MB(R)}'$ and $P_{MB(C)}'$ are the optimal $P_{MB(R)}$ and $P_{MB(C)}$, respectively. The optimal width W_{MB}' is:

$$W_{MB}' = \sqrt{\frac{k_{MB(R)}}{k_{MB(C)}}}\ . \tag{18}$$

For an optimally sized M_B, $P_{MB(R)}$ equals $P_{MB(C)}$ and both are negligible compared to P_{RL}. So, M_B's total loss is negligible compared to P_{RL}. In this design, optimal W_{MB} is 160 µm.

F. Gate Drivers

To minimize propagation delay, gate driver's optimal scaling factor A_X (denoted as A_X') is $e \approx 2.7$ [16]. However, designing at the optimal scaling factor increases power consumption. Thus, A_X is greater than e in this design:

$$A_X = \frac{W_{DRV(i)}}{W_{DRV(i-1)}} \geq A_X' = e\ . \tag{19}$$

As a design choice, A_X for sub-threshold wake-mode driver is set to 5 to achieve acceptable rise and fall time. A_X for static-mode drivers in Fig. 5 is set to 10 to reduce power consumption. M_G's static driver has 4 stages, and M_B's static driver has 2 stages.

G. Wake Circuit Disabling Switch

Switch M_{OFF}'s purpose is to connect R.O. and wake-mode driver to v_{IN} in wake mode and disconnects them from v_{IN} in static mode. To make a solid connection in wake mode, v_{RO} in Fig. 2 must be close to v_{IN}. This means M_{OFF}'s wake-mode resistance $R_{MOFF(W)}$ should be much less than the parallel combination of R.O.'s equivalent resistance R_{RO} and wake-mode driver's equivalent resistance R_{DRV}. In wake mode, LD_{HR} sets M_{OFF}'s gate voltage to ground, and $R_{MOFF(W)}$ should be much less than:

$$R_{MOFF(W)} = \rho_{MOFF(W)}\left(\frac{L_{MIN}}{W_{MOFF}}\right) << R_{RO}\,||\,R_{DRV}\ , \tag{20}$$

where $\rho_{MOFF(W)}$ is M_{OFF}'s channel sheet resistance in wake mode when its v_{SG} equals v_{IN}, and W_{MOFF} is M_{OFF}'s channel width. Thus, W_{MOFF} should be much larger than:

$$W_{MOFF} >> \frac{\rho_{MOFF(W)}L_{MIN}}{R_{RO}\,||\,R_{DRV}}\ . \tag{21}$$

R_{RO} is approximately the parallel combination of N_{INV} inverter

stages, therefore R_{RO} is approximately:

$$R_{RO} \approx \frac{R_{INV}}{N_{INV}}. \quad (22)$$

R_{DRV} is approximately the parallel combination of inverters whose widths are scaled by A_X, therefore R_{DRV} is roughly:

$$R_{DRV} \approx \frac{R_{INV}}{1+A_X+A_X{}^2+\cdots+A_X{}^{(N_{DRV}-1)}}, \quad (23)$$

where N_{DRV} denotes the number of stages in the wake driver.

Similarly, to disconnect the R.O. and wake-mode driver from v_{IN} in static mode, v_{RO} must be very close to ground. This means M_{OFF}'s static-mode resistance $R_{MOFF(S)}$ needs to be much higher than ($R_{RO}||R_{DRV}$). In static mode, LD_{HR} sets M_{OFF}'s gate voltage to v_B, which is no less than V_{HR}. Therefore, $R_{MOFF(S)}$ should be much higher than:

$$R_{MOFF(S)} = \rho_{MOFF(S)}\left(\frac{L_{MIN}}{W_{MOFF}}\right) >> R_{RO}||R_{DRV}, \quad (24)$$

where $\rho_{MOFF(S)}$ is M_{OFF}'s channel sheet resistance in static mode when its v_{SG} equals (v_{IN} –V_{HR}). This means W_{MOFF} should be much smaller than:

$$W_{MOFF} << \frac{\rho_{MOFF(S)} L_{MIN}}{R_{RO}||R_{DRV}}. \quad (25)$$

In this design, W_{MOFF}'s calculated limits are 9.2 μm << W_{MOFF} << 3.2×10^4 m. W_{MOFF}'s upper limit is extremely large since in static mode M_{OFF} has negative v_{SG} and thus extremely high $\rho_{MOFF(S)}$ [22]. Unfortunately, a large W_{MOFF} significantly rises silicon area and thus increases cost. Thus, the tradeoff here is to design a large-enough M_{OFF} without drastically increasing silicon area. Since the largest MOSFET in this design is M_G, which is 24-mm wide as Section II.D. justifies, M_{OFF} is chosen to be 10× smaller than M_G to prevent significantly increasing total silicon area. Thus, to keep v_{RO} very close to v_{IN} in wake mode while not significantly increasing silicon area, W_{MOFF} is set to 2 mm as a design choice.

H. Static-Mode Peak Inductor Current

Static control sets t_E and $i_{L(PK)}$ so individual energy packets are the most efficient [10]. This translates to setting $i_{L(PK)}$ so each energy transfer induces the lowest fractional loss. For a SL boost, power losses mainly consist of ohmic loss P_R caused by R_L and power switches, and charge loss P_C caused by driving these power switches and charging C_{SW}. i_{DS}-v_{DS} overlap loss is negligible because $i_{L(PK)}$ is at μA-level and the i_{DS}-v_{DS} overlapping time can be as short as 14 ns.

Since in static mode power switches can be fully turned on, their channel resistances are negligible compared to the 76-Ω ESR R_L. Thus, MOSFET ohmic loss is negligible compared to ESR loss P_{RL}, and the fractional ohmic loss σ_R is:

$$\sigma_R = \frac{P_R}{P_{IN}} \approx \frac{P_{RL}}{v_{IN} i_{L(AVG)}} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 \frac{R_L t_C f_{SW}}{v_{IN}\left(0.5 i_{L(PK)} t_C f_{SW}\right)} \equiv k_R i_{L(PK)}, \quad (26)$$

where t_C is the inductor's conduction time as labeled in Fig. 4, f_{SW} is the converter's switching frequency, and k_R is the $i_{L(PK)}$-independent coefficient that lumps all factors other than $i_{L(PK)}$:

$$k_R = \frac{2R_L}{3v_{IN}}, \quad (27)$$

From (26), σ_R is proportional to $i_{L(PK)}$. For the same L_X, increasing $i_{L(PK)}$ requires proportionally longer t_C. Thus, t_C is proportional to $i_{L(PK)}$. Because charge loss P_C doesn't scale with $i_{L(PK)}$, fractional charge loss σ_C is inversely proportional to $i_{L(PK)}{}^2$, as shown below.

$$\sigma_C = \frac{P_C}{P_{IN}} \approx \frac{P_{MG(C)}+P_{CSW}}{v_{IN} i_{L(AVG)}} = \frac{\left(C_{MG(G)}+0.5C_{SW}\right)v_B{}^2 f_{SW}}{v_{IN}\left(0.5 i_{L(PK)} t_C f_{SW}\right)} \equiv \frac{k_C}{i_{L(PK)}{}^2}, \quad (28)$$

where $P_{MG(C)}$ is M_G's gate-drive loss, $C_{MG(G)}$ is M_G's gate capacitance, and k_C is a $i_{L(PK)}$-independent coefficient that lumps all factors other than $i_{L(PK)}$. For v_{IN} that's much less than v_B (which is typical for TEG harvesters), k_C is approximately:

$$k_C = \frac{2\left(C_{MG(G)}+0.5C_{SW}\right)v_B\left(v_B-v_{IN}\right)}{L_X} \approx \frac{2\left(C_{MG(G)}+0.5C_{SW}\right)v_B{}^2}{L_X}, \quad (29)$$

Because when $i_{L(PK)}$ rises, σ_R rises linearly and σ_C drops quadratically, an optimal $i_{L(PK)}$ (denoted as $i_{L(PK)}'$) exists so the total fractional loss is minimized. $i_{L(PK)}'$ is:

$$i_{L(PK)}' = \left(\frac{2k_C}{k_R}\right)^{\frac{1}{3}}. \quad (30)$$

In this design, $i_{L(PK)}'$ is about 205 μA when v_S is 40 mV.

III. Experimental Validation

A. Prototype

A 1.6-μm CMOS wake-capable single-inductor SL boost charger prototype experimentally validates the theory and the lowest-possible v_S both in wake and static mode. The prototype is tested with off-chip LPS6225 inductors that measure 1–10 mH with 6–76 Ω ESR. Inductor volume is 6.0 × 6.0 × 2.4 mm^3, which is suitable for millimeter-scale IoT applications.

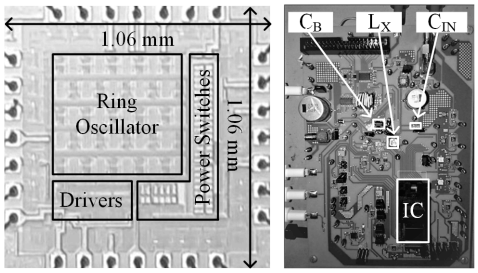

Fig. 8. 1.6-μm CMOS die and printed circuit board (PCB) test setup.

The 1.6-μm CMOS die in Fig. 8 occupies an active area of 640 × 635 $μm^2$. For testing purposes, a 1-μF on-board capacitor C_B serves as the battery v_B in Fig. 1. A 1-μF capacitor C_{IN} is placed at v_{IN} to suppress v_{IN}'s ripple. No capacitor is placed at v_S. For testing purposes only, to measure the minimum v_S, an on-board voltage source emulates v_S and an on-board series resistor sets R_S. R_S is chosen to be 350 Ω, which is typical for millimeter-scale (4.2 × 3.3 mm^2) TEGs [8]. The validity of emulating TEG with a voltage source and a series resistance is justified below.

A TEG is a transducer that outputs electrical voltage across its terminals whenever a temperature difference ΔT is present across it. The physical effect that converts thermal energy into electricity is called Seebeck effect [17, 28–29]. When the current drawn from the TEG increases, its terminal voltage v_{IN} (labelled in Fig. 1) reduces approximately linearly with the drawn current [17, 30]. Therefore, a source resistance R_S shown in Fig. 1 is used to model this linear reduction in v_{IN}. When no current is drawn from the TEG, the TEG is open-circuited, and v_{IN} equals TEG's open-circuit source voltage v_S shown in Fig. 1. According to Seebeck effect, v_S is proportional to ΔT. Therefore, majority of the literatures model TEG as a voltage source v_S in series with a series

resistance R_S [5, 12, 17, 20, 29, 31], like the grey block labelled "TEG Model" in Fig. 1.

Because the coupling between thermal energy domain and electricity domain could be as low as 2%, even when the maximum electrical power is drawn from the TEG, ΔT hardly reduces [30]. As a result, v_S hardly reduces even if maximum electrical power is drawn from it. Therefore, ΔT & the v_S generated by the TEG hardly reacts to the energy-harvesting circuit [30, 32]. Due to this reason, many literatures emulate the TEG using a voltage source and a series resistance to validate their energy harvester prototype [5, 6, 9, 12, 31].

The purpose of this paper is to theorize and experimentally verify the fundamental limitations of a SL boost charger, but is not system integration. Therefore, an off-chip field programmable gate array (FPGA) functions as the LD_{HR}, CP_{MPP}, CP_{ZCD}, SR latch, and delay block t_E in Fig. 5. The control in Fig. 5–7 can be integrated on-chip using CMOS in similar fashion as in [5, 10, 15] and can consume 132 nW in total. Detailed power breakdown and discussion on the impact of controller power consumption is provided in Section IV.

B. Functionality

Measured v_S, v_{IN}, and R.O. waveform v_{OSC} are shown in Fig. 9. Oscillations start when v_S rises above $v_{W(F)}$. The measured $v_{W(F)}$ is about 49 mV. v_S supplies the R.O. and as v_S rises, oscillation frequency f_{OSC} rises. So, the R.O. starts drawing more current from v_S. Thus, as v_S rises, v_{IN} drops from v_S. An inset plot shows the oscillation waveform in detail when v_S is 165 mV.

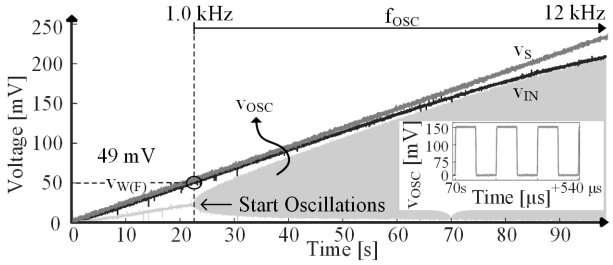

Fig. 9. Measured v_S, v_{IN} and ring oscillator's oscillation waveform v_{OSC}.

Measured f_{OSC} across v_S is shown in Fig. 10. At first, the R.O. is in sub-threshold. Thus, inverter's channel resistance R_{INV} drops exponentially as v_S rises, and therefore f_{OSC} rises exponentially. When v_S is above MOS threshold voltage, R_{INV} is inversely proportional to v_S. Thus, f_{OSC} rises linearly. Oscillation period t_{OSC} is no shorter than 39 µs. This is long enough to maximally energize L_X as discussed in Section II.B.

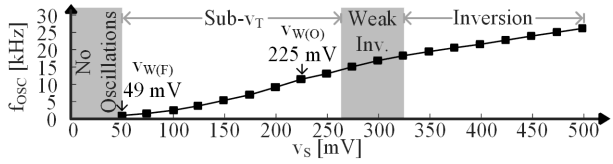

Fig. 10. Measured oscillation frequency f_{OSC} across v_S.

Measured i_L in wake mode is shown in Fig. 11. When v_S is 285 mV, t_{OSC} of the R.O. is 58 µs and energizing time t_E is 30 µs. Because P/NMOS in the R.O. are balanced, t_E is about 50% t_{OSC}. t_E is long enough to let i_L max out, and measured wake i_L resembles a square wave. The maximum $i_{L(PK)}$ is 90 µA. Because i_L must charge C_{SW} to (v_B + v_D) before the SL can output energy to v_B, at the instance when L_X is drained, C_{SW} is still pre-charged to (v_B + v_D) and therefore possesses left-over energy. Since at this moment v_{SW} is higher than v_{IN}, C_{SW}'s left-over energy drains into L_X so i_L is negative (flows from v_{SW} to v_{IN}) and v_{SW} discharges. When v_{SW} drops lower than v_{IN}, i_L starts to rise. At half resonance-period t_{LC}, i_L becomes positive (flows from v_{IN} to v_{SW}) and therefore starts to charge C_{SW} again. This resonance creates ringing in i_L waveform [21] and diminishes when ohmic losses (i.e., R_L) burns all left-over energy. t_{LC} is approximately:

$$t_{LC} \approx 2\pi\sqrt{L_X C_{SW}} \,. \tag{31}$$

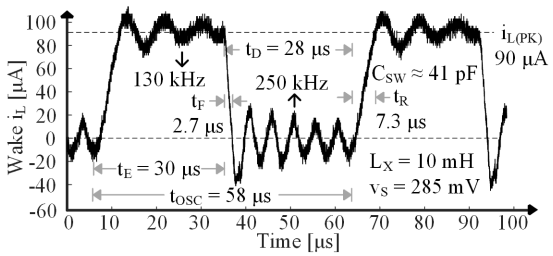

Fig. 11. Measured inductor current profile during wake mode.

Measured static mode i_L is shown in Fig. 12. In static mode, SL boost operates in DCM. L_X's 76-Ω ESR current-limits i_L, this is why i_L is curly. In static mode, static control implemented in the off-chip FPGA sets t_E and consequently sets $i_{L(PK)}$. It also turns the synchronous switch M_B off when i_L reaches 0.

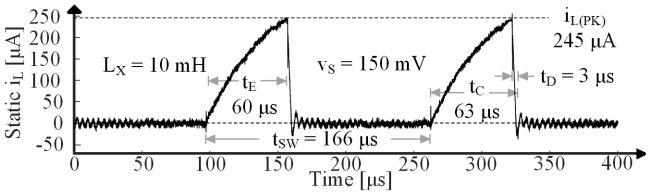

Fig. 12. Measured inductor current profile during static mode.

Measured v_B charging profile across both wake and static mode is captured in Fig. 13. Due to the lack of high gate-drive voltage in wake mode, M_G is in sub-threshold and the SL boost charges v_B slowly. When v_B reaches the headroom voltage V_{HR}, this high v_B starts supplying gate drivers so the SL boost enters static mode and v_B rises quickly. Equivalent charging current i_{CHG} is an equivalent constant current that charges the same battery capacitor C_B across the same voltage over the same time, as defined in [20]. Since wake time t_W changes with C_B and V_{HR}, this i_{CHG} normalizes t_W with C_B and V_{HR}. Fig. 13 shows that the wake-mode SL charges a 1-µF C_B to 0.87 V from 324 ms to 3.55 s. This translates to a 270-nA i_{CHG} from 324 ms to 3.55 s. Similarly, wake-mode i_{CHG} from 3.55 s to 9.03 s is 18 nA and static-mode i_{CHG} is 2.3 µA. Wake-mode i_{CHG} is much less than static-mode i_{CHG} because sub-threshold M_G is very resistive. In static mode, all power switches can be fully turned on and the 2.3-µA i_{CHG} charges C_B fast and efficiently.

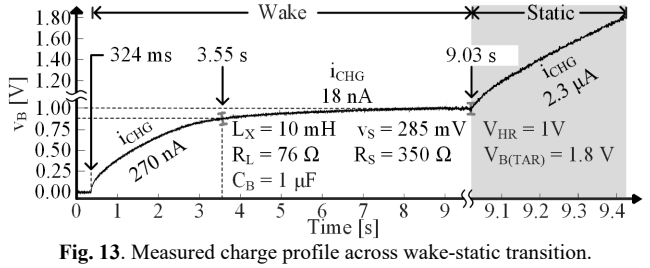

Fig. 13. Measured charge profile across wake-static transition.

The fundamental requirement to wake the system is when P_{IN} is higher than total power loss P_{LOSS}, therefore the remaining

power can reach and charge v_B. The minimum v_S such that $P_{IN} > P_{LOSS}$ is $v_{W(O)}$. Controller shown in Fig. 6 and Fig. 7 automatically shifts the SL boost to wake mode once $v_B < V_{HR}$, and thus ensures correct wake up of the system.

Directly charging a real battery would result in excessively long t_W. However, the purpose of this paper is to theorize and experimentally validate the fundamental voltage limits of a SL boost charger, but not to reduce t_W. In practice, avoiding charging a real battery directly and charge a small capacitor as a temporary supply instead can significantly reduce t_W [5].

C. Performance

SL boost cannot charge v_B to an infinite voltage. The highest voltage v_B can reach is called $v_{B(MAX)}$. Fig. 14 shows measured $v_{B(MAX)}$ across v_S in wake mode. When v_S is below 225 mV, $v_{B(MAX)}$ is approximately v_S because D_B's leakage current charges v_B to v_S over time. However, the wake-mode SL cannot boost v_B above v_S. When v_S is above 225 mV, the wake-mode SL starts to boost v_B above v_S. This means SL boost can output net power to charge the battery. Therefore, wake output threshold $v_{W(O)}$ is 225 mV. When v_S is beyond 285 mV, the SL boost can charge v_B beyond headroom voltage V_{HR}. This v_S is called the wake headroom threshold $v_{W(HR)}$ in this paper. With such v_S, SL boost can enter static mode and transfer energy efficiently.

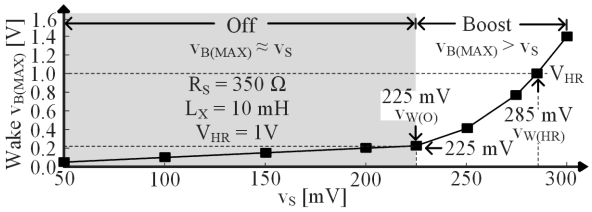

Fig. 14. Measured wake-mode $v_{B(MAX)}$ across v_S.

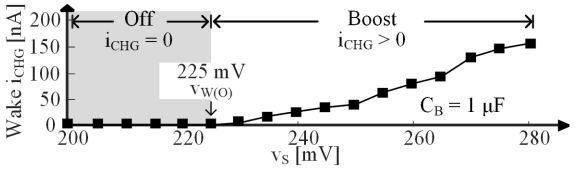

Fig. 15. Measured wake-mode i_{CHG} across v_S.

Measured wake-mode i_{CHG} across v_S is shown in Fig. 15. In wake-mode, i_{CHG} is the equivalent current that the boost outputs to charge C_B above v_S. When v_S is below 225 mV, the boost is off and never charges v_B above v_S, so i_{CHG} is 0. When v_S is above 225 mV, SL boost starts to deliver net power to C_B and charge v_B above v_S, so i_{CHG} rises above 0. v_S avails more power as it rises, so the SL boost outputs more power to v_B and i_{CHG} rises.

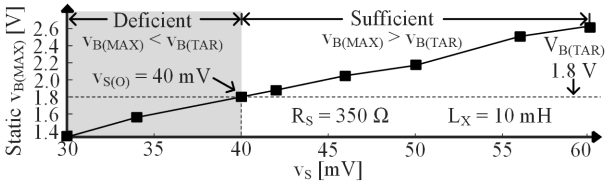

Fig. 16. Measured static-mode $v_{B(MAX)}$ across v_S.

Measured $v_{B(MAX)}$ across v_S in static mode is shown in Fig. 16. When v_S is below 40 mV, the available power is deficient, and the boost cannot charge v_B to its target voltage $v_{B(TAR)}$. This design sets $v_{B(TAR)}$ to 1.8 V because it is suitable for most IoT systems [13]–[14]. When v_S rises above 40 mV, SL boost can output sufficient power to fully charge v_B to the target voltage. So, the measured static output threshold $v_{S(O)}$ is 40 mV.

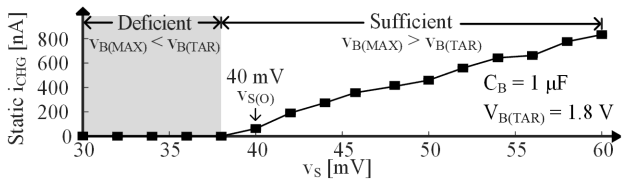

Fig. 17. Measured static-mode i_{CHG} across v_S.

Measured static-mode i_{CHG} across v_S is shown in Fig. 17. In static mode, i_{CHG} is the equivalent current that the boost outputs to charge C_B to $v_{B(TAR)}$. When v_S is below 40 mV, the SL boost never charges v_B to 1.8 V, so i_{CHG} is 0. When v_S is above 40 mV, the SL boost can fully charge v_B, and consequently, i_{CHG} rises above 0. Likewise, as v_S rises and avails more power, the SL boost outputs more power to v_B. Thus, i_{CHG} rises with v_S.

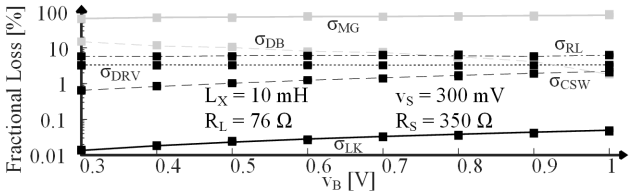

Fig. 18. Measured wake-mode fractional loss across v_B.

Measured fractional loss (labeled as σ) of the SL boost across v_B in wake mode is shown in Fig. 18. In wake mode, M_G is in sub-threshold and R_{MG} measures 1.1 kΩ. M_G's fractional loss σ_{MG} is therefore 69–81% in wake mode, which means M_G's loss overwhelms all other losses. This is why designers must optimally size M_G to minimize $v_{W(O)}$. Output diode D_B has minimum width, so its fractional leakage loss σ_{LK} is less than 0.1% and is negligible.

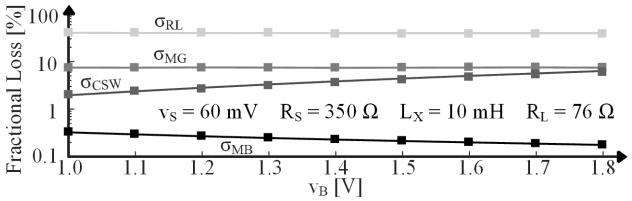

Fig. 19. Measured static-mode fractional loss across v_B.

Measured fractional loss of the SL boost across v_B in static mode is shown in Fig. 19. In static mode, tiny L_X is the most lossy component due to its high ESR R_L. R_L's fractional loss σ_{RL} is 36–42% and overwhelms all other losses. This is why designers must carefully manage $i_{L(PK)}$ to balance R_L's ohmic loss according to Section II.H. Output switch M_B's fractional loss σ_{MB} is less than 0.4%. Because M_B has optimal width, its loss is proved negligible according to Section II.E.

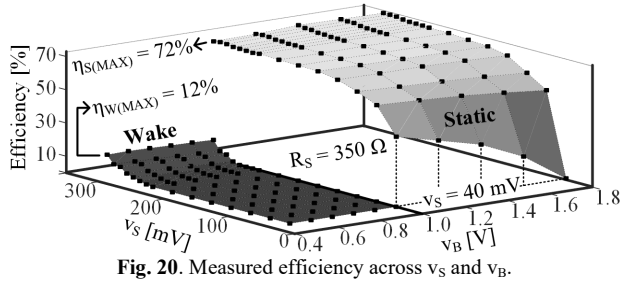

Fig. 20. Measured efficiency across v_S and v_B.

Measured efficiency η_C across v_S and v_B is shown in Fig. 20, and Table I. details measured power loss, energy loss per cycle, & fractional loss. In wake mode, sub-threshold M_G is the most lossy and η_C is less than 12%. In static mode, M_G also

contributes about 7.7% fractional loss. This is mainly because W_{MG} is large, so M_G consumes high charge loss $P_{MG(C)}$. This is also why $i_{L(PK)}$' should be carefully designed so it balances $P_{MG(C)}$ with P_R as Section II.H. describes. Maximum static mode efficiency $\eta_{S(MAX)}$ can reach 72%. This justifies that the target of wake-mode design is not high efficiency, but to minimize $v_{W(O)}$ so the SL charger can transit out of wake mode with the lowest-possible v_S.

TABLE I: LOSS BREAKDOWN AND EFFICIENCY

	Wake: v_S = 300 mV, v_B = 0.5 V			Static: v_S = 60 mV, v_B = 1.8 V		
	P_{LOSS}	E_{LOSS}	σ	P_{LOSS}	E_{LOSS}	σ
R_L	1.4 µW	88 pJ/Cycle	6.0%	830 nW	414 pJ/Cycle	40%
M_G	17 µW	1.1 nJ/Cycle	73%	160 nW	80 pJ/Cycle	7.7%
C_{SW}	240 nW	15 pJ/Cycle	1.0%	130 nW	67 pJ/Cycle	6.4%
D_B	2.4 µW	150 pJ/Cycle	10%	–	–	–
M_B	–	–	–	4 nW	2 pJ/Cycle	0.2%
Osc.	770 nW	48 pJ/Cycle	3.3%	–	–	–
η_C	**7%**	**Total σ**	**93%**	**46%**	**Total σ**	**54%**

D. Design

This subsection experimentally validates the closed-form design expressions from Section II.B to Section II.H. Extensive measurements across R.O.'s W_N and W_P, L_X, W_{MG}, and $i_{L(PK)}$ validates the design theory and proves that this design achieves the lowest-possible v_S for SL converters. It is worth highlighting that, it is for testing purposes only that an externally-reconfigurable CMOS chip is prototyped to experimentally validate the proposed theory across all design variables (i.e., W_P, W_N, W_{MG}, L_X, $i_{L(PK)}$, f_{SW}). Measurement data shown in Figs. 21 & 22 are gathered by first externally reconfiguring & setting these above-mentioned design variables and then making measurements. The purpose of Fig. 21 & 22 is to show that the theory is valid, since the fundamental contribution of this paper is proposing and experimentally verifying the theory, and it is the theory that predicts the optimal design. With the help of the proposed theory, designers can first calculate the optimal design variables, and then make a specific (fixed) design at these optimal values provided by the theory. The design insight and guidance proposed, theorized, and validated here is the main purpose and contribution of this paper.

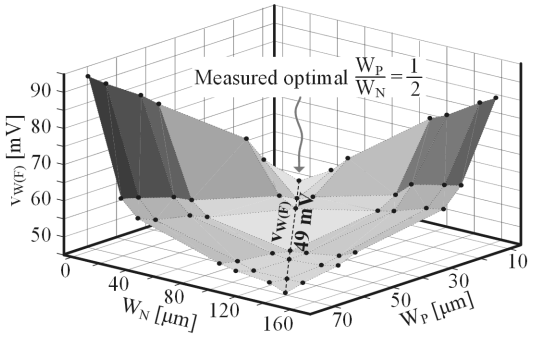

Fig. 21. Measured wake functional threshold $v_{W(F)}$ across W_N & W_P.

Ring Oscillator: Fig. 21 shows measured $v_{W(F)}$ across R.O.'s PMOS width W_P and NMOS width W_N. When PMOS and NMOS strengths are balanced, each inverter in the oscillator requires the lowest v_S to trip. Thus, the R.O. requires the lowest $v_{W(F)}$ to start oscillating [3]. $v_{W(F)}$ only depends on the ratio of W_P and W_N, but does not depend on their actual values. Thus, keeping W_P/W_N optimized and minimize actual transistor sizes can reduce power consumption and keep $v_{W(F)}$ the same. In this process, NMOS threshold voltage (about 320 mV) is about 50 mV higher than PMOS threshold voltage (about 275 mV). Since NMOS is weaker, the optimal NMOS size is approximately twice the optimal PMOS size.

Energy-Transfer Inductor L_X: Fig. 22 shows measured $v_{W(HR)}$ across L_X and M_G's width W_{MG}. V_{HR} can be as low as 1 V, which is enough to supply low-voltage CMOS controllers [12]. A higher L_X holds more energy to charge switch-node capacitance C_{SW}. This is why $v_{W(HR)}$ drops from 360 mV to 285 mV as L_X increases. The highest inductance available in the LPS6225 series is 10 mH. Relieving volume constraints and choosing a higher L_X can further reduce $v_{W(HR)}$.

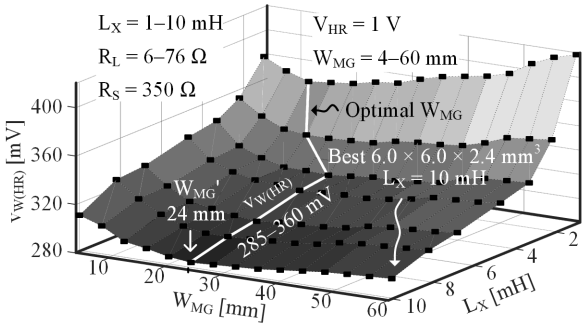

Fig. 22. Measured wake headroom threshold $v_{W(HR)}$ across W_{MG} & L_X.

Ground Switch M_G: Sizing W_{MG} is critical for minimizing wake thresholds, as Fig. 22 shows. Rising W_{MG} increases $i_{L(MAX)}$ so L_X holds more energy. But as discussed in Section II.D, W_{MG} cannot be prohibitively wide because then it requires too much i_{DRV} and causes an extensive v_{RS} voltage drop. With the best 10-mH L_X for a given volume, the measured optimal W_{MG} is 24 mm.

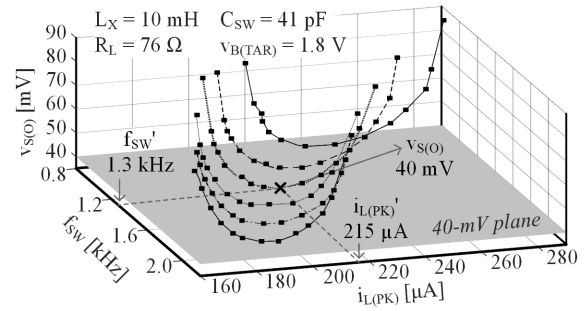

Fig. 23. Measured static output threshold $v_{S(O)}$ across $i_{L(PK)}$ & f_{SW}.

Static $i_{L(PK)}$ and f_{SW}: Fig. 23 shows measured $v_{S(O)}$ across $i_{L(PK)}$ and f_{SW}. The delay block t_E shown in Fig. 5 sets the pulse-width of v_{GI}', which, sets the energizing time of L_X and consequently sets $i_{L(PK)}$. t_E & f_{SW} can be externally changed in order to measure across different $i_{L(PK)}$ & f_{SW}. Similarly, measurement data shown in Fig. 23 are gathered by externally reconfiguring & setting t_E & f_{SW} first and then making measurements. The purpose of Fig. 23 is to experimentally show that the proposed theory is valid, since the major contribution of this paper is proposing and experimentally verifying the theory. With the help of the theory, designers can calculate $i_{L(PK)}$' first, infer the optimal t_E & f_{SW} next, and then make a specific design at the optimal operating point.

Measured $v_{S(O)}$ is 40 mV, and the corresponding measured optimal $i_{L(PK)}$ is about 215 µA, which closely agrees with the derived result. Likewise, relieving volume constraints and choosing a L_X with less R_L can further reduce $v_{S(O)}$.

Effect of PVT variations: CMOS process variation affects MOS threshold voltages v_{TH} and transconductance parameter $K_{N/P} = \mu_{N/P}C_{OX}$. Variations in v_{TH} and $K_{N/P}$ creates an imbalance in the strength of P/NMOS in the R.O. as indicated by equation (2), and consequently increases $v_{W(F)}$. v_{TH} and $K_{N/P}$ variations also affects R_{MG}, which also affects ohmic loss and may increase or decrease $v_{W(O)}$ and $v_{W(HR)}$. Table II. shows simulated $v_{W(F)}$, $v_{W(O)}$, $v_{W(HR)}$, and $v_{S(O)}$ across process corners.

TABLE II: SIMULATED $V_{W(F)}$, $V_{W(O)}$, $V_{W(HR)}$, AND $V_{S(O)}$ ACROSS CORNERS

Process Corner	TT	SS	SF	FS	FF
$v_{W(F)}$	43 mV	64 mV	147 mV	170 mV	91 mV
$v_{W(O)}$	203 mV	274 mV	261 mV	192 mV	173 mV
$v_{W(HR)}$	270 mV	336 mV	325 mV	247 mV	232 mV
$v_{S(O)}$	36 mV	37 mV	37 mV	36 mV	34 mV

$v_{W(F)}$ is much lower than $v_{W(O)}$ and $v_{W(HR)}$ across corners. This means when v_S reaches $v_{W(O)}$ or $v_{W(HR)}$, the R.O. is already oscillating in wake mode. Thus, PVT effects on R.O. and $v_{W(F)}$ will not propagate to worsen $v_{W(O)}$ and $v_{W(HR)}$, which ultimately determine the lowest v_S for successful wake up. Simulated $v_{W(O)}$ and $v_{W(HR)}$ varies across 173–274 mV and 232–336 mV across corners, respectively.

In static mode, PVT variation mostly affects R_{MG}. Since W_{MG} is wide and R_{MG}'s effect is negligible compared to R_L as Section II.H. indicates, so $v_{S(O)}$ varies less across corners.

IV. THE STATE-OF-THE-ART AND DISCUSSION

State-of-the-Art: Compact designs prefer a smaller number of off-chip components N_{OC}, and a smaller number of switches N_{SW}. This is because less N_{OC} & N_{SW} means smaller board and chip area. A tinier energy source often presents a higher R_S and avails less power. Because sources with higher R_S avail less power, a SL boost that has lower wake thresholds with low R_S may have higher wake thresholds with high R_S. Thus, R_S must be considered for a fair comparison. $v_{W(F)}$, $v_{W(O)}$, $v_{W(HR)}$, $v_{S(O)}$, and $v_{B(TAR)}$ are also crucial since they define charger performance. Since all wake and static thresholds refer to the open-circuit source voltage v_S in this paper, this section compares prior arts that report v_S. Technology nodes and special requirements are also compared. Table III summarizes this comparison.

TABLE III: COMPARISON WITH THE STATE-OF-THE-ART

		[17]	[5]	[6]	[7]	[18]	[19]	This Work
Wake Charger		SL	SL	SC	SC	–	–	SL
Static Charger		SL	SL	SL	SL	SL	SL	SL
Off-chip Components N_{OC}		2 L MEMS Sw.	1 L	1:60 X-former 1 Diode 1 C	4 L	1 L	1 L	1 L
Special Requirements		MEMS	Low-v_T NMOS	Native NMOS		–	–	–
Tech. [µm]		0.35	0.18	0.13	0.065	0.13	0.18	1.6
N_{SW}		4	2	3	26	2	2	2
R_S [Ω]		5	180	5	6.2	3.9	210	350
$v_{B(TAR)}$ [V]		1.8	0.9	1.2	1.2	1.0	1.9	1.8
v_S [mV]	$v_{W(F)}$	Require Motion	220	40	50	–	–	49
	$v_{W(O)}$		*350	40	50	–	–	225
	$v_{W(HR)}$		350	40	50	–	–	285
	$v_{S(O)}$	25	**70	40	50	**40	**30	40

* Projected based on reported time-domain waveform.
** Article only reports $v_{IN(MIN)}$, projected assuming MPP operation: $v_{S(O)} = 2 \times v_{IN(MIN)}$.

Designs in [5] and [17] use only SL chargers. However, [17] uses a MEMS switch in wake mode. Therefore, it not only requires motion to wake the SL charger system, but also demands special MEMS devices and occupies larger system volume. [5] uses single off-chip inductor and no mechanical switches in wake mode and targets higher R_S. Design in [5] is very compact, but $v_{W(O)}$ and $v_{W(HR)}$ are 350 mV, which is higher than the lowest-possible for SL chargers. With the proposed design theory, this proposed single-inductor SL charger reduces $v_{W(O)}$ and $v_{W(HR)}$ to the lowest-possible for SL converters, which are 225–285 mV, even with a higher R_S.

Designs in [6]–[7] uses SCs in wake mode. [6] uses a 1:60 off-chip transformer in wake mode to amplify the ac oscillation generated from v_{IN} and uses a SC charge pump to rectify amplified oscillation. However, the 1:60 transformer is off-chip, bulky, and occupies excessive volume.

To eliminate the bulky transformer, design in [7] uses a 13-stage SC in wake mode, and $v_{W(F)}$, $v_{W(O)}$, and $v_{W(HR)}$ are as low as 50 mV. The fundamental reason why SLs have to wake with higher v_S than SCs is: in wake mode, power switches lack gate-drive voltages and operate in sub-threshold region. Thus, highly resistive switches limit i_L and v_S can hardly energize inductor L_X as Section II.C justifies. However, for SCs, v_S can approximately fully pre-charge flying capacitors despite switches are resistive, provided that switching period is long enough and the SC operates in slow-switching region.

$v_{S(O)}$ is 30–40 mV in [18]–[19]. Although the design in [19] achieves lower $v_{S(O)}$, they are not wake-capable and thus designers do not have to select the highest inductance regardless of its ESR. Thus, designs in [18]–[19] use low ESR inductors at the cost of losing self-waking capability.

Despite [7] shows that SCs can wake with lower v_S, theorizing and experimentally validating the lowest-possible v_S for a SL boost proves the fundamental limits of SL converters in wake mode: sub-threshold resistive switches limits inductor current and prevents L_X from getting energized. Moreover, since this paper also experimentally validates that the lowest-possible v_S for SL to operate in static mode (about 40 mV) is lower than that of SC's, therefore, this paper also proves that the best system is a SC-SL hybrid that uses SC in wake mode and uses SL in static mode with experimental validations.

Comparator Offset Voltages: Comparators in this system (CP_{MPP} & CP_{ZCD} in Fig. 5) are only active during static mode, they can be completely shut off in wake mode by power-gating and only the cut-off currents of their MOSFETs load the system in wake mode [22]. Therefore, CP_{MPP} & CP_{ZCD}'s inaccuracies only affect $v_{S(O)}$, and only their cut-off currents (could be in nano-Amperes [22–23]) affect wake mode $v_{W(O)}$. When the system is in wake mode, since the total loss is in µW-level as Table I shows, CP_{MPP} & CP_{ZCD}'s leakage power is negligibly small compared to the total loss and thus has little impact on $v_{W(O)}$.

For an ideal CP_{ZCD}, its output trips when zero-volt crosses CP_{ZCD}'s input differential pair. For a practical design, CP_{ZCD}'s offset $v_{OS(ZCD)}$ and propagation delay $t_{P(ZCD)}$ affects the accuracy of Zero-Current Detection and consequently adds loss. For analog comparators like CP_{ZCD}, $v_{OS(ZCD)}$ incorporates both random and systemic components [25]. Random offsets usually stem from mismatch imperfections of MOSFETs in

the comparator, especially the input differential pair. Systemic offsets usually stem from drain-source voltage v_{DS} mismatches and channel-length modulation error [25–26]. $t_{P(ZCD)}$ usually stems from parasitic capacitances that delays signal.

However, for CP_{ZCD} in Fig. 5, intentionally adding a negative offset $v_{OS(INT)}$ to the v_{SW} terminal is preferable. This is usually done by sizing the input stage MOSFET on the v_{SW} side slightly smaller than the MOSFET on the other side as [10] proves. This intentional negative offset is to aid CP_{ZCD} such that it trips exactly when M_B's voltage $v_{MB} = v_{SW} - v_B$ crosses zero. Without this intentional offset, CP_{ZCD} can only trip and turn off M_B after sufficient differential overdrive voltage occurs at its input, which means v_{SW} needs to drop sufficiently lower than v_B. This causes inductor current i_L to flow in the reverse direction, and thus creates loss. With the intentional negative offset to assist the v_{SW} terminal, CP_{ZCD} would not require v_{SW} to drop below v_B to switch state due to the presence and help of the negative offset, and thus can turn off M_B exactly when v_{MB} crosses zero.

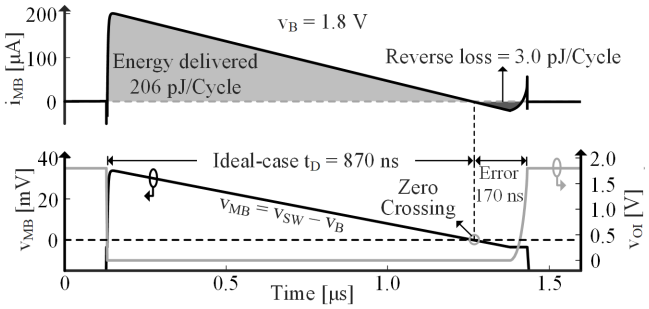

Fig. 24. Simulated transient waveforms related to zero-current detection.

This is why analog ZCD comparators are still widely used for low-voltage low-power energy harvesting applications as [5, 10, 15, 27] show. With such intentional offset, CP_{ZCD} can trip with 2 mV overdrive voltage (when v_{SW} is 2 mV less than v_B) and 30 ns $t_{P(ZCD)}$ as [10] shows. Fig. 24 shows the simulated M_B current i_{MB}, M_B's gate control v_{OI} (labelled in Fig. 5), and the voltage across M_B (labelled as v_{MB}) during a ZCD event. With $v_S = v_{S(O)} = 40$ mV, the ideal-case t_D is about 870 ns as Fig. 24 shows. CP_{ZCD}'s inaccuracies, which manifest themselves as a 170-ns error in t_D, adds a 19.5% error to the ideal-case t_D. As Fig. 24 shows, the simulated 3.0-pJ reverse-current loss caused by this 19.5% error is only 1.46% of the 206-pJ delivered energy. With this 19.5% error in t_D, the simulated $v_{S(O)}$ is 37.1 mV, which is only 0.8 mV or 2.2% higher than without this error (which is 36.3 mV).

CP_{MPP}'s offset $v_{OS(MPP)}$ makes v_{IN} deviate from v_{MPP}. Fortunately, input power P_{IN} (from the TEG to the SL boost) is less sensitive to v_{IN} near the MPP (for example, 10% error in v_{IN} causes 1% reduction in P_{IN}) [5]. Therefore, there is enough margin for error. CP_{MPP} designed and fabricated in [10] carries 3-mV $v_{OS(MPP)}$. With $v_S = v_{S(O)} = 40$ mV, v_{MPP} is 20 mV and the 3-mV $v_{OS(MPP)}$ only reduces P_{IN} from the ideal P_{MPP} by 2.3 %. With both CP_{MPP} & CP_{ZCD}'s errors altogether, the simulated $v_{S(O)}$ is 38.4 mV, which is only 2.1 mV or 5.8% higher than without both CP_{MPP} & CP_{ZCD}'s errors (which is 36.3 mV).

Controller Power Consumption: LD_{HR}, CP_{MPP}, and CP_{ZCD} account for the major power consumption P_{CNTR} of the control block shown in Fig. 5. CP_{MPP} & CP_{ZCD} are active only during static mode. During wake mode, they will be cut-off by power-gating techniques [23]. Therefore, CP_{MPP} & CP_{ZCD} consumes active power during static mode, and affects $v_{S(O)}$. LD_{HR} however, monitors v_B all the time and determines whether the system operates in wake or static mode. Thus, it is an always-on block and affects both $v_{W(O)}$ and $v_{S(O)}$.

LD_{HR}, CP_{MPP}, and CP_{ZCD} can all be designed in similar fashion as [5] & [10] show. When active in static mode, CP_{MPP} and CP_{ZCD} can consume 8.3 pJ & 8.4 pJ per switching cycle, respectively (according to [10]). When $v_S = v_{S(O)} = 40$ mV, the optimal switching frequency f_{SW}' is about 1.3 kHz as Fig. 23 shows. Thus, CP_{MPP} & CP_{ZCD} can consume 10.8 nW & 10.9 nW in static mode, respectively. The always-on level detector LD_{HR} can consume 110 nW as in [5, 28]. Therefore, the total power consumed by the controller can be 132 nW. Table IV details the power consumption P_{CNTR} of each block in the state-of-the-art.

TABLE IV: POWER CONSUMPTION OF STATE-OF-THE-ART CONTROL BLOCKS

Block	Power	Mode	Ref.
CP_{MPP}	10.8 nW	Static mode only	[10]
CP_{ZCD}	10.9 nW	Static mode only	[10]
LD_{HR}	110 nW	Wake & static mode	[5, 28]

In static mode, with 350-Ω R_S and $v_S = v_{S(O)} = 40$ mV, the maximum available power P_{MPP} from TEG is 1.14 μW, which is 8.7× higher than the controller power consumption. Because P_{MPP} is much larger than controller power consumption, this P_{MPP} provides good margin to support the controller. With all LD_{HR}, CP_{MPP}, & CP_{ZCD}'s power consumption altogether loading the system in simulation, the simulated $v_{S(O)}$ is 41.2 mV, which is only 4.9 mV or 13% higher than the ideal-case simulation (which is 36.3 mV).

In wake mode, only LD_{HR} consumes 110 nW [5], so this is less than 1.1% of the total wake mode power loss, which could be on the level of 10–20 μW as Table I shows. With this additional 110-nW LD_{HR} power consumption loading the system in simulation, the simulated $v_{W(O)}$ is 205 mV, which is only 2 mV or 1% higher than the ideal-case simulation (which is 203 mV). The simulated $v_{W(HR)}$ is 274 mV, which is only 4 mV or 1.5% higher than the ideal-case simulation (which is 270 mV). In sum, controller power consumption affects wake mode & static mode performance by 1.5% & 13%, respectively. Table V compares simulated performance with and without controller power consumption P_{CNTR}.

TABLE V: SIMULATED PERFORMANCE DEGRADATION

Metric	w/o P_{CNTR}	w/ P_{CNTR}	Absolute / Percentage Degradation
$v_{W(O)}$	203 mV	205 mV	2 mV / 1%
$v_{W(HR)}$	270 mV	274 mV	4 mV / 1.5%
$v_{S(O)}$	36.3 mV	41.2 mV	4.9 mV / 13%

Advanced Process Technologies: The 1.6-μm prototype shown in this paper is for testing purposes only. For more advanced processes (i.e, 350-nm and 180-nm processes), the losses involved are still channel ohmic loss P_{MR}, gate charge loss P_{MC} and leakage loss P_{LK}. For advanced process technologies and possible short-channel effects (i.e, threshold

voltage roll-off, velocity saturation, & drain-induced barrier lowering [23, 33]), what they affect are process parameters such as threshold voltage, mobility, channel resistivity, etc. However, P_{MR}, P_{MC}, & P_{LK}, they all change in the same fashion across design variables, especially transistor widths (i.e., P_{MR} reduces with increasing channel width, while P_{MC} & P_{LK} increases with increasing channel width). Thus, the fundamental trade-offs of these losses against all design variables do not change. This means despite the final numerical result may change across process technologies, the proposed fundamental design concept, which is the focus of this paper, does not change across process technologies.

V. Conclusions

This paper theorizes and experimentally validates the lowest v_S possible for a single-inductor switched-inductor (SL) boost charger, both in wake and static mode. This paper derives closed-form design expressions for the inductor, low-voltage ring oscillator, power switches, and peak inductor current, so a single-inductor SL charger can operate with the lowest v_S possible. This paper validates the design theory with a 1.6-µm CMOS prototype. When source resistance is 350 Ω, this prototype validates that the lowest-possible v_S for SLs in wake mode is 225–285 mV. In static mode, the lowest-possible v_S for SLs is 40 mV. Practical design issues such as comparator offset voltage, controller power consumption, and impacts of more advanced process technologies are also discussed in detail. Despite recent literature shows that switched-capacitors (SCs) can wake with lower v_S, theorizing and experimentally validating the lowest v_S possible for SL boost chargers can prove the fundamental limits of SL converters in wake mode. Moreover, since this paper also validates that SL operates with lower v_S than SC in static mode, therefore, SC-SL hybrids are the best system.

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