Energy-Harvesting Piezoelectric-Powered CMOS Series Switched-Inductor Bridge

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***Abstract*— Tiny piezoelectric transducers transform a very small fraction of ambient energy into electrical power. Power losses and breakdown voltages unfortunately limit how much of this power reaches the microsystem. The piezoelectric harvester presented here operates at the maximum power point (MPP) without the separate MPP stage that typical piezoelectric harvesters need. As a result, the system loses less power and occupies less space. Plus, with only four transistors, the charger increases the voltage with which the piezoelectric current generates power. This way, the harvester draws more power from vibrations. By pre-charging the transducer between half cycles, the 0.81–1.2-µm CMOS system outputs 0.7–49 µW of the 1.2–55 µW that a vibrating 16.8-nF transducer avails at 120 Hz. This is up to 6.8× more power than a lossless diode bridge can harness and as much as the best recycling bridge can output, but with four fewer power switches and without a separate maximum power-point stage.**

***Index Terms*— Energy harvester, piezoelectric charger, switched-inductor bridge, maximum power point (MPP), damping force, synchronized discharges, power index, synchronized switch damping/harvesting on inductor (SSDI and SSHI).**

Nomenclature

i_{PZ}	Piezoelectric current [A]
$i_{PZ(PK)}$	Peak piezoelectric current [A]
C_{PZ}	Piezoelectric capacitance [F]
$C_{PZ(XFR)}$	Piezoelectric capacitance during energy transfers between half cycles [F]
E_{PC}	C_{PZ}'s energy at v_{PC} [J]
E_{PK}	C_{PZ}'s energy at $v_{PZ(PK)}$ [J]
E_{XFR}	Energy C_{PZ} transfers between half cycles [J]
i_L	Inductor current [A]
P_{LOSS}	Power losses [W]
P_O	Output power [W]
P_{PZ}	Drawn piezoelectric power from transducer [W]
$P_{PZ(BRDG)}'$	Power generated by a lossless diode bridge [W]
$P_{PZ(MAX)}$	The maximum power that i_{PZ} can supply [W]
V_{BD}	CMOS breakdown voltage [V]
v_{PC}	Pre-charge voltage [V]
v_{PZ}	Piezoelectric voltage [V]
$v_{PZ(PK)}$	Peak piezoelectric voltage [V]
$\Delta v_{PZ(OC)}$	Transducer's open-circuit voltage [V]
$\eta_{I(PZ)}$	Drawn power index [W/W]
$\eta_{I(O)}$	Output power index [W/W]

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I. Piezoelectric Energy-Harvesting Microsystems

Sensors can monitor, process, store, and communicate data about their surrounding environment that save money, energy, and lives. In practice, many existing and emerging applications that can benefit from this technology cannot fit connectors or ports. Sensors should therefore be small and self-sustaining [1]–[2]. With so much functionality, however, tiny onboard batteries can drain quickly [3]. Luckily, vibrations are often available and abundant [4]–[5], so ambient energy in motion can replenish the energy that these small batteries supply.

Small transducers only draw 1% to 5% of the energy available in motion [6]. Piezoelectric generators are more popular than electromagnetic and electrostatic transducers are because they output 1.3× to 3× more power under similar constraints and conditions [7]. But since power-supply circuits burn power, the system receives less power than this [8]. In some cases, still less power is available because transistor breakdown voltages limit the voltage with which harvesters can draw power [9]. This is why energy harvesters should operate at their maximum power point (MPP) [10].

Energy-harvesting systems powered with piezoelectric transducers normally include MPP features for this purpose. In Fig. 1, for example, the charger draws power from a tiny piezoelectric generator. Since small transducers output little power, a battery vB is used to cache power. When vB holds enough energy, a power supply draws power from vB to feed the sensors, interface amplifiers (A_V), analog–digital converters (ADC), digital-signal processors (DSP), memory, and power amplifiers (PA) in the system. The purpose of the maximum power-point tracker (MPPT) is to adjust the charger so it outputs the highest power possible.

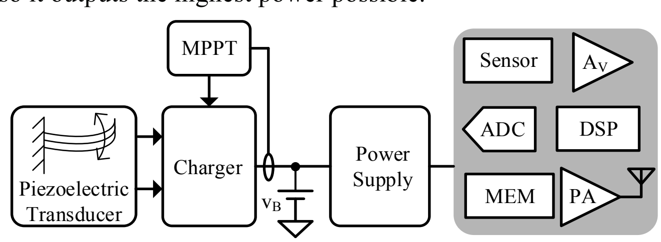

Fig. 1. Piezoelectric-powered energy-harvesting microsystem.

The principal aim of the charger is to draw the highest power possible with the least losses and under the least constraints. The four-transistor series switched-inductor bridge presented here does this by pre-charging the piezoelectric transducer to a level that is adjustable. This way, without another power stage, the charger can operate at the MPP with few power-consuming transistors switching across a vibration cycle. To understand the details and benefits of this bridge, Sections II–V describe operation, discuss output power, and assess and compare performance with the state of the art.

II. Proposed Series Switched-Inductor Bridge

A. Piezoelectric Transducer

Charge centers in a piezoelectric cantilever misalign when deformed [11]. The voltage potential that this establishes across the capacitance C_{PZ} of the transducer induces charge flow. So when a transducer vibrates without an electronic load, the resulting current i_{PZ} charges and discharges C_{PZ} across $\Delta v_{PZ(OC)}$. The transducer therefore delivers and recovers the energy that C_{PZ} receives.

But when a harvester extracts the energy that C_{PZ} receives, less energy is available to push the piezoelectric cantilever. As a result, displacement distance decreases, and in consequence, so does i_{PZ}. Electrical energy in C_{PZ} is so low with respect to mechanical energy in the system, however, that draining C_{PZ}'s energy has nearly no effect on the moving cantilever or the charge that i_{PZ} supplies [6], [12]–[21]. In other words, i_{PZ} is nearly independent of the damping force with which the harvester draws power. This means that drawing more power from the transducer has little effect on i_{PZ}.

B. Operation

The first basic objective of the charger proposed is to draw the power that C_{PZ} collects across each half cycle. For this, the switched-inductor bridge in Fig. 2 drains C_{PZ} between half cycles. This is why C_{PZ}'s voltage v_{PZ} in Fig. 3 falls to zero at 4.2, 8.4, and 13 ms. The second aim of the charger proposed is to raise the voltage v_{PZ} with which C_{PZ} collects charge. This way, with higher v_{PZ}, i_{PZ} generates more power P_{PZ} or $i_{PZ}v_{PZ}$. The bridge does this by recycling some of the energy drawn to pre-charge C_{PZ} to v_{PC} before every half cycle begins (at 4.2, 8.4, and 13 ms). Therefore, v_{PZ} starts at v_{PC} and rises to v_{PC} + $\Delta v_{PZ(OC)}$ across each half cycle. With a higher v_{PZ} (that is always greater than v_{PC}), the system draws more power from motion than without v_{PC}, which means the damping force against vibrations is greater.

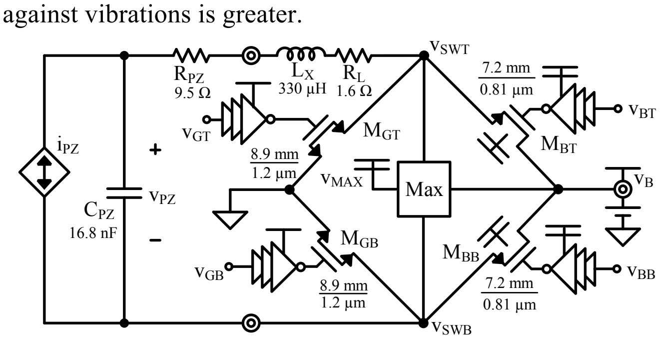

Fig. 2. Proposed piezoelectric-powered series switched-inductor bridge.

To start this, all but the bottom ground switch M_{GB} open across i_{PZ}'s positive half cycle, so the bridge open-circuits and i_{PZ} charges C_{PZ} to $v_{PZ(PK)}$ across 0.1–4.2 ms in Fig. 3. The top ground switch M_{GT} then closes to drain C_{PZ} into the transfer inductor L_X. As L_X energizes, v_{PZ} falls to zero and L_X's current i_L in Fig. 4 increases (across t_E at 4.167–4.170 ms). M_{GB} and M_{GT} remain closed for another short interval t_{D1} to partially drain L_X into C_{PZ}, and that way, pre-charge C_{PZ} in the negative direction. After that, M_{GT} opens and the top battery switch M_{BT} closes across t_{D2} to deplete L_X into the battery v_B and C_{PZ}. So v_B charges after the positive half cycle, like Fig. 3 shows, and C_{PZ} charges to $-v_{PC}$ before the negative half cycle.

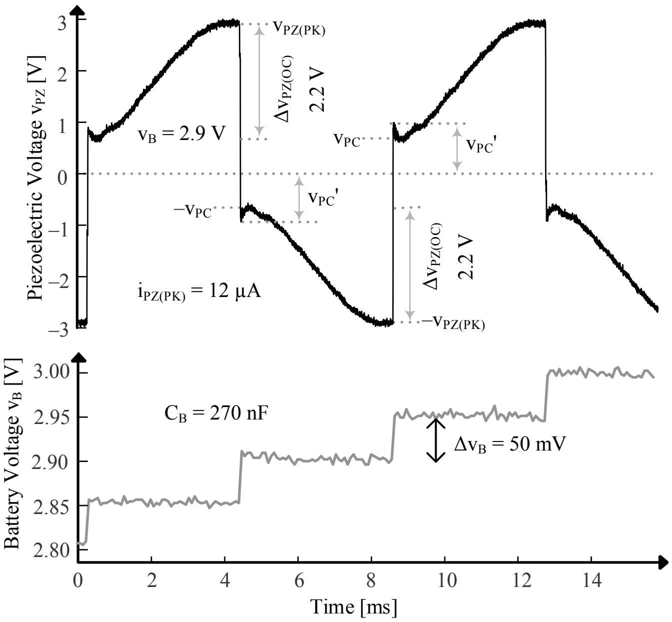

Fig. 3. Measured piezoelectric and battery voltages across cycles.

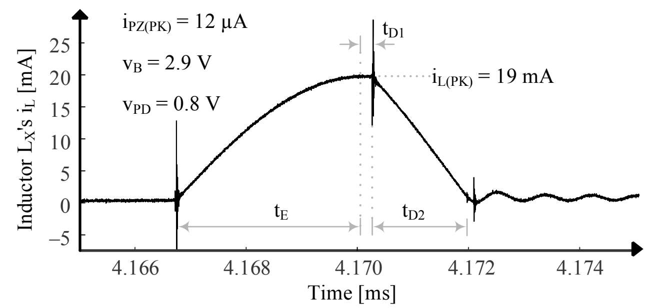

Fig. 4. Measured inductor current at the end of a positive half cycle.

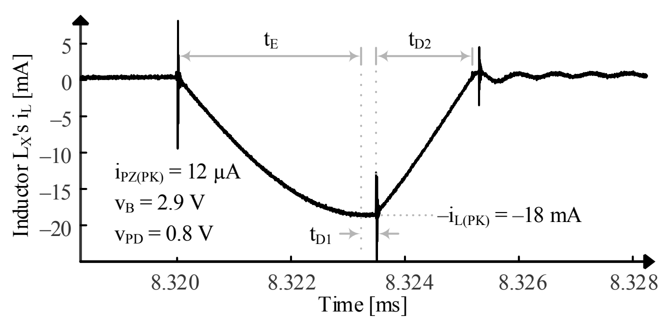

Fig. 5. Measured inductor current at the end of a negative half cycle.

The process repeats across negative half cycles. In this case, all but M_{GT} open across 4.2–8.4 ms in Fig. 3, so i_{PZ} charges C_{PZ} from $-v_{PC}$ to $-v_{PZ(PK)}$. M_{GB} then closes at 8.320 ms in Fig. 5 to drain C_{PZ} into L_X (across t_E) and a little longer (across t_{D1}) to partially drain L_X into C_{PZ}. After that, M_{GB} opens and M_{BB} closes (across t_{D2}) to deplete L_X into v_B and C_{PZ}. This way, v_B

receives charge and C_{PZ} pre-charges to v_{PC} in Fig. 3.

The entire sequence, which Table I summarizes, repeats every cycle to exhibit the steady-state behavior shown in Fig. 3. Figure 6, for example, shows how the system charges 270 nF across 2.7–4.2 V across 40 ms in approximately 50-mV increments. This voltage range corresponds to that of thin-film Li Ion batteries [22]. Total charge time ultimately depends on the capacity of the battery and vibration strength.

TABLE I: SWITCHING SEQUENCE

i_{PZ}'s State*	M_{GT}	M_{GB}	M_{BT}	M_{BB}
Across + ½ Cycle	Open	Closed	Open	Open
+/– Transition t_E	Closed	Closed	Open	Open
+/– Transition t_{D1}	Closed	Closed	Open	Open
+/– Transition t_{D2}	Open	Closed	Closed	Open
Across – ½ Cycle	Open	Open	Open	Closed
–/+ Transition t_E	Open	Open	Closed	Closed
–/+ Transition t_{D1}	Open	Open	Closed	Closed
–/+ Transition t_{D2}	Closed	Open	Open	Closed

*"+" and "–" refer to i_{PZ}'s polarity.

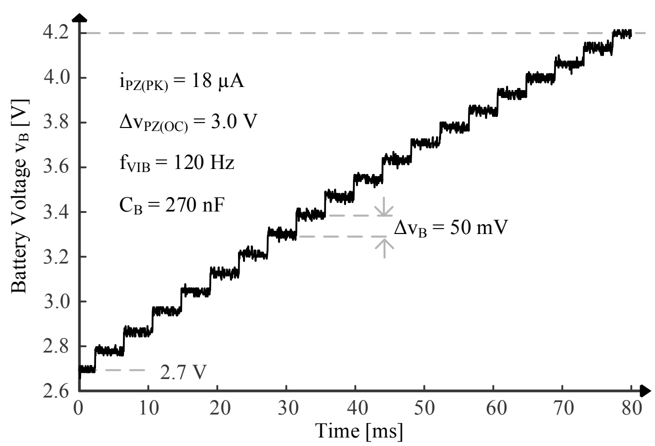

Fig. 6. Measured charging profile.

C. Power Transistors

The switches require gate-drive power P_G to switch and ohmic power P_R to conduct. Since gate capacitance C_G and channel resistance R_{CH} increase with channel length L_{CH}, L_{CH} should be minimum length L_{MIN}. In this case, the L_{MIN} that can withstand 5.5 V is 1.2 μm for NFETs and 0.81 μm for PFETs. But since C_G increases and R_{CH} decreases with wider channels, channel widths W_{CH} in Fig. 3 balance P_G and P_R [23] when the system draws 30 μW from the transducer, which here corresponds to the most probable vibration strength. Optimizing W_{CH} for the most likely condition saves energy, and in consequence, outputs the most power.

D. Drivers

Three inverters with transistors of increasing dimensions drive each switch. The first inverter in the driver is minimum size, the second is 5× larger than the first, and the third is 5× larger than the second. Although 2.67× is optimal for shortest propagation delay [24], a higher gain reduces the number of inverter stages, and as a result, the shoot-through power that they consume [25].

Since NFETs connect to ground and ground is the lowest potential in the circuit, NFETs can open and close with the voltage that a lithium-ion battery can supply: 2.7–4.2 V [22]. This is why the supplies for NFET drivers are v_B and ground. For PFETs to open, their gates must charge to the highest terminal voltage. PFETs here connect to v_B and switching nodes v_{SWT} and v_{SWB}, which rise to a level $v_{PZ(PK)}$ (in Fig. 3) that depends on pre-charge voltage v_{PC} and vibration strength $\Delta v_{PZ(OC)}$. This means, v_{SWT} and v_{SWB} may or may not surpass v_B, so v_B is not a good supply for PFET drivers.

E. Maximum-Supply Selector

The purpose of the maximum-supply selector block Max in Fig. 2 is to establish the highest supply v_{MAX} with which PFET drivers can open P-type switches. For this, cross-coupled PFET pair M_{1A}–M_{1B} in Fig. 7 selects and connects the higher of v_{SWT} and v_{SWB} to v_{O1}: M_{1A} connects v_{SWT} to v_{O1} when v_{SWB} is below v_{SWT} by more than a PFET threshold voltage $|v_{TP}|$ and M_{1B} connects v_{SWB} to v_{O1} when the opposite is true. M_{2A}–M_{2B} similarly selects and connects the higher of the resulting v_{O1} and v_B to v_{MAX}. So together, v_{MAX} is the highest of the three voltages:

$$v_{MAX} = \mathrm{Max}\left\{v_{O1}, v_B\right\} = \mathrm{Max}\left\{v_{SWT}, v_{SWB}, v_B\right\}. \qquad (1)$$

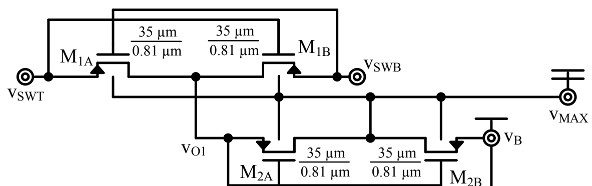

Fig. 7. Prototyped maximum-supply selector.

v_{MAX} in Fig. 8, for example, connects to v_B at 1.8–3.4 ms because v_B's 2.9 V exceeds v_{SWT}'s 0–2.9 V and v_{SWB}'s 0 V. v_{MAX} connects to v_{SWT} at 3.4–5.8 ms because v_{SWT}'s 2.9–4.5 V similarly surpasses v_B's 2.9 V and v_{SWB}'s 0 V. v_{MAX} then connects to v_{SWB} at 7.4–10 ms because v_{SWB}'s 2.9–4.5 V is greater than v_B's 2.9 V and v_{SWT}'s 0 V.

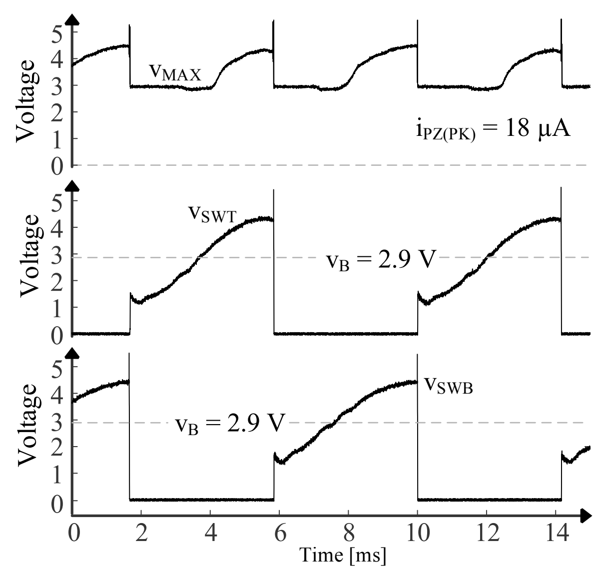

Fig. 8. Measured maximum-supply selector waveforms in steady state.

Although M_{1A}, M_{1B}, M_{2A}, and M_{2B} do not conduct as much current as power NFETs and PFETs in Fig. 2, they still supply the charge that PFET gates in Fig. 2 need to switch between states. This is why their channel lengths (in Fig. 7) are the shortest possible that can withstand 5.5 V. Their channel widths ensure M_{1A}, M_{1B}, M_{2A}, and M_{2B} drop less than 100 mV when charging PFET gates in Fig. 2.

Cross-coupled PFETs do not close when their terminal (gate) voltages are within a threshold $|v_{TP}|$ of one another. Here, however, M_{1A}–M_{1B}'s v_{SWT} and v_{SWB} are within a $|v_{TP}|$ only between half cycles across 2–4-μs transitions, when M_{GT} and M_{GB} connect v_{SWT} and v_{SWB} to ground. This is not a problem because v_B is much greater than v_{SWT} and v_{SWB} during this time, so M_{2B} connects v_B to v_{MAX}.

M_{2A}–M_{2B}'s v_{O1} and v_B are within a $|v_{TP}|$ only when C_{PZ} charges high enough to be within a $|v_{TP}|$ of v_B, which does not always happen. If $v_{PZ(PK)}$ is well above v_B, for example, v_{SWT} and v_{SWB} are within a $|v_{TP}|$ of v_B only when v_{SWT} and v_{SWB} cross v_B. This is not a problem because transitions are short and PFET gates do not need charge halfway across transitions. But even if v_{PZ} peaks within a $|v_{TP}|$ of v_B, M_{1A}–M_{1B} and M_{2A}–M_{2B}'s combined bulk-to-substrate capacitance C_{BULK} is large enough to hold and supply the charge that PFET gates in Fig. 2 need across this short interval. Although adding capacitance helps, C_{BULK} adds to C_{PZ} when v_{SWT} or v_{SWB} is higher than v_B, so C_{BULK} steers i_{PZ} away from C_{PZ}. In other words, adding capacitance sacrifices energy that would otherwise reach C_{PZ}.

The worst-case condition occurs when v_{SWT} and v_{SWB} cross v_B within half cycles (at, for example, 3.4, 7.4, and 11.4 ms in Fig. 8). Across these millisecond crossings, v_{MAX} is a $|v_{TP}|$ below v_{SWT} and v_{SWB}. With $|v_{TP}|$ of gate drive, however, battery PFETs M_{BT} and M_{BB} in Fig. 2 operate in weak inversion. So although their effect is to leak v_B to ground and to leak C_{PZ} to v_B, leakage is low because these PFETs are very resistive in weak inversion.

III. Output Power

A. Drawn Piezoelectric Power

The system draws between half cycles the energy that C_{PZ} collects across half cycles. The energy that C_{PZ} needs (E_{PC}) to pre-charge to v_{PC} essentially cycles between C_{PZ} and L_X. So of the energy drawn when v_{PZ} peaks (E_{PK}), the transducer supplies the difference $E_{PK} - E_{PC}$ every half cycle and twice that difference $2(E_{PK} - E_{PC})$ every full cycle t_{VIB}.

Since i_{PZ} charges C_{PZ} across $\Delta v_{PZ(OC)}$ every half cycle, v_{PZ} increases from v_{PC} (at 4.2, 8.4, and 13 ms in Fig. 3) to $v_{PC} + \Delta v_{PZ(OC)}$, C_{PZ}'s peak voltage $v_{PZ(PK)}$. C_{PZ}'s peak energy E_{PK} or $0.5C_{PZ}v_{PZ(PK)}^2$ is therefore $0.5C_{PZ}(v_{PC} + \Delta v_{PZ(OC)})^2$. But after subtracting E_{PC}'s $0.5C_{PZ}v_{PC}^2$, drawn piezoelectric power P_{PZ} reduces to

$$
\begin{aligned}
P_{PZ} &= 2\left(\frac{E_{PK} - E_{PC}}{t_{VIB}}\right) \\
&= 2\left(0.5C_{PZ}v_{PZ(PK)}^{\ 2} - 0.5C_{PZ}v_{PC}^{\ 2}\right)f_{VIB} \\
&= 2\left\{0.5C_{PZ}\left[\left(v_{PC} + \Delta v_{PZ(OC)}\right)^2 - v_{PC}^{\ 2}\right]\right\}f_{VIB} \\
&= C_{PZ}\left(\Delta v_{PZ(OC)}^{\ 2} + 2v_{PC}\Delta v_{PZ(OC)}\right)f_{VIB}
\end{aligned}
\quad , \qquad (2)
$$

where f_{VIB} is the frequency of vibrations.

The underlying assumption here is that P_{PZ}'s damping (loading) effect on motion is negligible, which is the case for small piezoelectric devices [6], [12]–[21]. As a result, i_{PZ} is nearly unaffected by how much power the harvester draws with P_{PZ}, which is another way of saying the transducer can source more power than it actually supplies. This is why pre-charging C_{PZ} is so important, because v_{PC} raises the voltage v_{PZ} with which i_{PZ} generates P_{PZ}. And with a higher v_{PZ}, the transducer sources more power.

B. Transducer Losses

The mechanical properties of the transducer dictate how much piezoelectric capacitance C_{PZ} appears across its terminals [26]. In the case of the unit tested, C_{PZ} in Fig. 9 is 16.8 nF at the vibration frequency f_{VIB}, which here is 120 Hz. This is the capacitance that collects piezoelectric charge across half cycles.

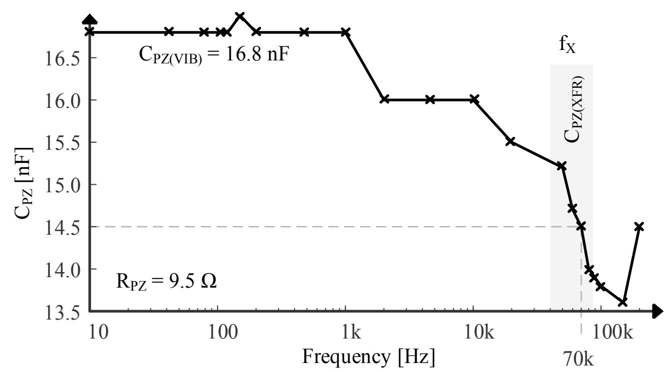

Fig. 9. Measured piezoelectric capacitance across frequency.

Interestingly, the effective capacitance falls as frequency climbs. This is not unreasonable because uneven distribution of so much series resistance R_{PZ} steers more current into capacitive components with lower resistance. This is why 14.5 nF of the 16.8 nF available activate when transferring energy at 70 kHz.

Here, 40–80 kHz corresponds to the 2–4 μs that L_X needs to transfer C_{PZ}'s energy between half cycles. In other words, a lower average capacitance $C_{PZ(XFR)}$ of 14.5 nF transfers between half cycles the energy that the higher counterpart C_{PZ} collects across half cycles. $C_{PZ(XFR)}$ therefore transfers the pre-charging charge q_{PC} required to pre-charge C_{PZ} to v_{PC}:

$$q_{PC} = C_{PZ}v_{PC} = C_{PZ(XFR)}v_{PC}' . \qquad (3)$$

Except, this same q_{PC} establishes a higher voltage v_{PC}' across $C_{PZ(XFR)}$'s lower capacitance. This is why C_{PZ}'s pre-charging level in Fig. 3 falls slightly at the beginning of every half cycle, because $C_{PZ(XFR)}$'s v_{PC}' drops to C_{PZ}'s v_{PC}.

This is unfortunate because a linear rise in voltage produces a quadratic rise in energy that outpaces a linear fall in capacitance. In other words, $C_{PZ(XFR)}$ needs more energy (E_{XFR}) than C_{PZ} requires (E_{PC}) to charge C_{PZ} to v_{PC}. Series resistances in C_{PZ} burn this difference $E_{XFR} - E_{PC}$ every half cycle and twice every full cycle t_{VIB}, so this loss P_{CPZ} is

$$\begin{aligned} P_{CPZ} &= 2\left(\frac{E_{XFR} - E_{PC}}{t_{VIB}}\right) \\ &= \left(C_{PZ(XFR)}\, v_{PC}'^2 - C_{PZ}\, v_{PC}^{\,2}\right) f_{VIB} \\ &= \left[C_{PZ(XFR)}\left(\frac{C_{PZ} v_{PC}}{C_{PZ(XFR)}}\right)^2 - C_{PZ}\, v_{PC}^{\,2}\right] f_{VIB} \\ &= C_{PZ}\, v_{PC}^{\,2}\left(\frac{C_{PZ}}{C_{PZ(XFR)}} - 1\right) f_{VIB} \end{aligned} \quad (4)$$

Note that P_{CPZ} vanishes when $C_{PZ(XFR)}$ and C_{PZ} match, when all capacitive components in the transducer transfer energy between half cycles. Also notice that P_{CPZ} scales with v_{PC}, so P_{CPZ} increases when v_{PC} rises. Plus, the series resistance R_{PZ} that conducts the power at 40–80 kHz burns ohmic losses P_{RPZ}. So imperfections in the transducer ultimately cost the system ohmic and dynamic losses P_{RPZ} and P_{CPZ}.

C. Maximum Output Power

Loss Limit: Power losses P_{LOSS} limit how much of the drawn piezoelectric power P_{PZ} the system can deliver. Unfortunately, all components lose power. The transducer loses ohmic power P_{RPZ} to R_{PZ} and dynamic power P_{CPZ} when pre-charging C_{PZ}. The inductor L_X's series resistance R_L also burns ohmic power P_{RL}. MOS transistors consume ohmic power P_{MR} to conduct and need gate-drive power P_{MG} to switch. Plus, drivers burn shoot-through power P_{ST} when they transition. And although not nearly as much, power PFETs leak piezoelectric and battery power P_{LK} when the switching nodes v_{SWT} and v_{SWB} cross v_B and C_{BULK} leaks piezoelectric power P_B away from C_{PZ} when v_{SWT} and v_{SWB} surpass v_B. So of P_{PZ}, the battery v_B receives $P_{PZ} - P_{LOSS}$, where P_{LOSS} is

$$P_{LOSS} = P_{RPZ} + P_{CPZ} + P_{RL} + P_{MR} + P_{MG} + P_{ST} + P_{LK} + P_B. \quad (5)$$

Power-conversion efficiency η_C is therefore the fraction of PPZ that all these losses P_{LOSS} in the system avail with output power P_O:

$$\eta_C = \frac{P_O}{P_{PZ}} = \frac{P_{PZ} - P_{LOSS}}{P_{PZ}} = 1 - \frac{P_{LOSS}}{P_{PZ}}. \quad (6)$$

Notice that fractional losses P_{LOSS}/P_{PZ} set this efficiency.

Since ohmic losses P_R climb with L_X's root–mean–squared conduction current $i_{L(RMS)}$ and $i_{L(RMS)}$ climbs with piezoelectric power P_{PZ}, losses P_{RPZ}, P_{RL}, and P_{MR} increase with P_{PZ}. But while P_{PZ} climbs linearly with $i_{L(RMS)}$, P_R grows quadratically (with $i_{L(RMS)}^{\,2}R_{EQ}$) for resonant transfers (t_E and t_{D1} in Fig. 4 and Fig. 5) and cubically (with $i_{L(RMS)}^{\,3}R_{EQ}$) for battery transfers (t_{D1} in Fig. 4 and Fig. 5) [20]. This means that, when vibration strength is low, an increase in P_{PZ} exceeds the rise in P_R to produce a net gain in P_O. Eventually, however, P_R's quadratic-to-cubic loss outpaces P_{PZ}'s linear gain to the extent that P_O falls. Plus, P_{CPZ} also increases quadratically with pre-charging voltage v_{PC}. So even though P_{PZ} rises monotonically across v_{PC}'s entire 0–4-V range in Fig. 10, P_O maxes at 12 µW when vibration strength peaks i_{PZ} to 12 µA and charges C_{PZ} across 2.0 V.

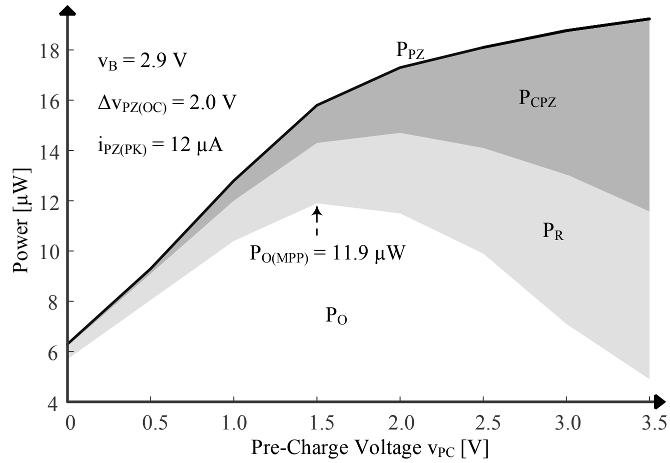

Fig. 10. Measured power across C_{PZ}'s pre-charge voltage.

As vibrations gain strength, P_R's rise cancels P_{PZ}'s gain at higher power levels. This is why the maximum power point $P_{O(MPP)}$ in Fig. 11 increases with $i_{PZ(PK)}$ up to 21 µA. As this happens, P_{RPZ}, P_{RL}, and P_{MR} rise. P_{MG} and P_{ST} do not increase with $i_{PZ(PK)}$ because gate-drive losses and shoot-through power do not scale with vibration strength. P_{RPZ} and P_{RL} dominate because R_{PZ} and R_L in small devices are much higher at 1–10 Ω [27]–[28] than MOS resistances, which engineers normally keep at milliohms [29]. In other words, scaling down the size of the transducer and the inductor produces the losses that dominate and limit P_O.

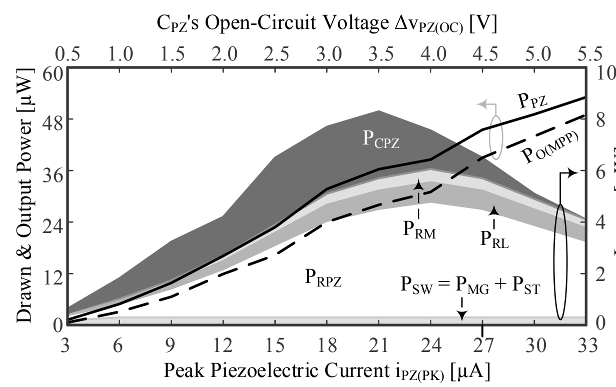

Fig. 11. Measured power and losses.

Since the power P_{CPZ} that C_{PZ} loses when pre-charging scales with v_{PC} and v_{PC} increases with vibration strength in this region, P_{CPZ} also increases with $\Delta v_{PZ(OC)}$ up to 3.5 V. In all, the system delivers 45%–91% of the 1.2–55 µW that the transducer supplies with i_{PZ} and v_{PZ} in P_{PZ}. Power-conversion efficiency η_C is lower when vibrations are weak because switching losses P_{MG} and P_{ST}, which do not scale with $\Delta v_{PZ(OC)}$, dominate when P_{PZ} is low.

Breakdown Limit: Recall that C_{PZ}'s voltage v_{PZ} is the voltage with which the piezoelectric current i_{PZ} supplies power P_{PZ}. So for the same i_{PZ}, the transducer outputs more power when v_{PZ}

is higher. The switched inductor here raises v_{PZ} by pre-charging C_{PZ} to v_{PC} before every half cycle begins. This way, i_{PZ} charges C_{PZ} to a higher peak $v_{PZ(PK)}$: to $v_{PC} + \Delta v_{PZ(OC)}$ (not just $\Delta v_{PZ(OC)}$). But since C_{PZ} exposes the switches in the bridge to this $v_{PZ(PK)}$, $v_{PZ(PK)}$ cannot exceed the transistors' breakdown level V_{BD}:

$$v_{PZ(PK)} = v_{PC} + \Delta v_{PZ(OC)} \le V_{BD} . \tag{7}$$

$v_{PZ(PK)}$ does not exceed V_{BD} when losses limit and set maximum output power $P_{O(MPP)}$, like in Figs. 10 and 11 when $i_{PZ(PK)}$ is below 21 μA. Above 21 μA, however, additional losses P_{LOSS} balance gains in piezoelectric power P_{PZ} at levels that require $v_{PZ(PK)}$ to surpass V_{BD}. V_{BD} limits $v_{PZ(PK)}$ under those conditions, which then limits and sets $P_{O(MPP)}$ before P_{LOSS} does. So as stronger vibrations raise Δv= above 3.5 V in Figs. 11 and 12, the system reduces C_{PZ}'s pre-charge level v_{PC} to keep $v_{PZ(PK)}$ from exceeding V_{BD}'s 5.5-V limit. This is why C_{PZ}'s loss P_{CPZ} falls in this region, because v_{PC} drops when $\Delta v_{PZ(OC)}$ surpasses 3.5 V (and P_{CPZ} scales with v_{PC}). Note that Fig. 12 shows v_{PZ} in steady state for several vibration strengths, for which peak currents $i_{PZ(PK)}$ range from 21 to 33 μA.

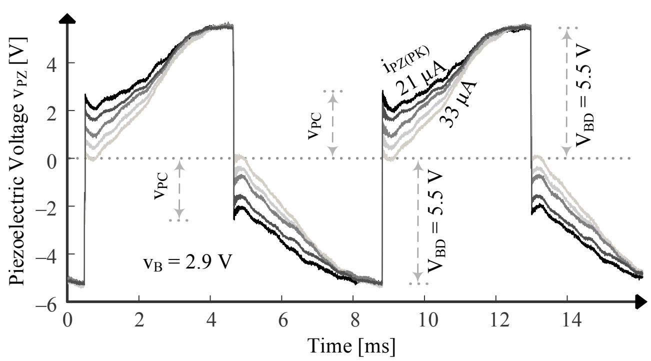

Fig. 12. Measured piezoelectric voltage when breakdown limits v_{PZ}.

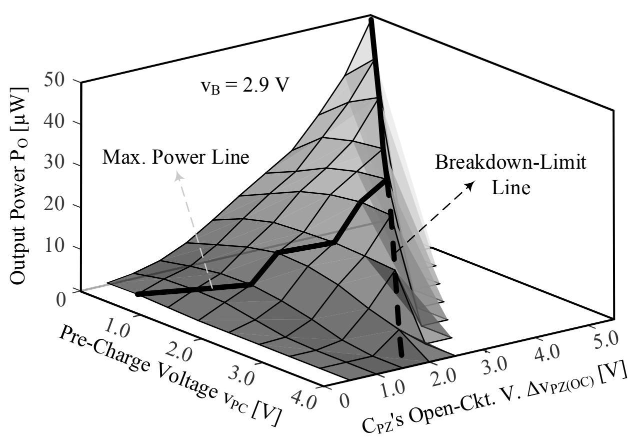

Fig. 13. Measured power across vibration strength and pre-charge voltage.

v_{PZ}'s breakdown boundary limits $v_{PC} + \Delta v_{PZ(OC)}$ to V_{BD}, which bounds the maximum power $P_{PZ(MAX)}$ that the transducer can supply to

$$\begin{aligned} P_{PZ(MAX)} &= P_{PZ}\big|_{v_{PC}+\Delta v_{PZ(OC)}=V_{BD}} \\ &= C_{PZ}\left(2V_{BD}\Delta v_{PZ(OC)} - \Delta v_{PZ(OC)}^{\;2}\right) f_{VIB} \end{aligned} . \tag{8}$$

But to be clear, $P_{PZ(MAX)}$ still under-damps the transducer to such a degree that the transducer can easily supply more power. The circuit, however, is the ultimate bottleneck that limits P_{PZ} to $P_{PZ(MAX)}$. This is why the trajectory of the maximum power point in Fig. 13 shifts when vibrations charge C_{PZ} across 3.5 V, because losses P_{LOSS} limit and set $P_{O(MPP)}$ below 3.5 V and breakdown voltage V_{BD} limits and sets $P_{O(MPP)}$ above 3.5 V.

Interestingly, ohmic losses P_R in Fig. 11 fall as stronger vibrations raise $\Delta v_{PZ(OC)}$ above 4.0 V. Before this happens, the switched inductor depletes C_{PZ} into L_X, so while L_X charges the battery v_B, L_X can also pre-charge C_{PZ} to v_{PC}. When $\Delta v_{PZ(OC)}$ surpasses 4.0 V, however, V_{BD} keeps v_{PC} so low that C_{PZ}'s energy E_{PK} is too much for L_X to pre-charge C_{PZ} to v_{PC}. So before C_{PZ} finishes draining into L_X, the system steers some of this energy E_{PK} to v_B. As a result, L_X receives and transfers less energy, and with less current to conduct, series resistances burn less ohmic power P_R. Since fractional losses P_{LOSS}/P_{PZ} are lower, power-conversion efficiency η_C increases in this region.

IV. Measured Prototype

The CMOS die in Fig. 14 integrates the power switches, the drivers, and the maximum-supply selector in Figs. 2 and 7. The board shown incorporates the packaged integrated circuit (IC) and the 330-μH, 1.6-Ω transfer inductor L_X used. The 16.8-nF, 9.5-Ω piezoelectric cantilever transducer attaches to the edge of the board. The die, transducer, and inductor occupy 0.7 × 0.7 mm2, 10 × 50 × 1 mm3, and 5 × 5 × 1 mm3, respectively. A field-programmable gate array (FPGA) generates the signals that switch the switched-inductor bridge and a shaker from Brüel & Kjær vibrates the cantilever so it generates 3–33 μA.

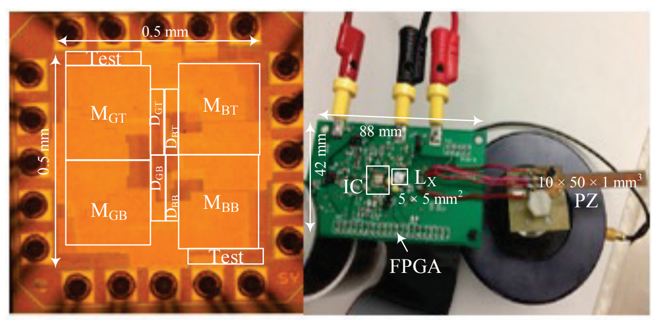

Fig. 14. CMOS die and board prototyped.

A. Power Indices

Maximum output power $P_{O(MPP)}$ hinges on vibration frequency and strength, the transducer, the voltage with which the transducer's current generates power, and losses. Of these, the only design-independent, application-specific factors are vibration frequency f_{VIB} and strength (in the form of acceleration in the mechanical domain and current i_{PZ} in the electrical domain). The transducer and the circuit that transfers power are typically the design variables that engineers control. Unfortunately, research splits along these lines, so advancements in circuits normally appear in the absence of advancements in transducers, and vice versa. As a result, literature rarely reports the best all-around solution.

The research focus here and in [13]–[19], [30]–[35] is on the circuit, not the transducer. So comparing performance without normalizing the effects of the transducers used seems unfair. The components in the transducer that in part determine $P_{O(MPP)}$ are capacitance C_{PZ}, resistance R_{PZ}, and dynamic capacitance $C_{PZ(XFR)}$. But since the diode bridges in [13]–[15], [19] draw power across half cycles (not between half cycles), the dynamic effects of $C_{PZ(XFR)}$ are absent. So including $C_{PZ(XFR)}$'s losses P_{CPZ} in the comparison seems fair. How R_{PZ} affects $P_{O(MPP)}$ also depends on the harvester, so although R_{PZ} is an imperfection in the transducer like $C_{PZ(XFR)}$, a fair evaluation should account for R_{PZ}'s loss P_{RPZ}.

The power $P_{PZ(BRDG)}'$ that a lossless diode bridge draws with i_{PZ} and C_{PZ} at f_{VIB} [36] includes all the independent components that research in circuits assumes (like i_{PZ}, C_{PZ}, and f_{VIB}) and excludes all the variables that circuit designers control and assign:

$$P_{PZ(BRDG)}' = 0.25 C_{PZ} \Delta v_{PZ(OC)}^{2} f_{VIB} . \tag{9}$$

Like before, $\Delta v_{PZ(OC)}$ is the voltage that i_{PZ} charges C_{PZ} across every half cycle. So comparing input and output power to this lossless case is a good way of assessing and normalizing circuit performance to the transducers used.

In this light, drawn power index $\eta_{I(PZ)}$ indicates how much additional power a harvester draws (with P_{PZ}) than a lossless diode bridge can harness from the same piezoelectric transducer:

$$\eta_{I(PZ)} = \frac{P_{PZ}}{P_{PZ(BRDG)}'} . \tag{10}$$

Losses P_{LOSS} limit how much of P_{PZ} the system ultimately delivers with $P_{O(MPP)}$. So with respect to the output, power-conversion efficiency η_C reduces $\eta_{I(PZ)}$ to yield output power index $\eta_{I(O)}$:

$$\eta_{I(O)} = \eta_{I(PZ)} \eta_C = \left(\frac{P_{PZ}}{P_{PZ(BRDG)}'}\right)\left(\frac{P_{O(MPP)}}{P_{PZ}}\right) = \frac{P_{O(MPP)}}{P_{PZ(BRDG)}'} , \tag{11}$$

which compares $P_{O(MPP)}$ with $P_{PZ(BRDG)}'$. But since gains in P_{PZ} can outpace P_{LOSS} and vice versa, $\eta_{I(O)}$ is a better metric than either $\eta_{I(PZ)}$ or η_C alone. Still, $\eta_{I(PZ)}$ indicates the ability of a system to draw piezoelectric power P_{PZ} and η_C the efficacy with which a system transfers this power.

B. Performance

The 3.3–33 µA (i_{PZ}) that the shaker here induces at 120 Hz (f_{VIB}) charges a 16.8-nF piezoelectric capacitance C_{PZ} across 0.5–5.5 V ($\Delta v_{PZ(OC)}$). With this stimulation, the lossless diode bridge can draw 0.13–15 µW, like $P_{PZ(BRDG)}'$ in Fig. 15 shows. Under the same conditions, the series switched-inductor bridge prototyped here draws 1.2–55 µW (P_{PZ}) and delivers 0.70–49 µW ($P_{O(MPP)}$). So like Fig. 15 shows, the system draws 3.7×–9.8× ($\eta_{I(PZ)}$) and outputs 3.3×–6.8× ($\eta_{I(O)}$) more power than the lossless bridge can and outputs 45%–91% (η_C) of the power drawn.

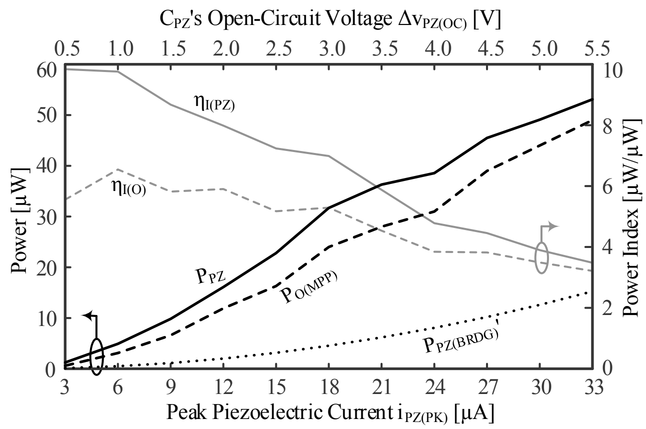

Fig. 15. Measured power and resulting power indices.

Piezoelectric power P_{PZ} overcomes losses when vibrations charge C_{PZ} more than 0.5 V. This 0.5-V threshold corresponds to the minimum vibration strength from which the system can harvest power. Power indices $\eta_{I(PZ)}$ and $\eta_{I(O)}$ are high at 5.9–9.8 and 4.5–6.8 when vibrations charge C_{PZ} across 0.5–3.5 V.

TABLE II: RELATIVE PERFORMANCE

	JSSC [14]	TCAS I [15]	JSSC [16]	TCAS I [17]	JSSC [18]	JSSC [19]	This Work
	Diode Bridge	Half-Switched SL Bridge	SL Half Bridge	Switched-Inductor Recycling Bridges			SL Bridge
L_{MIN}	1 µm	2 µm	180 nm	250 nm	350 nm	350 nm	0.82–1.2 µm
V_{BD}			15 V			5 V	5.5 V
Si Area	4.25 mm²	0.90 mm²	2.3 mm²	0.75 mm²	9.0 mm²	0.54 mm²	0.25 mm²
L_X		160 µH	330 µH	220 µH	1000 µH	3400 µH	330 µH
R_L		3.4 Ω	1.6 Ω			8.1 Ω	1.6 Ω
[A]$i_{PZ(PK)}$	40.7 µA	30.2–104 µA	8.22–35.7 µA	84 µA	1.34–16.1 mA	>9.3 µA	3.0–33 µA
C_{PZ}	12 nF	275 nF	15 nF	19 nF	5200 nF	9.6 nF	16.8 nF
f_{VIB}	225 Hz	100 Hz	143 Hz	144 Hz	82 Hz	230 Hz	120 Hz
$\Delta v_{PZ(OC)}$	4.8 V	0.35–1.2 V	1.22–5.24 V	9.8 V	1.0–12 V	≥ 1.34 V	0.50–5.5 V
$P_{PZ(BRDG)}'$	15.6 µW	0.84–9.9 µW	0.80–15.1 µW	65.7 µW	0.11–15.3 mW	≥0.99 µW	0.13–15 µW
P_{PZ}	8.2 µW	4–72 µW	7–78 µW				1.2–55 µW
P_Q	–	0.7 µW	0.5 µW	1.5 µW	777 nW		Off Chip
$\eta_{I(PZ)}$	53%	4.8×–7.3×	5.4×–11×				3.5×–9.8×
$P_{O(MPP)}$	7.5 µW	1.7–31 µW[B]	2.10–52.5 µW[B]	136 µW	1700 µW	5–410 µW[C]	0.70–49 µW
η_C	90%	42%–50%	30%–67%			50%–96%[C]	45%–91%
$\eta_{I(O)}$	48%	1.2×–3.0×	2.6×–3.5×	2.1×		3.1×[C]–6.8×	3.2×–6.8×
Components	4 FETs MPP Buffer	L_X, 4 FETs	L_X, 2 FETs	L_X, 4 FETs MPP Buffer	L_X, 6 FETs MPP Buffer	L_X, 6 FETs MPP Buffer	L_X, 4 FETs

[A]Calculated from C_{PZ}'s open-circuit voltage variation $\Delta v_{PZ(OC)}$. [B]Increased to discount controller's P_Q. [C]Approximated from reported graphs.

Harvesting performance is lower when vibrations are stronger because the transistors' 5.5-V breakdown voltage V_{BD} limits the voltage v_{PZ} with which i_{PZ} draws P_{PZ}.

Power-conversion efficiency η_C is not as important as $\eta_{I(PZ)}$ and $\eta_{I(O)}$ because η_C does not account for how much power the harvester can draw from motion. η_C is still a good measure of design quality, however, because systems output more power when optimally designed to balance losses. In this case, η_C is 75%–91% when vibrations charge C_{PZ} more than 3 V. η_C falls to 45% below 1 V because gate-drive and shoot-through losses P_G and P_{ST}, which do not scale down with P_{PZ}, dominate when P_{PZ} is low. In other words, the system is more optimal for higher P_{PZ}.

C. Relative Performance

Diode bridges output less power than switched-inductor (SL) bridges because the voltage v_{PZ} with which piezoelectric current i_{PZ} generates power P_{PZ} is lower in diode bridges than the voltage $\Delta v_{PZ(OC)}$ that i_{PZ} charges C_{PZ} across a half cycle in switched inductors [37]. Plus, and this is also why v_{PZ} never reaches $\Delta v_{PZ(OC)}$ in diode bridges, diode bridges collect a fraction of the charge that i_{PZ} outputs. The diode bridge [14] in Table II, for example, draws 53% and outputs 48% of the power that the lossless diode bridge can transfer. Table II summarizes steady-state performance across vibration cycles. Since the controller here is off chip, parameters $P_{O(MPP)}$, η_C, and $\eta_{I(O)}$ in the table discount the power consumed by the controller. This way, the table compares the performance of the power stage only (without the controller).

The half-switched switched-inductor diode bridge in [15] draws 4.8×–7.3× and outputs 1.2×–3.0× more power than the lossless diode bridge can because the system collects all the charge that i_{PZ} outputs with a higher voltage (that is as high as $\Delta v_{PZ(OC)}$). The switched-inductor half bridge in [16] draws and outputs more power (5.4×–11× and 2.6×–3.5×) because the system charges C_{PZ} above $\Delta v_{PZ(OC)}$. The recycling switched-inductor bridges in [17]–[19], [38]–[41] draw and output even more power because v_{PZ} is, on average, greater than the others. The redeeming advantage of the diode bridge is that it does not require a controller, so quiescent losses are absent.

The switched-inductor bridge prototyped here outputs up to 6.8× more power than the lossless bridge can. This is as much power as the recycling bridge in [19] outputs, but with four fewer power switches. In addition to the six switches that the rectifier uses, [19] also requires a two-switch bucking power stage to keep the rectified level at the maximum power point.

Reported silicon areas are not comparable because the minimum channel length L_{MIN} for the 5-V 0.54-mm2 switches in [19] is 350 nm and L_{MIN} for the 5.5-V 0.25-mm2 transistors here is 1.2 μm for NFETs and 810 nm for PFETs. Plus, the switches in [19] transfer 410 μW and the transistors here transfer 49 μW. Still, four fewer power transistors without a separate MPP power stage under similar constraints should consume less power, and as a result, deliver more of the power drawn. This is probably why the minimum harvestable voltage $\Delta v_{PZ(OC)}$ here is 840 mV lower at 500 mV than the 1.34 V needed in [19].

V. Conclusions

The switched-inductor bridge presented here draws 1.2–55 μW and outputs 0.70–49 μW with the 3.3–33 μA that a vibrating 16.8-nF piezoelectric transducer generates at 120 Hz to charge the transducer across 0.5–5.5 V. The prototype draws 3.7×–9.8× and outputs 3.3×–6.8× more power than a lossless diode bridge can. This is as much power as the best recycling switched-inductor bridge outputs, but with four fewer power switches and without a separate maximum power-point stage. This is possible because, before every half cycle begins, the single-inductor four-switch network pre-charges the transducer to an adjustable voltage. This way, the system can deliver as much power as power losses and breakdown voltage allow. Drawing maximum power is important because small piezoelectric transducers couple a very small fraction of the mechanical power that vibrations supply. Replenishing the energy that drains tiny onboard batteries with higher power extends the cost-, energy-, and life-saving features that biomedical implants and wireless microsensors networked across fields, factories, hospitals, and homes can offer.

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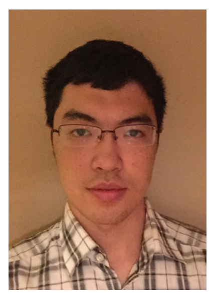

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