87%-Efficient 330-mW 0.6-µm Single-Inductor Triple-Output Buck–Boost Power Supply

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***Abstract*—Microsystems that sense, process, and communicate data can save money, energy, and lives. Such varied functionality, however, demands power that can easily deplete a small battery. Integrating so many analog and digital functions can also imperil performance with noise and distortion. To survive all this with an exhaustible battery, blocks require several efficient power supplies that both buck and boost the battery voltage. Luckily, switched inductors are flexible and efficient, but also bulky. So what these microsensors need are single-inductor multiple-output supplies that buck *and* boost. But to reconfigure the inductor for such diverse operation requires many power-consuming switches. Plus, cycling between outputs requires time and delays response time. The single-inductor supply proposed bucks and boosts and cycles between outputs frequently with two input switches, one inductor, and one switch and one capacitor per output. Other buck–boost supplies either bypass the inductor or require one to two more switches and up to one more inductor and one more capacitor. The prototype presented here bucks two outputs and boosts one output with five switches by energizing the inductor to buck outputs first. By collecting sufficient energy this way, the inductor can feed boost outputs directly. A sixth switch engages only when boost power is greater than a threshold that the input voltage and buck power levels establish. This way, the 0.6-µm CMOS system bucks and boosts 2.7–4.0 V to 1.2, 1.8, and 4.0 V to deliver 80%−87% of the 379–412 mW drawn. The system cycles every 1–3 µs and responds within 5–10 µs.**

***Index Terms*— Buck–boost, single inductor, multiple output, dc–dc power supply, and hysteretic current-mode control.**

I. Powering Wireless Microsystems

MICROSYSTEMS that sense, process, store, and transmit information incorporate sensors, amplifiers (A_V), analog–digital converters (ADC), digital-signal processors (DSP), memory, and power amplifiers (PA) like Fig. 1 shows [1]–[2]. Unfortunately, the battery that supplies them is small. DSPs and PAs can also be so noisy that discerning, amplifying, and converting sensor signals can be challenging.

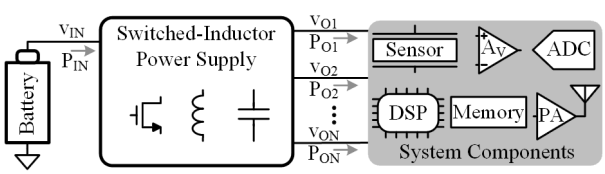

Fig. 1. Power-efficient wireless microsystem.

Designing one power supply to meet the power and noise demands of *all* system components might not be possible. DSPs, for example, are low voltage and noise tolerant, so noisy 0.5–1-V power supplies can drive them [3]–[4]. Sensors and ADCs, on the other hand, usually require higher supplies with lower noise content [5]. And to drive the 1–10 mW that antennas require, PAs often need 4–5 V [6]. This is why many applications call for multiple buck and boost supplies [7]–[8].

Although linear regulators are fast, they are lossy and can only buck [9]. Switched networks are not as fast, but they can buck and boost and burn less power [10]. But with so many switches and switching configurations, switched capacitors are usually less accurate and more lossy than switched inductors [11]. Inductors, however, are bulky [12], which is the reason using only one inductor is so appealing [13].

The system presented here does this: uses one inductor to buck and boost a battery voltage to three outputs. [20], [21], [22], and [23] are also switched inductors that buck and boost. Common requirements to all these supplies are two switches, one switched inductor, and one switch and one capacitor per output. Plus, [20] requires one more inductor, one more capacitor, and two more switches. The additional overhead for [21] is lower with one more switch. Although [22]–[23] do not need additional components, one of the switches in [22]–[23] bypasses the power inductor when buck power surpasses a threshold, which altogether eliminates the efficiency benefit of the switched inductor. The system proposed here does not require additional overhead, and only uses one more switch (that does not bypass the inductor) when boost power surpasses a threshold.

The fundamental advantages of fewer inductor-switching components are lower cost, lower volume, and because every device incorporates parasitic resistances that burn power, lower losses, and as a result, higher efficiency. Like Section II describes, the proposed single-inductor multiple-output (SIMO) system cycles between outputs often with the least number of switches possible. That way, like Sections III–V then explain, the system responds quickly and with lower losses.

II. One-Inductor Triple-Output Buck–Boost Supply

Single-inductor multiple-output (SIMO) power supplies save space at the expense of accuracy and efficiency. Accuracy is worse because, while the switched inductor feeds one output, other outputs droop. So with more outputs, voltage ripples are generally higher. Power-conversion efficiency also suffers because, to reconfigure the system to feed several outputs, the system requires several power-hungry switches. Minimizing these sacrifices first hinges on conduction sequence.

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A. Conduction Sequence

Switched inductors deliver power by energizing and draining an inductor L_O from an input source v_{IN} into an output v_O in alternating phases of a switching sequence. Dedicating one energize–drain sequence to each output is one way of supplying several loads. Feeding all outputs within one energize–drain sequence, however, is more accurate and efficient because wait times between connections are shorter and with fewer connection events [14]–[15].

The buck–boost supply in Fig. 2, for example, closes M_{IN} and M_1 first to energize L_O from the input v_{IN} into the first output v_{O1}. L_O's current i_L and v_{O1} in Fig. 3 therefore rise past 450 ns. When v_{O1} reaches its 1.84-V target v_{T1}, after t_1, M_1 opens and M_2 closes to supply v_{O2}. But since L_O still does not hold enough energy to feed the rest of the loads, M_{IN} continues to energize L_O. As a result, i_L and v_{O2} both rise after 1.25 µs.

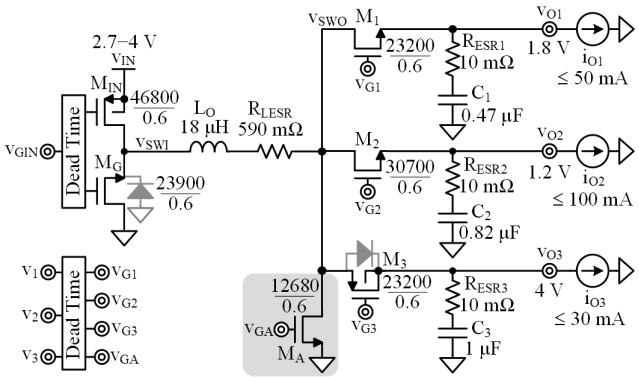

Fig. 2. One-inductor triple-output buck–boost power supply.

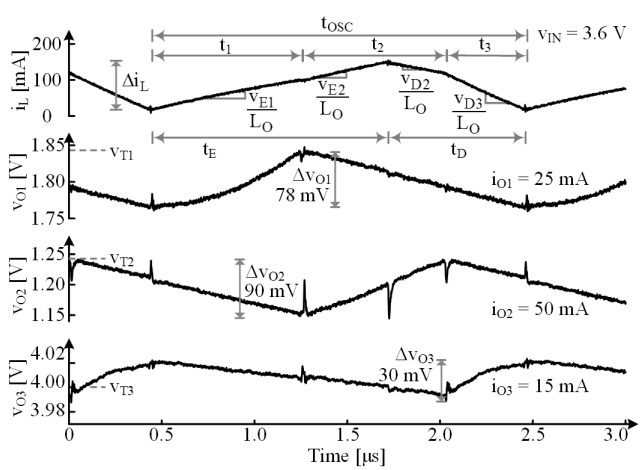

Fig. 3. Measured waveforms when operating in the five-switch mode.

When L_O holds enough energy to feed the rest of the loads, M_{IN} opens and M_G closes to begin draining L_O. So i_L starts to fall at 1.75 µs. But since M_2 still supplies v_{O2}, v_{O2} continues to climb. When v_{O2} reaches its 1.24-V target v_{T2} (at 2.05 µs), M_2 opens and M_3 closes to feed v_{O3}. v_{O3} therefore rises until the feedback controller finishes draining L_O at 2.45 µs. This way, L_O feeds all outputs across one energize–drain sequence.

Since M_1 and M_2 feed buck outputs, they can be NFETs. M_3 is a PFET because v_{O3} is high. To avoid shorting v_{IN} to ground, M_{IN}'s and M_G's gate signals include a dead period across which M_G's body diode conducts i_L. M_1's, M_2's, and M_3's gates similarly incorporate a dead time to keep M_1, M_2, and M_3 from shorting their outputs. But since i_L must nevertheless flow, M_3's bulk connection to v_{O3} adds a body diode that conducts i_L to v_{O3} through this dead-time period.

L_O operates in discontinuous conduction when loads are so light that L_O can satisfy them with small and infrequent energy packets. Still, the operation is generally the same. In Fig. 4, for example, L_O energizes to v_{O1} across t_1 and v_{O2} for part of t_2. Then, M_{IN} opens and M_G closes to drain L_O to v_{O2} for the remainder of t_2 and to v_{O3} across t_3. In this mode, the energy the outputs receive is sufficient to satisfy them for the rest of the oscillating period t_{OSC}. The sequence repeats after that.

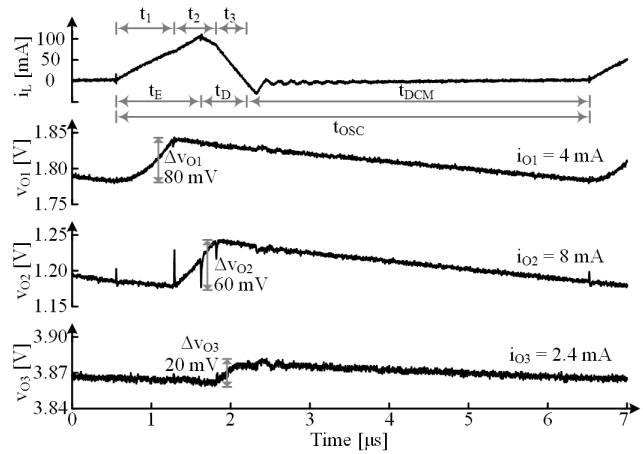

Fig. 4. Measured waveforms in discontinuous conduction.

B. Five-Switch Mode

L_O can energize and drain into any buck output v_{BK} because L_O's energizing voltage v_E or $v_{IN} - v_{BK}$ is always positive and L_O's drain voltage v_D or $0 - v_{BK}$ is always negative. Without M_A, however, L_O can drain, but not energize into a boost output v_{BT} because $v_{IN} - v_{BT}$ is negative. But if L_O energizes sufficiently into buck outputs, L_O can drain into boost outputs. This is why L_O in Figs. 2–4 can drain into v_{O3}'s boosted 4.0 V.

Limit: L_O can feed v_{O3} this way only if, after supplying v_{O1} and v_{O2}, L_O can still satisfy v_{O3}'s load P_{O3} across the time t_3 that L_O feeds v_{O3}. To determine this limit, first consider that the feedback controller ensures L_O delivers enough current to satisfy all outputs. With that much current, L_O connects to each output v_{OX} the fraction d_{OX} of the oscillating period t_{OSC} that i_L requires to satisfy each load i_{OX}. When i_L's ripple is much lower than i_L's average, d_{OX} is nearly the fraction of current that i_{OX} demands of all the loads combined Σi_{OX}:

$$d_X \equiv \frac{t_X}{t_{OSC}} = \frac{t_X}{\sum t_X} = \frac{t_X}{t_1 + t_2 + t_3} \approx \frac{i_{OX}}{\sum i_{OX}} = \frac{i_{OX}}{i_{O1} + i_{O2} + i_{O3}}. \quad (1)$$

L_O can supply the most P_{O3} when L_O energizes the entire time L_O connects to v_{O1} and v_{O2} and drains the entire time L_O connects to v_{O3}. But to balance i_L, i_L must rise as much as i_L falls across t_{OSC}. i_L must therefore climb Δi_L with v_{O1}'s and v_{O2}'s energizing voltages v_{E1} and v_{E2} or $v_{IN} - v_{O1}$ and $v_{IN} - v_{O2}$ and fall Δi_L with v_{O3}'s drain voltage v_{D3} or $-v_{O3}$:

$$\Delta i_L = \left| \left(\frac{v_{E1}}{L_O} \right) t_1 + \left(\frac{v_{E2}}{L_O} \right) t_2 \right| \equiv \left| \left(\frac{v_{D3}}{L_O} \right) t_3 \right|. \quad (2)$$

When factoring L_O out and noting t_1, t_2, and t_3 relate like i_{O1}, i_{O2}, and i_{O3}, the expression reveals that, of the power v_{IN} supplies with i_{O1} and i_{O2}, v_{O3} receives as P_{O3}' what v_{O1} and v_{O2} do not collect with P_{O1} and P_{O2} or $v_{O1}i_{O1}$ and $v_{O2}i_{O2}$:

$$v_{O3}t_3 \approx v_{IN}\left(t_1+t_2\right)-v_{O1}t_1-v_{O2}t_2$$
$$v_{O3}i_{O3} \approx v_{IN}\left(i_{O1}+i_{O2}\right)-v_{O1}i_{O1}-v_{O2}i_{O2}\,. \qquad (3)$$
$$P_{O3}' \approx v_{IN}\left(i_{O1}+i_{O2}\right)-\left(P_{O1}+P_{O2}\right)$$

The system, however, loses power to the controller and switches. To generalize and adjust for losses, of what v_{IN} supplies with buck currents Σi_{BK}, boost outputs can receive as $\Sigma P_{BT}'$ what buck outputs and losses do not consume with ΣP_{BK} and P_{LOSS}:

$$\sum P_{BT}' = v_{IN}\sum i_{BK} - \sum P_{BK} - P_{LOSS} = \left(v_{IN}\sum i_{BK}\right)\eta_C - \sum P_{BK}\,, \qquad (4)$$

where $(v_{IN}\Sigma i_{BK})\eta_C$ is the fraction of v_{IN}'s power not lost to P_{LOSS}.

Since v_{IN} is greater than all buck outputs, v_{IN}'s buck power $v_{IN}\Sigma i_{BK}$ climbs faster with buck currents Σi_{BK} than buck power ΣP_{BK}. Boost power limit $\Sigma P_{BT}'$ therefore rises with buck currents. This is why the six-switch boundary that v_{O3}'s boost power limit P_{O3}' establishes in Fig. 5 increases with input voltage v_{IN} and buck currents i_{O1} and i_{O2}. This is another way of saying total buck power limits boost power.

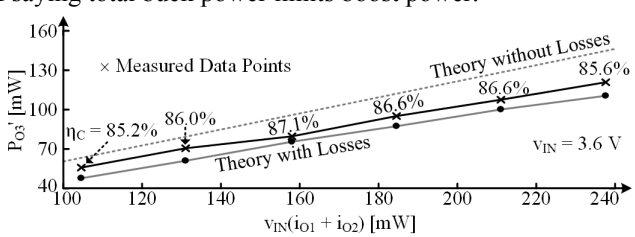

Fig. 5. Theoretical and measured maximum boost power with five switches.

C. *Six-Switch Mode*

If v_{IN}'s buck power is not sufficient to supply boost power, M_A in Fig. 2 can help. So if after energizing to buck outputs L_O's energy is not enough to supply boost outputs, M_A can energize L_O further. In Fig. 6, for example, M_{IN} and M_1 and M_2 first energize L_O into v_{O1} and v_{O2} across t_1 and t_2. But since energy in L_O is not enough, M_2 opens and M_A closes. In this way, L_O continues to energize (from v_{IN} to ground). Then, with sufficient energy in L_O, M_A opens and M_3 closes to feed v_{O3}. Note M_A only closes during the energizing phase, when M_{IN} energizes L_O. In other words, M_A does not close when M_G conducts, so L_X never freewheels current.

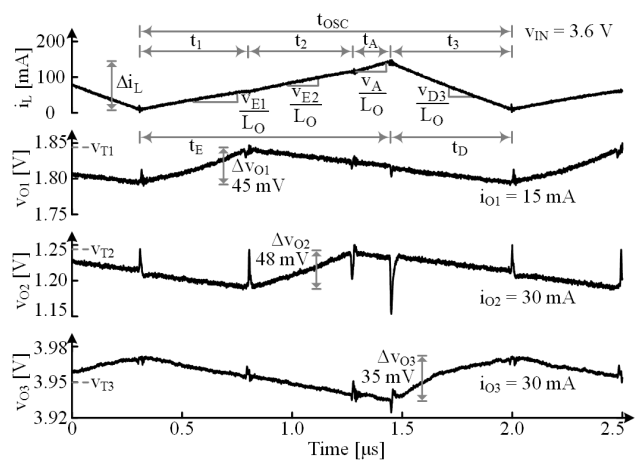

Fig. 6. Measured waveforms when operating in the six-switch mode.

When v_{O3}'s load i_{O3} just rises above the five-switch limit P_{O3}' in discontinuous conduction, v_{O3} needs M_A's assistance, but at first, only occasionally. In Fig. 7, for example, v_{O3} requires additional energy every other cycle: every 50 µs. That is in addition to the energy packet v_{O1}, v_{O2}, and v_{O3} receive every 25-µs cycle. When i_{O3} rises above a threshold level, v_{O3} starts receiving energy every cycle. At that point, L_O operates more like Fig. 6 shows, but with intervening zero-current time gaps t_{DCM} between energy packets like Fig. 4 illustrates.

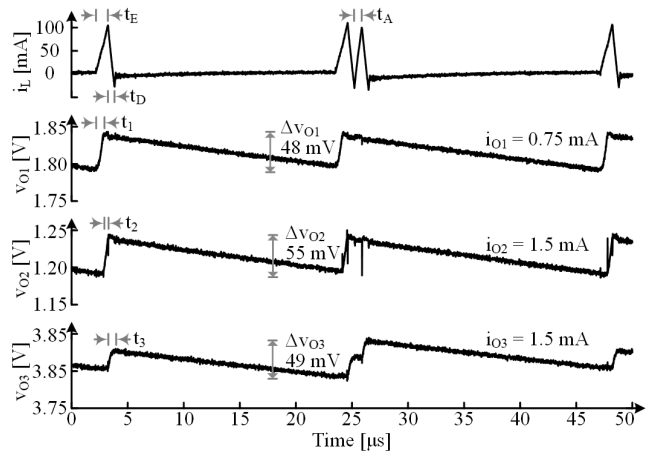

Fig. 7. Measured six-switch waveforms in discontinuous conduction.

When M_A energizes L_O, none of the outputs receive power. As a result, all outputs droop across t_A in Fig. 6, and accuracy suffers. Engaging M_A also requires power that adds to losses in P_{LOSS}. So power-conversion efficiency η_C also drops. This is why η_C in Fig. 8 for the supply in Fig. 2 is generally higher when operating in the five-switch mode, maxing at $\eta_{C(PK)}$ or 87%. When delivering the same total current, η_C is 2% to 3% higher with five switches than with six. Full-load efficiency $\eta_{C(FL)}$ when i_{O1}, i_{O2}, and i_{O3} are 50, 100, and 30 mA is 81%.

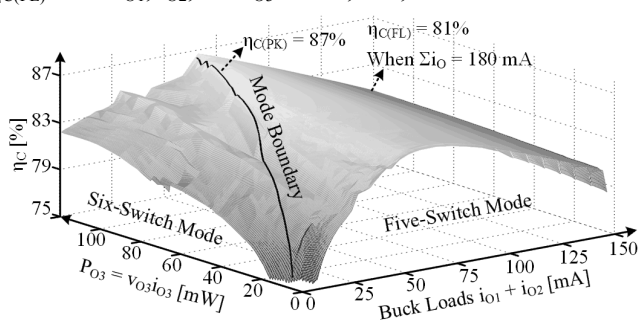

Fig. 8. Measured power-conversion efficiency across load power.

III. Feedback Controller

A. *Five-Switch Mode*

The fundamental drawback of sharing one inductor L_O is that each output receives L_O's current i_L less frequently. To minimize this sacrifice, the feedback controller should be fast. This is why the triple-output buck–boost power supply in Fig. 9 adapts the controller in [16] to include M_A. This way, M_1 feeds L_O to v_{O1} until comparator CP_1 senses that v_{O1} reaches target v_{T1}. M_2 then feeds L_O to v_{O2} until CP_2 similarly senses v_{O2} reaches v_{T2}. M_3 ends the sequence by directing L_O to v_{O3}.

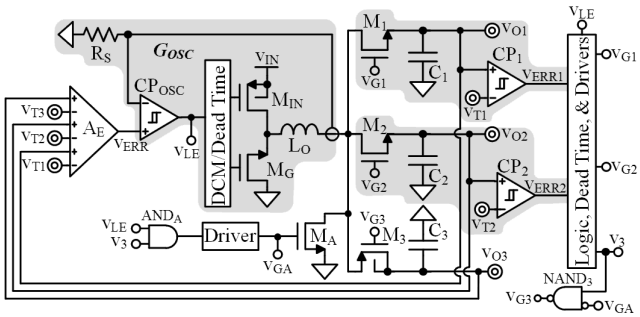

Fig. 9. Triple-output buck–boost switched-inductor power-supply system.

Here, G_{OSC} is a hysteretic oscillator that ripples i_L about a level that the error amplifier A_E dictates. CP_1 and CP_2 close independent loops that ensure v_{O1} and v_{O2} peak at v_{T1} and v_{T2}. A_E senses all outputs to generate an error v_{ERR} that adjusts i_L so that, after satisfying v_{O1} and v_{O2}, i_L can still supply P_{O3}.

i_L's rising and falling rates limit how fast G_{OSC} responds, which is as fast as any switched inductor can [17]. C_1 and C_2 similarly limit how fast v_{O1} and v_{O2} can reach their targets, which again is the fastest possible [10]. Since G_{OSC} is essentially a rippling transconductor with high bandwidth f_{IBW}, L_O behaves like a current source up to f_{IBW}. C_3 therefore sets a dominant low-frequency pole that ensures the loop gain of the master loop (with A_E) reaches unity near f_{IBW}. This way, the closed-loop bandwidth of the system is near f_{IBW}, which is as high as a current-mode power supply can [9].

B. Six-Switch Mode

If CP_{OSC} does not stop energizing L_O by the time L_O satisfies v_{O2}, AND_A invokes M_A's assistance. For this, $NAND_3$ keeps M_3 from opening, and instead, directs L_O to ground. L_O therefore continues to energize to ground until CP_{OSC} opens M_{IN} to stop energizing L_O. At that point, AND_A opens M_A and $NAND_3$ closes M_3 to supply v_{O3}.

Like in boost converters, disconnecting all outputs to energize L_O introduces an out-of-phase right-half-plane zero z_{RHP}. This is because, while energizing L_O with M_A, which without z_{RHP} should raise v_{O3}, load i_{O3} discharges C_3. In other words, what should raise v_{O3} also lowers v_{O3}. z_{RHP} therefore appears at the frequency when the fall exceeds the rise [10].

To find z_{RHP}, first consider that L_O's energizing and drain voltages v_E or v_{IN} and v_D or $-v_{O3}$ across L_Os and across and after M_A's connection time t_A set how much additional current L_O collects i_l [10]. The fraction of the oscillating period t_{OSC} that L_O connects to v_{O3}: d_3 or t_3/t_{OSC}, determines how much of i_l reaches v_{O3}. So a rise in t_A ultimately delivers i_{l+} to v_{O3}:

$$i_{l+} = i_l d_3 = d_a\left(\frac{v_E - v_D}{L_O s}\right)\left(\frac{t_3}{t_{OSC}}\right) \approx \left(\frac{t_a}{t_{OSC}}\right)\left(\frac{v_{IN} + v_{O3}}{L_O s}\right)\left(\frac{i_{O3}}{\sum i_{OX}}\right). \quad (5)$$

The current M_A sinks, however, does not reach v_{O3}. This current: i_{lA}, is the charge i_L supplies at its peak $i_{L(PK)}$ across t_a:

$$i_{l-} = \frac{q_{l-}}{t_{OSC}} \approx \frac{i_{L(PK)} t_a}{t_{OSC}} = i_{L(PK)} d_a . \quad (6)$$

The loop is inverting as long as i_{l+} surpasses i_{l-}. But since i_{l+} drops with frequency s, v_{O3} inverts when i_{l+} falls below i_{l-}. This means that z_{RHP} appears when i_{l-} matches and exceeds i_{l+}:

$$z_{RHP} \approx \left(\frac{v_E - v_D}{2\pi L_O i_{L(PK)}}\right) d_3 \approx \left(\frac{v_{IN} + v_{O3}}{2\pi L_O i_{L(PK)}}\right)\left(\frac{i_{O3}}{i_{O1} + i_{O2} + i_{O3}}\right). \quad (7)$$

For the system to remain stable, z_{RHP} must therefore surpass the closed-loop bandwidth by maybe 10×. z_{RHP}, however, falls with i_{O3}'s fraction of the total load $i_{O1} + i_{O2} + i_{O3}$. So the system is more stable and can therefore be faster when i_{O3}'s fraction is higher. But z_{RHP} and the condition it carries only apply to the six-switch mode, so the worst-case stability condition is near the five–six boundary in Figs. 5 and 8, where i_{O3}'s fraction is just high enough to warrant six-switch operation. And it only applies in continuous conduction because L_O delivers all the energy L_O collects in discontinuous conduction [18].

IV. Prototype

A. Hardware

The 0.6-µm CMOS die in Fig. 10 integrates the power stage in Fig. 2 and the controller in Fig. 9, except for the current sensor, 18-µH inductor L_O, and 0.47-, 0.82-, and 1-µF capacitors C_1, C_2, and C_3. Aside from the integrated circuit (IC), L_O, C_1, C_2, and C_3, the board also includes test and load circuits. The die, L_O, and each of the capacitors occupy 2.0 × 1.4 mm^2, 3.5 × 2.7 × 2.4 mm^3, and 1.6 × 0.81 × 0.91 mm^3. With these dimensions, L_O's equivalent series resistance (ESR) is 590 mΩ and those of C_1, C_2, and C_3 are 10 mΩ.

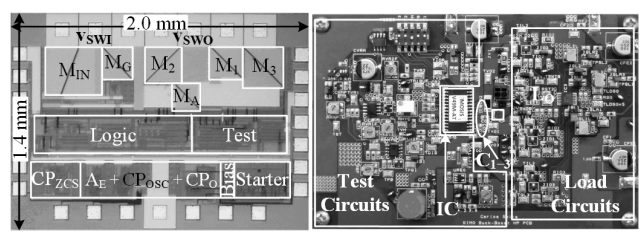

Fig. 10. Prototyped 0.6-µm CMOS die and two-layer board.

B. Output Regulation

In the five-switch mode, independent comparators CP_1 and CP_2 and master error amplifier A_E ripple v_{O1}, v_{O2}, and v_{O3} in Fig. 3 across 78, 90, and 30 mV about their 1.8-, 1.2-, and 4-V targets. Output ripples in Fig. 6 are 45, 48, and 35 mV in the six-switch mode, when v_{O3}'s boost power P_{O3} surpasses the threshold P_{O3}' that input voltage v_{IN} and v_{O1}'s and v_{O2}'s buck loads set in Fig 5. In discontinuous conduction, ripples in Figs. 4 and 7 are 80, 60, and 20 mV with five switches and 48, 55, and 49 mV with six switches. v_{O1}'s and v_{O2}'s ripples are lower and v_{O3}'s ripple is higher with six switches because, to be in the six-switch mode, v_{O1}'s and v_{O2}'s buck loads pull less current and v_{O3}'s boost load pulls more current.

Parasitic bond-wire and capacitor inductances L_{BW} and L_{ESL} produce voltage spikes in the outputs when M_1, M_2, and M_3 re-direct L_O's currents between outputs. This is because switch and capacitor currents change drastically across those transitions. Just before M_1 closes, for example, M_1 conducts no current and C_1 supplies v_{O1}'s full load. But when M_1 closes at 0.4 µs in Fig. 3, M_1 conducts all of L_O's i_L to both supply the load and recharge C_1, which reverses C_1's current. These drastic changes in current produce transient voltages across M_1's L_{BW1} and C_1's L_{ESL1} that spike v_{O1}. M_2's and M_3's L_{BW2},

L_{BW3}, L_{ESL2}, and L_{ESL3} similarly spike v_{O2} and v_{O3} when M_2 and M_3 switch on and off.

The outputs also receive cross-coupled noise every time the switching nodes v_{SWI} and v_{SWO} in Fig. 2 transition: when t_1, t_2, t_3, and t_E end in Figs. 3–4 and 6–7. v_{SWI} and v_{SWO} generate substantial noise because they carry up to 200 mA and swing between 0, 1.2, 1.8, and 4 V. v_{O2} suffers the most because M_2 in Fig. 10 is between v_{SWI}'s pin, which connects to M_{IN} and M_G, and v_{SWO}'s pin, which connects to M_2, M_3, and M_A. M_2 is so close to v_{SWI} and v_{SWO} that noise spikes in v_{O2} are more prevalent and severe than in v_{O1} and v_{O3}.

C. Dynamic Performance

When all loads suddenly rise four times their initial 12.5-, 25-, and 7.5-mA levels, the system responds in 5.2 µs and all outputs settle within another 15 µs, as Fig. 11 shows. The system similarly responds in 5.4 µs and all outputs recover within another 40 µs when those same loads return to their initial levels. The system requires more time to settle after the loads disappear because, with such a light load, C_3 slews slowly back to its target. Irrespective of direction, v_{O3} suffers the most variation at 176 and 268 mV because the controller, by design, feeds and satisfies v_{O1} and v_{O2} first.

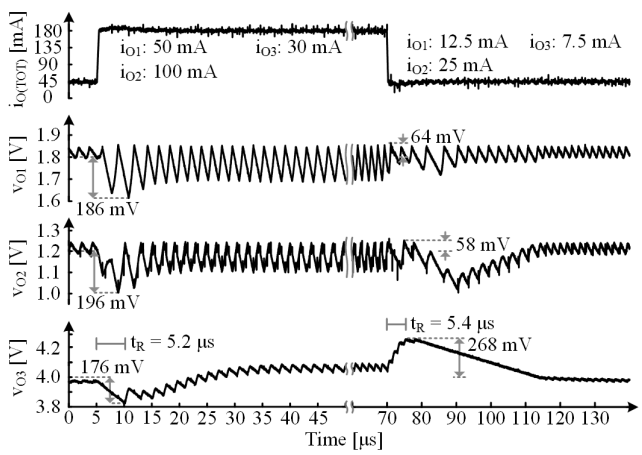

Fig. 11. Measured load-dump response when operating with five switches.

The system responds a little less quickly when operating in the six-switch mode. This is because connecting L_O to ground requires additional time. So when subjected to the sudden 1.67× load variations in Fig. 12, the system responds in 6.2–7 µs and outputs settle within another 17–20 µs.

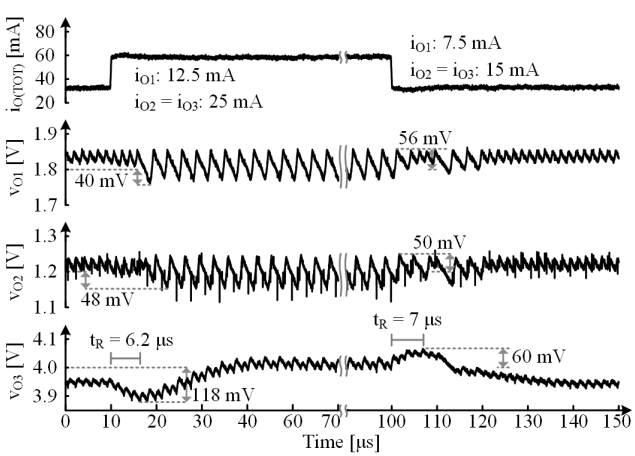

Fig. 12. Measured load-dump response when operating with six switches.

Transitioning between modes adds additional overhead. So when responding to v_{O3}'s 3–30-mA load dumps in Fig. 13, the system responds in 8–10 µs and outputs settle within another 20–26 µs. Notice, however, v_{O3} over-reacts before finally settling. This is because z_{RHP} reduces the phase margin of the system. Still, the system recovers within one or two rings, which corresponds to 60° to 70° of phase margin [19].

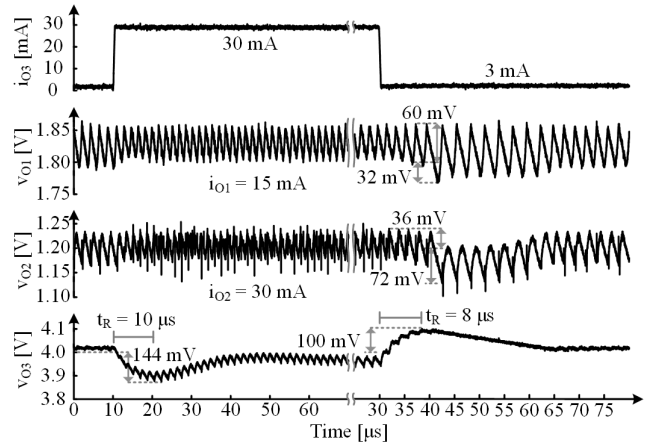

Fig. 13. Measured load-dump response across switching modes.

V. State-of-the-Art Comparison

A. Relative Figure of Merit

Comparing the state of the art (SoA) is difficult because too many metrics describe the performance of a switched-inductor power supply. Plus, tradeoffs between metrics obscure the absolute significance of individual parameters. Lower dimensions, for example, translate to higher resistances, which means efficiency suffers with higher integration. The importance and relative weight of each parameter can also vary widely from one application to the next. Still, combining independent parameters, removing redundancies, and comparing technologies under equivalent operating conditions and uniform weights can be useful. So for the purposes of the following discussion, all independent parameters carry equal weight.

A multiple-output inductor is more appealing when it supplies higher total current $i_{O(MAX)}$ and more outputs N_O with higher power-conversion efficiency η_C. Although η_C can be more important and relevant to a particular application at one particular level, peak and full-load efficiencies $\eta_{C(PK)}$ and $\eta_{C(FL)}$ reflect what is possible when optimized and stretched to output as much power as possible. And although maximum output-voltage variation $\Delta v_{O(MAX)}$ is important, $\Delta v_{O(MAX)}$ ultimately depends on output capacitance C_O, maximum load dump $\Delta i_{O(MAX)}$, and response time t_R. t_R, however, is largely independent of the others. Plus, given t_R and any of the other two, the third is simply their consequence. So of these, t_R is arguably the one that represents the rest.

A power supply is also more attractive when it costs less and occupies less space. In this respect, fewer off-chip components N_{OC} and smaller silicon dies A_{SI} cost and occupy less, and longer channel-length technologies L_{MIN} cost less. Plus, longer L_{MIN} technologies can sustain higher voltages. So assuming all these parameters are equally significant, an all-encompassing figure of merit FoM should rise with higher

$i_{O(MAX)}$, N_O, $\eta_{C(PK)}$, $\eta_{C(FL)}$, and L_{MIN} and lower t_R, N_{OC}, and A_{SI}. Normalizing the FoM to one point of reference PoR reveals a relative FoM or RFoM that is useful when comparing devices:

$$\text{RFoM} \equiv \frac{\text{FoM}}{\text{PoR}} \equiv \frac{i_{O(MAX)} N_O \eta_{C(PK)} \eta_{C(FL)} L_{MIN}}{t_R N_{OC} A_{SI} \text{PoR}}, \quad (8)$$

where PoR is the FoM of the supply referenced in the comparison.

B. The State of the Art

Table I summarizes the state of the art in switched inductors with multiple outputs that can both buck and boost voltages. Unfortunately, of the parameters assessed in the FoM, response time t_R is largely absent in literature. Still, literature reports enough metrics for the FoM and RFoM to be of value.

TABLE I. STATE-OF-THE-ART COMPARISON

	[20]	[21]	[22]	[23]	Proposed
L_{MIN}	0.5 µm	0.25 µm	0.25 µm	0.25 µm	0.6 µm
A_{SI}	3.6 mm^2	10 mm^2	2.1 mm^2	3.8 mm^2	[B]2.94 mm^2
N_O	5	4	2	4	3
N_{OC}	10	5	3	5	4
$i_{O(MAX)}$	145 mA	650 mA	240 mA	400 mA	180 mA
$\eta_{C(PK)}$	83%	91%	92%	93%	[C]87%
$\eta_{C(FL)}$	[A]	74%	92%	92%	[C]81%
t_R	[A]	10 µs[2]	[A]	[A]	10 µs
RFoM	[C]35%	45%	[C]83%	[C]92%	100%

[A]Not reported. [B]Adjusted to include current sensor. [C]Excludes unreported data.

For testing purposes, the prototyped die here excludes the current sensor. This exclusion distorts efficiency and silicon area. Output power and ohmic losses, however, are usually so high at peak and full-load conditions that current-sensor power becomes a negligible fractional loss [22]. And power switches and the controller are typically so large that the current sensor occupies less than 5% of the die [23]. Table I compensates for this distortion in silicon area by increasing A_{SI} 5%: from 2.8 to 2.94 mm^2.

Overall, [20] scores 65% lower than the system here because [20] requires 1.5× more off-chip parts per output. [21] is better than [20], but still 55% lower overall. This is largely because, despite channel lengths being 2.4× shorter, silicon area per output is still 2.7× greater. Plus, [21]'s efficiency is low because the inductor freewheels current that the controller regulates and the output does not receive, so losses are higher. [22]'s rating is 17% lower mainly because channel lengths are 2.4× lower, so cost is higher and breakdown voltage is lower. Although [23]'s efficiency and maximum current are higher, [23] still scores 8% lower. The reason for this is silicon area per output is about the same even when channel lengths are 2.4× shorter.

Without response times, [20]'s, [22]'s, and [23]'s scores are unfortunately incomplete. Plus, test conditions are neither standard nor uniform. Irrespective of this, one of the features of the system presented here is speed. Because when subjected to load dumps, the hysteretic oscillator that sets L_O's current i_L slews i_L to its target. This is as fast as any switched inductor can possibly respond. Pulse-width-modulated systems require more time because they raise i_L after several clock cycles [24].

More fundamentally, the key innovation here is how to buck and boost with fewer inductor-switching components. The basic benefit is power-conversion efficiency η_C because fewer switches (that do not bypass the inductor) consume less power. This is why power efficiency in Fig. 8 is generally higher when operating with five switches than with six. Discerning this benefit from η_C alone in Table I is elusive, however, because the number of components, physical size of components, feedback control scheme, minimum channel length, load levels, and other process-dependent parameters and features all affect η_C. Still, eliminating the need for the additional inductor, capacitor, and two switches that [20] requires, the one more switch that [21] needs, and replacing the switch in [22]–[23] that bypasses the inductor with one that does not would decrease their losses, and as a result, increase their respective efficiencies.

VI. CONCLUSIONS

The single-inductor 0.6-µm CMOS power supply prototyped and presented here draws power from a 2.7–4.0-V battery to supply and regulate 1.2-, 1.8-, and 4-V outputs with up to 180 mA. The design bucks and boosts three outputs with five switches when possible and with six switches only when boost power is a small fraction of the total load. Excluding one switch this way raises power-conversion efficiency 2% to 3% to peak, in this case, with 87% and deliver all 180 mA with 81%. The hysteretic current-mode controller adopted determines when to use the sixth switch automatically and quickly, responding to load dumps with five switches, six switches, and across switch modes within 5.4, 7, and 10 µs. These power-loss and response-time reductions help offset the efficiency and bandwidth that sharing one inductor between several outputs normally sacrifices. This is very important because microsystems cannot fit several bulky inductors.

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