Abstract—Microsystems can sense, process, information between nodes across hospitals, factories, and homes that can save lives, energy, and money. Unfortunately, supplying power with so much embedded functionality is challenging, because while some functions can survive higher noise levels and voltages, others cannot. Power supplies must therefore satisfy several independent outputs without consuming much power or occupying much space. A switched inductor is attractive in this respect because, with only one off-chip inductor, the system can output 80%–90% of the power it draws. Regulating multiple outputs with one inductor, however, links several feedback loops and their reactions to individual and combined loads. The sacrifice for this is usually accuracy in the form of response time. The single-inductor dual-output buck converter presented here uses a hysteretic current loop for this reason: to accelerate the response of the loops used to regulate the outputs. The 0.6-µm CMOS prototype supplies 70 and 50 mA to 1.5- and 2.5-V outputs with 80%–88% power-conversion efficiency and responds to 45–65-mA load dumps within 3.8 µs to keep 1.5 V within ±5% and 2.5 V within ±7%.

Index Terms—DC–DC buck converter, cross regulation, hysteretic current-mode control, single-inductor multiple-output (SIMO), dual output, and switched-inductor power supply.

I. POWERING MULTIFUNCTIONAL MICROSYSTEMS

NETWORKED microsystems that sense, process, store, transmit, and receive information in hospitals, factories, farms, and homes can save lives, energy, and money [1]–[2]. But functions require power, and although digital-signal processors (DSPs) can tolerate some degree of noise in their supplies, sensors and analog–digital converters (ADCs) cannot [3]. Plus tiny batteries cannot sustain power for long, so even though DSPs, ADCs, and power amplifiers (PAs) can tolerate higher voltages, they (for the sake of saving energy) should not [4]. Efficient power-supply systems like Fig. 1 illustrates must therefore supply and regulate several outputs [5]–[6].

![Fig. 1. Multifunctional wireless microsystem.](image)

To save energy, microsystems often idle or disable non-critical blocks [7]. This means, responding to sensed events and load dumps requires short wake-up times. In other words, power supplies must react quickly [8]. Unfortunately, linear regulators, which are fast, are typically inefficient [9], and switched inductors, which are efficient, are normally slow and bulky [10]–[11]. This is why the state of the art relies on one inductor for efficient power conversion and on one or several series low-dropout (LDO) regulators for fast response [12].

Switched inductors are slower than linear regulators because inductor voltages and inductances limit how fast inductor currents change. Plus, several switching cycles elapse before typical digital [13] and pulse-width modulated (PWM) [14]–[15] controllers can respond. Waiting for one switched inductor to respond to one of several loads also requires additional time [16]–[18]. So after one output's load imbalances the inductor, other outputs suffer the irregularity in the form of cross regulation [19]–[21].

The single-inductor dual-output buck converter presented here reduces cycling time by supplying all outputs within one energize/drain sequence of the inductor [22]–[26] and shortens response time by using a hysteretic oscillator to establish the inductor's current [27]. To demonstrate this, Sections II and III explain and show how the system supplies and regulates two outputs with one inductor. Sections IV and V then assess and compare performance with the state of the art.

II. SWITCHED-INDUCTOR DUAL-SUPPLY SYSTEM

The circuit in Fig. 2 essentially transforms inductor L0 into an adjustable current source iL0 that supplies and responds to the demands of two outputs. GOSC is this current source, a transconductor whose current an amplifier AE adjusts. So when first energizing L0, GOSC’s VOSC connects L0 to vO1 until comparator CP01 senses that L0 satisfies vO1. L0 then connects to vO2, and if L0’s leftover energy is insufficient or excessive, AE amplifies vO2’s error to adjust and tune GOSC’s iL0.

Functionally, GOSC is an oscillating current source that implements the function of the current loop in this current-mode system. CP01 closes the independent voltage loop that ensures vO1 peaks near target vR1. AE closes the master loop that adjusts GOSC’s current iL0 to ensure vO2 nears target vR2.

Drivers insert dead times between the conduction periods of adjacent switches M0 and M2 and M0 and M2 to keep them from shorting the input voltage vIN, ground, and vO1 and vO2. M0’s and M2’s body terminals connect to their drains to ensure their body diodes conduct L0’s iL0 during M0’s and M2’s dead-time periods. M0’s driver also opens M0 when L0’s current reaches zero to keep L0 from conducting negative current. This way, in discontinuous-conduction mode (DCM), M0 does not consume unnecessary ohmic power. M0 is an NFET because vIN’s 2.6–4.2 V is high enough above vO1’s

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1.5 V to drive \( M_{O1} \)'s gate. \( M_{O2} \) is a PFET because ground is similarly low enough below \( v_{O2} \)'s 2.5 V to drive \( M_{O2} \)'s gate.

![Fig. 2. Switched-inductor dual-supply hysteretic current-mode system.](image)

**A. Oscillating Current Source**

Continuous Conduction: Comparator \( C_{OSC}, M_R, M_N, L_O, \) and \( R_S \) implement a relaxation oscillator that ramps \( L_O \)'s current \( i_L \) between the hysteretic limits that \( C_{OSC} \) and \( R_S \) establish and about the average that \( A_i \)'s \( v_{ERR2} \) and \( R_S \) set. For this, \( C_{OSC} \) closes \( M_P \) and \( M_{O1} \) to energize \( L_O \) from \( V_{IN} \) to \( v_{O1} \) with energize voltage \( V_E \) or \( V_{IN} - v_{O1} \) until \( i_L \) into \( R_S \) reaches \( C_{OSC} \)'s upper threshold. This is why \( i_L \) in Fig. 3 climbs across energize period \( t_E \). After that, \( C_{OSC} \) opens \( M_P \) and closes \( M_N \) to drain \( L_O \) from ground with drain voltage \( v_{D1} \) or \( 0 - v_{O1} \), and after \( i_L \) satisfies \( v_{O1} \)'s load, into \( v_{O2} \) with \( v_{D2} \) or \( 0 - v_{O2} - i_L \) therefore falls across drain period \( t_D \) first at \( v_{D2}/L_O \) and then at \( v_{D2}/L_O \).

![Fig. 3. Measured waveforms in continuous-conduction mode.](image)

R \( S \) senses \( i_L \) and translates \( C_{OSC} \)'s hysteresis \( V_{HYS} \) and \( A_i \)'s error \( v_{ERR2} \) into currents. \( i_L \) therefore oscillates across \( V_{HYS}/R_S \), and if \( C_{OSC} \)'s thresholds are symmetrical, about \( v_{ERR2}/R_S \). This means, \( i_L \)'s ripple \( \Delta i_L \) is \( V_{HYS}/R_S \), \( i_L \)'s average \( i_{LAVG} \) is \( V_{HYS}/R_S \), and the oscillator's closed-loop gain \( G_{OSC} \) is

\[
G_{OSC} = \frac{i_{LAVG}}{v_{ERR2}} = \frac{1}{R_S}. \tag{1}
\]

Since \( L_O \)'s voltage determines how fast \( i_L \) crosses \( \Delta i_L \), energize voltage \( V_E \) sets \( t_E \), drain voltage \( V_D \) sets \( t_D \), and together, they set oscillating period \( t_{OSC} \)

\[
t_{OSC} = t_E + t_D = \frac{\Delta i_L}{V_E} \left( \frac{L_O}{V_E} + \frac{L_D}{V_D} \right) = \frac{V_{HYS}}{R_S} \left( \frac{L_O}{V_E} + \frac{L_D}{V_D} \right). \tag{2}
\]

Relative load levels dictate the fraction of time \( L_O \) connects to each output. In Fig. 3, for example, \( i_{O1} \)'s 60 mA is 75% of the combined 80-mA load, so \( i_{O1} \)'s connection time \( t_{O1} \) is roughly 75% of \( t_{OSC} \), well past \( L_O \)'s energizing period \( t_E \). As a result, energize voltage \( V_E \) is \( V_{E1} \) or \( V_{IN} - v_{O1} \) and drain voltage \( V_D \) is first \( v_{D1} \) or \( -v_{O1} \) and then \( v_{D2} \) or \( -v_{O2} \). When \( i_{O2} \) is approximately higher than 50% of the combined load, \( v_{O2} \)'s connection time \( t_{O2} \) extends into \( t_E \), so \( V_E \) is first \( v_{E1} \) or \( v_{IN} - v_{O1} \) and then \( v_{E2} \) or \( v_{IN} - v_{O2} \), and \( v_D \) is \( v_{D2} \) or \( -v_{O2} \). This shift in relative connectivity translates to a variation in the oscillating period \( t_{OSC} \) and resulting frequency \( f_{OSC} \) or \( 1/t_{OSC} \).

Discontinuous Conduction: When the combined load is light, the loop lowers \( v_{ERR2} \) to the point \( i_L \) reaches zero before \( i_R \) \( R_S \) reaches \( C_{OSC} \)'s lower threshold. Once at zero, \( M_N \)'s driver opens \( M_N \) to keep \( i_L \) from reversing, so \( v_{O1} \)'s load discharges \( C_{O2} \) past 1.5 \( \mu \)s in Fig. 4 until \( v_{ERR2} \) finally trips \( C_{OSC} \). In other words, \( i_L \)'s lower ripple produces an offset \( (V_{HYS} - \Delta i_R R_S)/A_i \) that \( v_{O2} \)'s fall must overcome to trip \( C_{OSC} \). This means, \( i_{O2} \) reduces \( v_{O2} \)'s lower peak when \( L_O \) is in discontinuous conduction — from 2.5 V in Fig. 3 to 2.44 V in Fig. 4 — and \( i_{O2} \) extends \( t_{OSC} \) to \( t_{OSC}' \):

\[
t_{OSC}' = t_{OSC} + t_{DCM} = t_{OSC} + \left( \frac{V_{HYS} - \Delta i_R R_S}{A_i} \right) \left( \frac{C_{O2}}{i_{O2}} \right). \tag{3}
\]

\( t_{OSC}' \) therefore shorts and \( f_{OSC} \) in Fig. 5 climbs with \( i_{O2} \) until discontinuous time \( t_{DCM} \) in Fig. 4 vanishes, after which \( t_{OSC}' \) levels to \( t_{OSC} \) and \( f_{OSC} \) to \( 1/t_{OSC} \).

![Fig. 4. Measured waveforms in discontinuous-conduction mode.](image)

![Fig. 5. Measured oscillating frequency across modes under balanced loads.](image)

**Bandwidth:** The comparator \( C_{OSC} \), drivers, switches \( M_P \) and \( M_N \), and slew-rate of \( L_O \)'s \( i_L \) determine the oscillator's response time \( t_R \). Of these, \( C_{OSC} \), the drivers, \( M_P \) and \( M_N \), respond in ns and \( i_L \) in \( \mu s \), so \( t_R \) mostly depends on \( L_O \). When rising, energizing voltage \( V_E \) slews \( L_O \), and when falling, drain voltage \( V_D \) slews \( L_O \), so to account for both, \( t_R \) is roughly the average of rise and fall times \( t_{FA} \) and \( t_{FA} [30] \):

\[
t_R = t_{FA} + t_{FA} = \frac{\Delta i_L}{V_E} \left( \frac{L_O + L_D}{V_E + V_D} \right) = \frac{(\Delta V_{ERR2})}{2R_S} \left( \frac{L_O + L_D}{V_E + V_D} \right) \left( \frac{L_O + L_D}{V_E + V_D} \right) \text{ for } \Delta V_{ERR2} < 2V_{HYS}. \tag{4}
\]

So when the oscillator's input steps across a variation \( \Delta V_{ERR2} \) that is less than \( 2V_{HYS}, t_R \) is less than \( t_{OSC} \), which means \( i_L \) reaches its target within one cycle. In other words, the oscillator's bandwidth \( f_{BW} \) is as high as the oscillating frequency \( f_{OSC} \), which is as high as any current loop in a dc–dc converter can claim. What is more, since switching converters cannot outpace their inductors, this oscillating current source is as fast as any current loop can ever be.
B. Independent Peak-Voltage Loop

GoSc in Fig. 2 feeds the independent feedback loop that regulates VO1. Comparator CP0 senses VO1 and VR1 to generate an error vERR that determines when to disconnect L to VO1. This way, CPOSC’s edge-triggered output vOSC first sets MO’s flip-flop to connect L to VO1. LO’s iL raises VO1 past this point, past 0.2 µs in Fig. 3, because iL carries more energy than either output alone requires. When VO1 reaches VR1, CP0 resets MO’s flip-flop to disconnect L from VO1. VO1’s load then discharges CO until vOSC again connects L to VO1.

Stability: GoSc’s iL is essentially an oscillating current source that feeds the loop that regulates VO1. CP0, MO’s flip-flop, MO’s driver, and MO into CO shunt and delay feedback signals across this loop to establish poles. The delays across CP0, the flip-flop, and the driver, however, are a small fraction of the oscillating cycle, so their effects appear well above fOSC. CO, on the other hand, is so high at 470 nF that CO delays and shunts VO1 signals past a pole pO1 that is well below fOSC. So VO1’s loop gain drops at 20 dB/decade past pO1, and because no other delays disturb the fall, reaches unity with nearly 90° of phase margin, which means the loop is stable.

Load Regulation: Since vOSC connects L to VO1 and CP0 disconnects L from VO1 when VO1 rises to VR1, CP0 keeps VO1’s peak near VR1 and VO1’s load drops L across what remains of TOSC after VO1’s connection time tO1 lapses. So as iO1 and iO2 together climb above 25 mA in Fig. 6, VO1’s bottom and average levels droop to lower levels:

\[ V_{O1(AVG)} = V_{R1} \left( 1 - \frac{i_{O1}}{2} \right) \left[ t_{OSC} - t_{O1} \right] \frac{1}{C_{O1}}. \]

In discontinuous conduction, when iO1 and iO2 are both below 25 mA in Fig. 6, raising VO2’s load reduces discontinuous time tDCM in Fig. 4, which shortens TOSC and the time VO1’s load discharges CO. As a result, TOSC’s reduction counters the effect of iO1’s rise on VO1 to produce less variation in VO1’s low and average values. This means, load regulation is worse in continuous conduction.

Load-Dump Compensation: Response time tR in power supplies sets how long load dumps slew their outputs. So after a rising load dump +ΔV0, the difference between the load and iO1 (which is equivalent to ΔiO1) discharges CO1 across tR to produce a falling variation −ΔVL in VO1. After a falling load dump −ΔV0, the difference between iO1 and the load (which is equivalent to ΔiO1) charges CO1 to produce a similar rising variation +ΔVL. Unfortunately, these load dumps are often fast and wide, so +ΔVL can be ±7% to ±10%, high enough to overwhelm other effects and to, alone, limit a supply’s accuracy [28]. This worsens when several outputs share one inductor because cycling between outputs extends tR.

In this case, VO1’s load regulation −ΔVL from Fig. 6 is significant by design. ΔVL, however, does not affect VO1(MIN) because a fast rising load dump normally pulls VO1 well below VR1 − ΔVL to VR1 − ΔVL. But since a falling load dump raises VO1 from its loaded level VR1 − ΔVL, −ΔVL counters +ΔVL to reduce VO1(MAX) to (VR1 − ΔVL) + ΔVL. In other words, load regulation mitigates the effect of the falling load dump [28–29]. So adding a positive offset to VR1 that is similar, but opposite in magnitude to −ΔVL, can reduce VO1(MIN) to VO1 − ΔVL, and when VO1 matches ΔVL, reduce VO1’s total variation ΔVO1(MAX) to

\[ ΔV_{O1(MAX)} = V_{O1(MAX)} - V_{O1(MIN)} = \pm [ΔVL - ΔVL]. \]

This is why VR1 in Fig. 2 is slightly above 1.5 V and VO1 in Figs. 7 and 8 ripples about 1.5 V when loaded with 50 mA.

C. Master Voltage Loop

Since LO carries more energy than either load requires, iL satisfies all small-signal variations in VO1’s load. Insufficient or excess current in LO then produces small-signal alterations in VO2 much like small changes in VO2’s load would. AQ in Fig. 2 senses these variations in VO2 to generate an error vERR2 that adjusts GoSc’s iL until VO2 is again near its target VR2.

Operationally, vOSC feeds MO’s flip-flop to connect L to VO1. When VO1 rises to VR1, CP0 resets MO’s flip-flop to disconnect L from VO1 and sets MO’s flip-flop to close MO and connect L to VO2 after a dead time that the drivers insert. During this dead time, MO’s body diode steers iO2 into VO2. vOSC then resets MO’s flip-flop and sets MO’s flip-flop to reconnect L to VO1 and start another cycle.

Stability: As mentioned earlier, CP0, MO, MP, MN, and LO realize an oscillator GoSc whose output is a current iL that ripples across CP0’s VHY/Rs and about VERR2/Rs. CP0’s, MP’s, and MN’s delays are a small fraction of the oscillating period, so their effects are well above fOSC. But LO is high at 12 µH, so LO and the voltages that VN, VO1, and VO2 impress across LO limit how fast iL responds to VERR2 variations. The resulting delay sets GoSc’s bandwidth [30].

Because LO fully supplies VO1 before feeding VO2, the effect of VO1’s loop on iL is to sink or subtract a portion of iL. In other words, iO1 is essentially another load to LO. This means, the small-signal dynamics of VO1’s loop appear as additional load variations to the loop that senses VO2 to adjust GoSc’s iL.

Ae, GoSc, and CO2 close the loop that feeds VO1’s load and
regulates $v_{O2}$. $C_{O2}$ is high at 560 nF to keep load dumps from deviating $v_{O2}$ too much. This means, $C_{O2}$ shunts $v_{O2}$'s load at a low-frequency pole $p_{O2}$. So to ensure the gain across the loop reaches unity at 20 dB/decade with nearly 90° of phase margin, $A_E$'s and $G_{OSC}$'s bandwidths are, by design, above the unity-gain frequency that $C_{O2}$, by design, establishes.

Load Regulation: Since $A_E$ amplifies $v_{O2}$'s error to continually adjust $G_{OSC}$'s $i_L$, $v_{O2}$'s average $v_{O2}(AVG)$ in Fig. 9 is near $V_{R2}$'s 2.5 V when $L_O$ is in continuous conduction, when both load currents are above 25 mA. Below 25 mA, when $L_O$ is in discontinuous conduction, $i_L$ reaches zero before $i_L R_S$ reaches CPOSC's lower threshold. $v_{O2}$'s load therefore continues to discharge $C_{O2}$ until $v_{O2}$'s amplified error $v_{ERR2}$ overcomes the difference. As a result, $v_{O2}$ drops, and as the loads continue to lighten, $i_L$'s ripple diminishes and $v_{O2}$ falls further.

When load currents match, however, both outputs share $L_O$'s current evenly, so $v_{O1}$'s and $v_{O2}$'s switching frequencies $f_{O1}$ and $f_{O2}$ match $G_{OSC}$'s oscillating frequency $f_{OSC}$ in Fig. 5. When one load current is much lower than the other, however, the lighter load requires two or more cycles to droop its corresponding output to a level that warrants correction. As a result, the lightly loaded output skips cycles, like Figs. 10 and 11 show before 10 µs and Figs. 12 and 13 show after 40 µs. Although the variation in frequency is normally undesirable, this behavior is systemic, and therefore predictable and stable.

When $v_{O2}$'s load is 25 mA, for example, and $v_{O1}$'s load exceeds 7 mA, $i_{O1}$ is high and close enough to $i_{O2}$ for $v_{O1}$ to demand current every oscillating cycle. This is why $v_{O1}$'s $f_{O1}$ and $v_{O2}$'s $f_{O2}$ in Fig. 14 (black traces) match $i_L$'s $f_{OSC}$ above 7 mA when $i_{O2}$ is 25 mA. $L_O$ starts skipping $v_{O1}$ when $i_{O1}$ falls below 7 mA, when one cycle is enough to satisfy $v_{O1}$ for two cycles. This is why $f_{O1}$ falls under $f_{O2}$.

Similarly, when $i_{O2}$ is 5 mA and $i_{O1}$ is less than 60 mA, $i_{O2}$ is close enough to $i_{O1}$ for $v_{O2}$ to demand current every cycle. $f_{O1}$ and $f_{O2}$ in Fig. 14 (gray traces) therefore match $i_L$'s $f_{OSC}$ below 62 mA when $i_{O2}$ is 5 mA. $L_O$ starts skipping $v_{O2}$ above 62 mA because $v_{O1}$'s demand is so much greater than $v_{O2}$'s that $v_{O1}$'s load sinks $L_O$'s $i_L$ continuously across multiple cycles. In this case, $v_{O2}$ receives $i_L$ every other cycle.

Load Dumps: When $v_{O1}$'s load $i_{LD1}$ suddenly rises to a vastly higher level, $L_O$'s initial current cannot satisfy the higher load. CP$_{O1}$ and the flip-flops in Fig. 2 therefore skip $v_{O2}$ until $i_L$ satisfies $i_{LD1}$. As a result, load dump $\Delta i_{LD1}$ drops $v_{O1}$, like Fig. 10 shows, and $v_{O2}$ indirectly. And because $v_{O2}$ does not receive energy until $L_O$ satisfies $v_{O1}$, $v_{O2}$ recovers after $v_{O1}$ does. But since $G_{OSC}$'s hysteretic loop responds within $A_E$ and CP$_{OSC}$'s combined propagation delay, $i_L$ rises quickly to
recover $v_{O1}$ within one oscillating cycle and recover $v_{O2}$ 3.8 $\mu$s after $v_{O1}$'s load dump when oscillating frequency is 760 kHz.

When a heavy load suddenly disappears from $v_{O1}$, $C_{P1}$ disconnects $L_0$ from $v_{O1}$ quickly enough to keep $v_{O1}$ in regulation. $L_0$'s excess current, however, charges $C_{O2}$ above $v_{O2}$'s target $v_{R2}$, like Fig. 11 demonstrates. Like before, though, $A_E$ and $C_{OSC}$ respond quickly to recover $v_{O2}$ 2.2 $\mu$s after $v_{O1}$'s falling load dump. In other words, $v_{O2}$'s rising and falling load dumps, for the most part, only affect $v_{O2}$, but the hysteretic loop is fast enough to recover $v_{O2}$ within 3.8 $\mu$s.

Since the system always satisfies $v_{O1}$ first, fast and wide load dumps at $v_{O2}$ induce little to no effects on $v_{O1}$. $v_{O2}$'s rising and falling load dumps in Figs. 12 and 13, for example, lower and raise $v_{O2}$ out of regulation, but not $v_{O1}$. And like before, the hysteretic loop recovers $v_{O2}$ within 2–3 $\mu$s.

Since $A_E$ and $C_{OSC}$'s combined delay is well within one oscillating cycle, $v_{O1}$'s and $v_{O2}$'s response to simultaneous load dumps in Figs. 7 and 8 is similar to the independent load dumps in Figs. 10–13. So $v_{O1}$ again recovers within one oscillating cycle and $v_{O2}$ within 1–3 $\mu$s.

III. IMPLEMENTATION

Feedback resistors $R_{1T}$, $R_{1B}$, $R_{2T}$, and $R_{2B}$ in Fig. 15 translate reference voltages $v_{R1}$' and $v_{R2}$' to $v_{O1}$'s and $v_{O2}$'s actual targets $v_{R1}$ and $v_{R2}$ in Fig. 2. Comparator $C_{PZCS}$ opens $M_S$ when $i_L$ into $M_S$'s resistance reaches zero to keep $i_L$ from reversing and push $L_0$ into discontinuous conduction. $v_{O1}$'s $C_{P1}$ incorporates hysteresis $V_{TH}$ to keep noise in $v_{O1}$ from inadvertently tripping $C_{P1}$. $V_{TH}$, however, also keeps $v_{O1}$'s ripple $\Delta V_{O1}$ from falling below $V_{IH}$'s lower threshold. This is acceptable because, with $V_{IH}$ at 10 mV, load-dump effects in $v_{O1}$ overwhelm $V_{IH}$ to determine $v_{O1}$'s accuracy.

A. Current Sensor

The oscillator $G_{OSC}$ in Fig. 2 requires a current sensor. For testing purposes, the current sensor is the off-chip filter network in Fig. 15. Here, $R_{S3}$ and $C_{S3}$ and $R_{S0}$ and $C_{S0}$ filter $L_0$ and $R_{ESR}$'s voltage $v_L$ into voltages $v_{S3}$ and $v_{S0}$ like $L_0$ and $R_{ESR}$ filter $v_L$ into current $i_L$. So when $R_{S3}$ and $L_0R_{ESR}$ time constants match, $v_{S3}$ = $v_{S0}$ is a linear translation of $i_L$ [31].

$C_{P1}$-$R_{TH}$ and $C_{P0}$-$R_{TH}$ high-pass filter $v_{TH}$ and $v_{SO}$ to keep their dc components from propagating through. $v_{CM}$ is a bias dc voltage that establishes $v_{TH}$ and $v_{SO}$'s common-mode level. So with an adjustable $v_{CM}$, $v_{TH}$ and $v_{SO}$ can be within the input common-mode range of the comparator they feed.

B. Summing Comparator

Reducing $A_E$'s gain to one in Fig. 2 amounts to adding $v_{O2}$'s error $v_{O2}$ = $v_{R2}$ to $C_{OSC}$'s inverting input $v_i$: $(v_{O2} - v_{R2}) - v_i$.

Summing comparator $C_P$ in Fig. 15 does this with $(v_{O2} - v_{R2}) + (v_{FO} - v_{FI})$, where $v_{FO} - v_{FI}$ is $v_i$ in Fig. 2. But for the system to regulate $v_{O2}$ about $v_{R2}$ accurately, $v_{FO} - v_{FI}$'s dc component should be negligibly low. This is another reason why the current sensor high-pass filters $v_{S3}$'s and $v_{S0}$'s translation of $i_L$ to ensure $v_{FO} - v_{FI}$ is nearly zero at dc. This way, $C_P$ and the loop can keep $v_{O2}$ near $v_{R2}$.

When $L_0$ is in discontinuous conduction, $i_L$ reaches zero before $i_L$'s translation $v_i$ in Fig. 2 reaches $C_{P1}$'s lower threshold. $v_{R2}$'s load therefore discharges $C_{O2}$ until $v_{R2}$'s droop finally trips $C_{P2}$ to start another cycle. When $v_{R2}$'s load is very light, discontinuous-conduction time $t_{DCM}$ between cycles (from Fig. 4) is long. So if $v_{O1}$'s load suddenly rises, response time $t_r$ is that much longer.

Feeding $v_{O1}$'s error $v_{O1} - v_{TH}$ into $C_P$ in Fig. 15 allows $v_{O1}$'s error to trip $C_P$ sooner for a faster response. In steady state, $v_{O1}$'s loop keeps $v_{O1}$ near $v_{R1}$, so $v_{O1} - v_{R1}$ is low at dc. Since $v_{FO} - v_{FI}$ is also low at dc, $C_P$ keeps $v_{O2}$ near $v_{R2}$.

C. Power Management

![Fig. 15: Prototyped 0.6-µm CMOS switched-inductor dual-supply hysteretic current-mode buck converter.](image-url)

Resistances, switching gates, and the controller consume ohmic, gate-drive, and quiescent power $P_R$, $P_G$, and $P_0$. So to minimize $P_R$ and $P_G$, transistor channel lengths are minimum at 0.6 µm and widths are wide enough to balance their ohmic and gate-drive losses, and therefore, consume the least power [32]. This way, $L_0$'s series resistance 400 mΩ and other ohmic losses in $P_R$ climb in Fig. 16 with load power from nearly zero to 22 mW, when the combined load is 200 mW. Logic and other gate-drive losses in $P_G$ rise with $f_{OSC}$ (from Fig. 5) in discontinuous conduction and flatten past 96 mW, when $f_{OSC}$ settles in continuous conduction. $C_P$, $C_{P1}$, and $C_{ZCS}$ dissipate about 2 mW as $P_R$ across load levels.

Like Fig. 17 shows, power-conversion efficiency $\eta_c$ peaks at 88% when $i_{O1}$ is 25 mA and $i_{O2}$ is 43 mA, when the combined load is 145 mW. $\eta_c$ remains above 85% when $i_{O2}$ pulls at least 25 mA or 62 mW and above 80% when $i_{O2}$ pulls more than 5 mA or 13 mW. $\eta_c$ is generally higher when $i_{O2}$ is greater than $i_{O1}$ because $M_{O2}$'s current–overlap loss is lower. This is because $M_{O2}$'s initial voltage when it shorts is about 0.65 V (across its body diode) and $M_{O1}$'s is about 1.65 V.
(between \(v_{O1}\) and \(v_{O2}\) and \(M_{O2}'\)s body-diode voltage).

![Fig. 17. Measured power-conversion efficiency across load levels.](image)

**IV. Prototype**

Everything but the current-sensor network, inductor, output capacitors, and feedback resistors in Fig. 15 are in the 1.4×2.0-mm\(^2\) 0.6-μm CMOS die in Fig. 18. A finer-pitched CMOS process is possible, but also more costly, with lower breakdown voltages, and for proof of concept, unnecessary. The current sensor and feedback resistors are off chip for breakdown voltages, a process is possible.

2.0 μF capacitors, and feedback resistors in Fig. 18.

This Work

![Fig. 18. Prototyped 0.6-μm CMOS die and two-layer board.](image)

| TABLE I: COMPARISON OF THE STATE OF THE ART |
|-----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
|                | [33]           | [16]           | [34]           | [35]           | [36]           | [37]           | [38]           | [39]           |
| Tech.          | 0.5 μm         | 0.35 μm        | 0.25 μm        | 40 nm          | 55 nm          | 65 nm          | 0.35 μm        | 0.5 μm         | 0.6 μm         |
| Area           | 2.4 mm\(^2\)   | 3.84 mm\(^2\)  | 5.29 mm\(^2\)  | 4.00 mm\(^2\)  | 0.98 mm\(^2\)  | 1.86 mm\(^2\)  | 5.04 mm\(^2\)  | 4.40 mm\(^2\)  | 2.80 mm\(^2\)  |
| \(v_{IN}\)     | 1.3–2.85 V     | 2.7–3.3 V      | 2.7–5 V        | 2.7–3.6 V      | 3.4–4.3 V      | 2.0–3.0 V      | 1.2–2.2 V      | 2.6–4.2 V      |
| \(v_{O}\)      | 3.3, 6 V       | 1.2, 1.8 V     | 1.2, 1.8 V     | 1.1–2.25 V     | 1.8, 1.2 V     | 1.2–2.8 V      | 2.5–5 V        | 3.0, 2.5 V     | 1.5, 2.5 V     |
| \(k_{O(MAX)}\) | 170 mA         | 200 mA         | 600 mA         | 100 mA         | 900 mA         | 600 mA         | 1150 mA        | 100 mA         | 120 mA         |
| \(L\)          | 1 μH           | 125 μΩ         | 1 μH           | 4.7 μH         | 4.7 μH         | 4.7 μH         | 4.7 μH         | 10 μH          | 40 μΩ          |
| \(C\)          | 33–40 μF       | 85–80 μΩ       | 22 μF          | 47 μF          | 47 μF          | 47 μF          | 47 μF          | 47 μF          | 22 μF          |
| Extra Dev.     | 3 μF           |                |                |                |                |                |                |                |                |
| \(f_{SW}\)     | 1 MHz          | 1 MHz          | 1.3 MHz        | 1 MHz          | 1 MHz          | 1 MHz          | 0.8 MHz        | 0.5 MHz        | 200–850 kHz    |
| \(Δ\)         | ±50 mA         | ±90 mA         | ±547 mA        | ±200 mA        | ±180 mA        | ±150 mA        | ±40 mA         | ±50 mA         | ±65 mA         |
| \(t_{B}\)      | 20 μs          | 2 μs           | 15 μs          | 40 μs          | 8 μs           | 12 μs          | 200 μs         | 3 μs           | 3.8 μs         |
| \(Δ\)         | 40 mV          | 33 mV          | 60 mV          | 60 mV          | 100 mV         | 50 mV          | 200 mV         | 30 mV          | ±177 mV        |
| \(η\)         | 88%            | 83%            | 87%            | 89%            | 91%            | 83%            | 92%            | 81%            | 88%            |
| \(Δ\)         | 72%            | 72%            | 80%            | 86%            | 83%            | 83%            | 74%            | 80%            | 85%            |
| \(R_FOM\)     | 22%            | 108%           | 13%            | 3.4%           | 63%            | 46%            | 1.9%           | 29%            | 100%           |

\(^{1}\)Uses linear regulator; \(^{2}\)estimated values; and \(^{3}\)when \(v_{O1} = 1\) V and \(v_{O2} = 1.8\) V.
practice, the application dictates how much $\Delta i_{O(LD)}$ the load requires and how much $\Delta V_{O(MAX)}$ the load can sustain, and with these, $t_{\text{tr}}$ sets $C_{O}$, or in some cases, $C_{G}$ sets $t_{\text{g}}$. In other words, $\Delta i_{O(LD)}$ and $\Delta V_{O(MAX)}$ are independent application parameters and $t_{\text{g}}$ and $C_{O}$ are codependent design variables that are normally independent of $\Delta i_{O(LD)}$ and $\Delta V_{O(MAX)}$. So $t_{\text{tr}}$ alone is a good way of assessing and comparing designs.

The system here responds quickly at 0.9–3.8 $\mu$s because the oscillator’s response time is practically the time $L_{0}$’s $i_{L}$ requires to slew to its target. This is as fast as a switched inductor possibly can. [16] in Table 1 is slightly faster at 2 $\mu$s because a linear regulator is the one that responds to load dumps. This linear regulator, however, requires additional silicon area and power, so die size is 37% larger with 42% shorter channel lengths and peak and full-load efficiencies are 5% and 13% lower.

[39] is a close second at 5 $\mu$s, but die area is 57% larger and efficiencies are 7% and 5% lower. [36] is third at 8 $\mu$s, but with 91% shorter channel lengths $L_{\text{MIN}}$. [37] is next at 12 $\mu$s, but with 89% shorter $L_{\text{MIN}}$ and 5% and 2% lower efficiencies. [34] follows at 15 $\mu$s because a capacitor between outputs couples errors, like CP$E_{L}$ here does, to accelerate response time. This capacitor, however, is off chip, die size is 89% larger with 58% shorter $L_{\text{MIN}}$ and efficiencies are 1% and 5% lower.

**Relative Figure of Merit:** Maximum current $i_{O(MAX)}$, peak and full-load efficiencies $\eta_{(PK)}$ and $\eta_{(FL)}$, maximum response time $t_{\text{r(MAX)}}$, and cost of silicon area $A_{SI}$, additional off-chip components $\Delta N_{OC}$, and process technology define the merits of a power supply. Although not always weighed evenly, a relative figure of merit (RFoM) should climb with $i_{O(MAX)}$, $\eta_{(PK)}$, $\eta_{(FL)}$, and minimum channel length $L_{\text{MIN}}$ (for lower cost) and fall with $t_{\text{r(MAX)}}$, $A_{SI}$, and $\Delta N_{OC}$.

$$\text{RFoM} = \frac{i_{O(MAX)} \eta_{(PK)} \eta_{(FL)} L^{-1}_{\text{MIN}}}{t_{\text{r(MAX)}} A_{SI} (1 + \Delta N_{OC}) \text{PoR}},$$

where PoR is a normalizing point of reference. So when normalizing to this system, whose $i_{O(MAX)}$ is 120 mA, $\eta_{(PK)}$ is 88%, $\eta_{(FL)}$ is 85%, $L_{\text{MIN}}$ is 0.6 $\mu$m, $t_{\text{r(MAX)}}$ is 3.8 $\mu$s, $A_{SI}$ is 2.8 $\text{mm}^2$, and $\Delta N_{OC}$ is 0, PoR is 5.0616E3 and RFoM is 1.

Using this metric, [16]'s rating is slightly higher by 8% because 67% higher $i_{O(MAX)}$ and 47% lower $t_{\text{r(MAX)}}$ edge other deficiencies. (Note that [16]'s $t_{\text{r(MAX)}}$ is an unmeasured estimate.) [36]'s and [37]'s ratings are 37% and 54% lower than the system presented here primarily because $L_{\text{MIN}}$’s are 91% and 89% lower. [39]'s, [33]'s, and [34]'s ratings are 71%, 78%, and 87% lower because the balance between response times and efficiencies is less favorable. [35]'s rating is 96% lower because $L_{\text{MIN}}$ is 83% shorter and $t_{\text{r(MAX)}}$ is 10.5 $\times$ higher and [38]'s ratings is 98% lower mostly because $i_{O(MAX)}$ is 53 $\times$ higher. In other words, this work and [16] rate similarly high, except this work is more efficient and [16] is slightly faster.

**V. CONCLUSIONS**

The 0.6-$\mu$m CMOS switched-inductor dual-supply system presented here responds to rising and falling 45–65-mA load dumps within 3.8 $\mu$s to keep its outputs within $\pm 78$ mV and $+160$ and $-177$ mV of their 1.5- and 2.5-V targets with 88% and 85% peak and full-load efficiencies. Response time is essentially the time the inductor current requires to slew to its target, which is as fast as any switched inductor possibly can. The system is so quick and stable because the hysteretic oscillator that ripples the inductor current about the loop-defined average responds within the propagation delay of a comparator: within one cycle. Response time is critical because faster supplies require less capacitance to supply load dumps and maintain accuracy. In literature, only [16] is slightly faster at 2 $\mu$s because a linear regulator bypasses the inductor to supply load dumps. [16]'s tradeoffs are 37% larger die, 42% shorter channel lengths, and 5% and 13% lower peak and full-load efficiencies. Sacrificing conversion efficiency, die area, and process technology for the sake of speed, however, shortens battery life and raises cost, which limits market penetration, profits, and overall impact.

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**REFERENCES**


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