# 0.6-μm CMOS Switched-Inductor Dual-Supply Hysteretic Current-Mode Buck Converter

Carlos J. Solis, *Graduate Student Member, IEEE*, Gabriel A. Rincón-Mora, *Fellow, IEEE*

***Abstract*—Microsystems can sense, process, information between nodes across hospitals, factories, and homes that can save lives, energy, and money. Unfortunately, supplying power with so much embedded functionality is challenging, because while some functions can survive higher noise levels and voltages, others cannot. Power supplies must therefore satisfy several independent outputs without consuming much power or occupying much space. A switched inductor is attractive in this respect because, with only one off-chip inductor, the system can output 80%–90% of the power it draws. Regulating multiple outputs with one inductor, however, links several feedback loops and their reactions to individual and combined loads. The sacrifice for this is usually accuracy in the form of response time. The single-inductor dual-output buck converter presented here uses a hysteretic current loop for this reason: to accelerate the response of the loops used to regulate the outputs. The 0.6-μm CMOS prototype supplies 70 and 50 mA to 1.5- and 2.5-V outputs with 80%–88% power-conversion efficiency and responds to 45–65-mA load dumps within 3.8 μs to keep 1.5 V within ±5% and 2.5 V within ±7%.**

***Index Terms*—DC–DC buck converter, cross regulation, hysteretic current-mode control, single-inductor multiple-output (SIMO), dual output, and switched-inductor power supply.**

## I. Powering Multifunctional Microsystems

Networked microsystems that sense, process, store, transmit, and receive information in hospitals, factories, farms, and homes can save lives, energy, and money [1]–[2]. But functions require power, and although digital-signal processors (DSPs) can tolerate some degree of noise in their supplies, sensors and analog–digital converters (ADCs) cannot [3]. Plus tiny batteries cannot sustain power for long, so even though DSPs, ADCs, and power amplifiers (PAs) can tolerate higher voltages, they (for the sake of saving energy) should not [4]. Efficient power-supply systems like Fig. 1 illustrates must therefore supply and regulate several outputs [5]–[6].

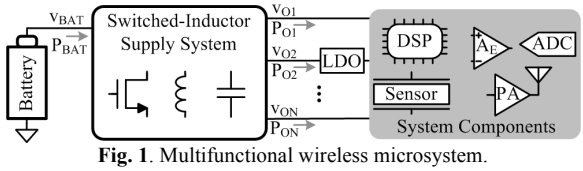


**Fig. 1**. Multifunctional wireless microsystem.

To save energy, microsystems often idle or disable non-critical blocks [7]. This means, responding to sensed events and load dumps requires short wake-up times. In other words, power supplies must react quickly [8]. Unfortunately, linear regulators, which are fast, are typically inefficient [9], and switched inductors, which are efficient, are normally slow and bulky [10]–[11]. This is why the state of the art relies on one inductor for efficient power conversion and on one or several series low-dropout (LDO) regulators for fast response [12].

Switched inductors are slower than linear regulators because inductor voltages and inductances limit how fast inductor currents change. Plus, several switching cycles elapse before typical digital [13] and pulse-width modulated (PWM) [14]–[15] controllers can respond. Waiting for one switched inductor to respond to one of several loads also requires additional time [16]−[18]. So after one output's load imbalances the inductor, other outputs suffer the irregularity in the form of cross regulation [19]−[21].

The single-inductor dual-output buck converter presented here reduces cycling time by supplying all outputs within one energize/drain sequence of the inductor [22]−[26] and shortens response time by using a hysteretic oscillator to establish the inductor's current [27]. To demonstrate this, Sections II and III explain and show how the system supplies and regulates two outputs with one inductor. Sections IV and V then assess and compare performance with the state of the art.

## II. Switched-Inductor Dual-Supply System

The circuit in Fig. 2 essentially transforms inductor $L_O$ into an adjustable current source $i_L$ that supplies and responds to the demands of two outputs. $G_{OSC}$ is this current source, a transconductor whose current an amplifier $A_E$ adjusts. So when first energizing $L_O$, $G_{OSC}$'s $v_{OSC}$ connects $L_O$ to $v_{O1}$ until comparator $CP_{O1}$ senses that $L_O$ satisfies $v_{O1}$. $L_O$ then connects to $v_{O2}$, and if $L_O$'s leftover energy is insufficient or excessive, $A_E$ amplifies $v_{O2}$'s error to adjust and tune $G_{OSC}$'s $i_L$.

Functionally, $G_{OSC}$ is an oscillating current source that implements the function of the current loop in this current-mode system. $CP_{O1}$ closes the independent voltage loop that ensures $v_{O1}$ peaks nears target $v_{R1}$. $A_E$ closes the master loop that adjusts $G_{OSC}$'s current $i_L$ to ensure $v_{O2}$ nears target $v_{R2}$.

Drivers insert dead times between the conduction periods of adjacent switches $M_N$ and $M_P$ and $M_{O1}$ and $M_{O2}$ to keep them from shorting the input voltage $v_{IN}$, ground, and $v_{O1}$ and $v_{O2}$. $M_N$'s and $M_{O2}$'s body terminals connect to their drains to ensure their body diodes conduct $L_O$'s $i_L$ during $M_P$–$M_N$'s and $M_{O1}$–$M_{O2}$'s dead-time periods. $M_N$'s driver also opens $M_N$ when $L_O$'s current reaches zero to keep $L_O$ from conducting negative current. This way, in discontinuous-conduction mode (DCM), $M_N$ does not consume unnecessary ohmic power. $M_{O1}$ is an NFET because $v_{IN}$'s 2.6–4.2 V is high enough above $v_{O1}$'s

Manuscript received .

The authors are with the School of Electrical and Computer Engineering at the Georgia Institute of Technology in Atlanta, Georgia 30332-0250 U.S.A. (E-mail: csolis3@gatech.edu and Rincon-Mora@gatech.edu).

1.5 V to drive $M_{O1}$'s gate. $M_{O2}$ is a PFET because ground is similarly low enough below $v_{O2}$'s 2.5 V to drive $M_{O2}$'s gate.

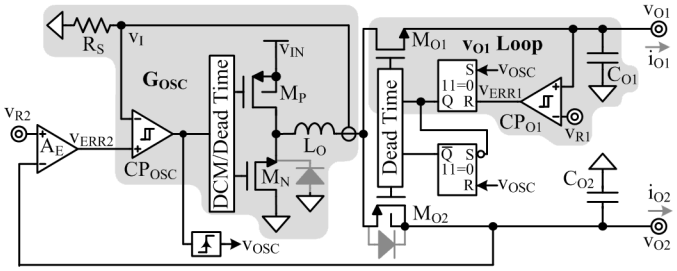


**Fig. 2.** Switched-inductor dual-supply hysteretic current-mode system.

### *A. Oscillating Current Source*

Continuous Conduction: Comparator $CP_{OSC}$, $M_P$, $M_N$, $L_O$, and $R_S$ implement a relaxation oscillator that ramps $L_O$'s current $i_L$ between the hysteretic limits that $CP_{OSC}$ and $R_S$ establish and about the average that $A_E$'s $v_{ERR2}$ and $R_S$ set. For this, $CP_{OSC}$ closes $M_P$ and $M_{O1}$ to energize $L_O$ from $v_{IN}$ to $v_{O1}$ with energize voltage $v_{E1}$ or $v_{IN} - v_{O1}$ until $i_L$ into $R_S$ reaches $CP_{OSC}$'s upper threshold. This is why $i_L$ in Fig. 3 climbs across energize period $t_E$. After that, $CP_{OSC}$ opens $M_P$ and closes $M_N$ to drain $L_O$ from ground into $v_{O1}$ with drain voltage $v_{D1}$ or $0 - v_{O1}$, and after $i_L$ satisfies $v_{O1}$'s load, into $v_{O2}$ with $v_{D2}$ or $0 - v_{O2}$. $i_L$ therefore falls across drain period $t_D$, first at $v_{D1}/L_O$ and then at $v_{D2}/L_O$.

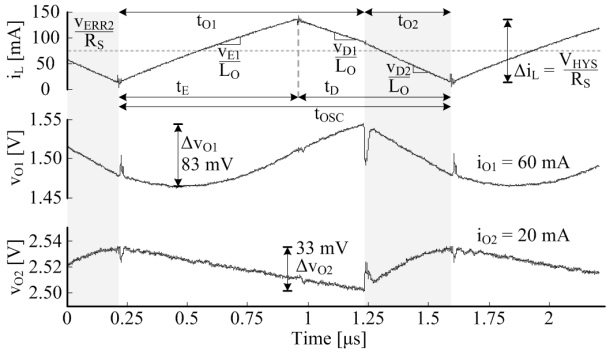


**Fig. 3.** Measured waveforms in continuous-conduction mode.

$R_S$ senses $i_L$ and translates $CP_{OSC}$'s hysteresis $V_{HYS}$ and $A_E$'s error $v_{ERR2}$ into currents. $i_L$ therefore oscillates across $V_{HYS}/R_S$, and if $CP_{OSC}$'s thresholds are symmetrical, about $v_{ERR2}/R_S$. This means, $i_L$'s ripple $\Delta i_L$ is $V_{HYS}/R_S$, $i_L$'s average $i_{L(AVG)}$ is $v_{ERR2}/R_S$, and the oscillator's closed-loop gain $G_{OSC}$ is

$$G_{OSC} \equiv \frac{i_{L(AVG)}}{v_{ERR2}} = \frac{1}{R_S}. \qquad (1)$$

Since $L_O$'s voltage determines how fast $i_L$ crosses $\Delta i_L$, energize voltage $v_E$ sets $t_E$, drain voltage $v_D$ sets $t_D$, and together, they set oscillating period $t_{OSC}$ to

$$t_{OSC} = t_E + t_D = \Delta i_L \left(\frac{L_O}{v_E} + \frac{L_O}{v_D}\right) = \left(\frac{V_{HYS}}{R_S}\right)\left(\frac{L_O}{v_E} + \frac{L_O}{v_D}\right). \qquad (2)$$

Relative load levels dictate the fraction of time $L_O$ connects to each output. In Fig. 3, for example, $i_{O1}$'s 60 mA is 75% of the combined 80-mA load, so $v_{O1}$'s connection time $t_{O1}$ is roughly 75% of $t_{OSC}$, well past $L_O$'s energizing period $t_E$. As a result, energize voltage $v_E$ is $v_{E1}$ or $v_{IN} - v_{O1}$ and drain voltage $v_D$ is first $v_{D1}$ or $-v_{O1}$ and then $v_{D2}$ or $-v_{O2}$. When $i_{O2}$ is approximately higher than 50% of the combined load, $v_{O2}$'s connection time $t_{O2}$ extends into $t_E$, so $v_E$ is first $v_{E1}$ or $v_{IN} - v_{O1}$ and then $v_{E2}$ or $v_{IN} - v_{O2}$, and $v_D$ is $v_{D2}$ or $-v_{O2}$. This shift in relative connectivity translates to a variation in the oscillating period $t_{OSC}$ and resulting frequency $f_{OSC}$ or $1/t_{OSC}$.

Discontinuous Conduction: When the combined load is light, the loop lowers $v_{ERR2}$ to the point $i_L$ reaches zero before $i_L R_S$ reaches $CP_{OSC}$'s lower threshold. Once at zero, $M_N$'s driver opens $M_N$ to keep $i_L$ from reversing, so $v_{O2}$'s load discharges $C_{O2}$ past 1.5 µs in Fig. 4 until $v_{ERR2}$ finally trips $CP_{OSC}$. In other words, $i_L$'s lower ripple produces an offset $(V_{HYS} - \Delta i_L R_S)/A_E$ that $v_{O2}$'s fall must overcome to trip $CP_{OSC}$. This means, $i_{O2}$ reduces $v_{O2}$'s lower peak when $L_O$ is in discontinuous conduction – from 2.5 V in Fig. 3 to 2.44 V in Fig. 4 – and $i_{O2}$ extends $t_{OSC}$ to $t_{OSC}'$:

$$t_{OSC}' = t_{OSC} + t_{DCM} = t_{OSC} + \left(\frac{V_{HYS} - \Delta i_L R_S}{A_E}\right)\left(\frac{C_{O2}}{i_{O2}}\right). \qquad (3)$$

$t_{OSC}'$ therefore shortens and $f_{OSC}$ in Fig. 5 climbs with $i_{O2}$ until discontinuous time $t_{DCM}$ in Fig. 4 vanishes, after which $t_{OSC}'$ levels to $t_{OSC}$ and $f_{OSC}$ to $1/t_{OSC}$.

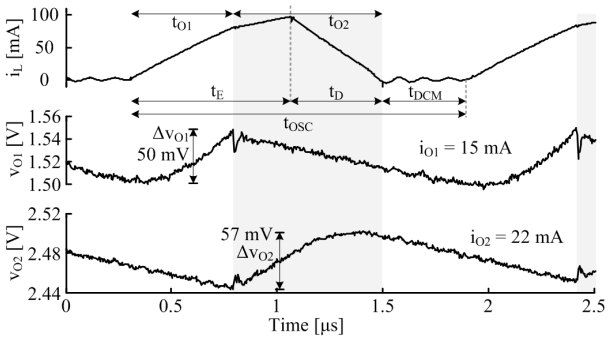


**Fig. 4.** Measured waveforms in discontinuous-conduction mode.

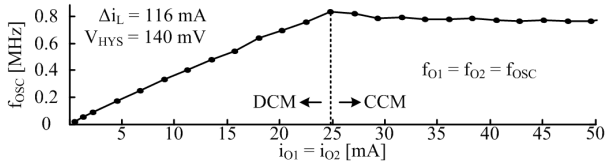


**Fig. 5**. Measured oscillating frequency across modes under balanced loads.

Bandwidth: The comparator $CP_{OSC}$, drivers, switches $M_P$ and $M_N$, and slew-rate of $L_O$'s $i_L$ determine the oscillator's response time $t_R$. Of these, $CP_{OSC}$, the drivers, and $M_P$ and $M_N$ respond in ns and $i_L$ in µs, so $t_R$ mostly depends on $L_O$. When rising, energizing voltage $v_E$ slews $L_O$, and when falling, drain voltage $v_D$ slews $L_O$, so to account for both, $t_R$ is roughly the average of rise and fall times $t_{RI}$ and $t_{FA}$ [30]:

$$t_R \approx \frac{t_{RI} + t_{FA}}{2} = \left(\frac{\Delta i_L}{2}\right)\left(\frac{L_O}{v_E} + \frac{L_O}{v_D}\right) = \left(\frac{\Delta v_{ERR2}}{2R_S}\right)\left(\frac{L_O}{v_E} + \frac{L_O}{v_D}\right)\Bigg|_{\Delta v_{ERR2} < 2V_{HYS}} < t_{OSC}. \qquad (4)$$

So when the oscillator's input steps across a variation $\Delta v_{ERR2}$ that is less than $2V_{HYS}$, $t_R$ is less than $t_{OSC}$, which means $i_L$ reaches its target within one cycle. In other words, the oscillator's bandwidth $f_{BW}$ is as high as the oscillating frequency $f_{OSC}$, which is as high as any current loop in a dc–dc converter can claim. What is more, since switching converters cannot outpace their inductors, this oscillating current source is as fast as any current loop can ever be.

### *B. Independent Peak-Voltage Loop*

$G_{OSC}$ in Fig. 2 feeds the independent feedback loop that regulates $v_{O1}$. Comparator $CP_{O1}$ senses $v_{O1}$ and $v_{R1}$ to generate an error $v_{ERR1}$ that determines when to disconnect $L_O$ from $v_{O1}$. This way, $CP_{OSC}$'s edge-triggered output $v_{OSC}$ first sets $M_{O1}$'s flip-flop to connect $L_O$ to $v_{O1}$. $L_O$'s $i_L$ raises $v_{O1}$ past this point, past 0.2 µs in Fig. 3, because $i_L$ carries more energy than either output alone requires. When $v_{O1}$ reaches $v_{R1}$, $CP_{O1}$ resets $M_{O1}$'s flip-flop to disconnect $L_O$ from $v_{O1}$. $v_{O1}$'s load then discharges $C_{O1}$ until $v_{OSC}$ again connects $L_O$ to $v_{O1}$.

Stability: $G_{OSC}$'s $i_L$ is essentially an oscillating current source that feeds the loop that regulates $v_{O1}$. $CP_{O1}$, $M_{O1}$'s flip-flop, $M_{O1}$'s driver, and $M_{O1}$ into $C_{O1}$ shunt and delay feedback signals across this loop to establish poles. The delays across $CP_{O1}$, the flip-flop, and the driver, however, are a small fraction of the oscillating cycle, so their effects appear well above $f_{OSC}$. $C_{O1}$, on the other hand, is so high at 470 nF that $C_{O1}$ delays and shunts $v_{O1}$ signals past a pole $p_{O1}$ that is well below $f_{OSC}$. So $v_{O1}$'s loop gain drops at 20 dB/decade past $p_{O1}$, and because no other delays disturb the fall, reaches unity with nearly 90° of phase margin, which means the loop is stable.

Load Regulation: Since $v_{OSC}$ connects $L_O$ to $v_{O1}$ and $CP_{O1}$ disconnects $L_O$ from $v_{O1}$ when $v_{O1}$ rises to $v_{R1}$, $CP_{O1}$ keeps $v_{O1}$'s peak near $v_{R1}$ and $v_{O1}$'s load droops $v_{O1}$ across what remains of $t_{OSC}$ after $v_{O1}$'s connection time $t_{O1}$ lapses. So as $i_{O1}$ and $i_{O2}$ together climb above 25 mA in Fig. 6, $v_{O1}$'s bottom and average levels droop to lower levels:

$$v_{O1(AVG)} = v_{R1} - \left(\frac{i_{O1}}{2}\right)\left(\frac{t_{OSC} - t_{O1}}{C_{O1}}\right). \qquad (5)$$

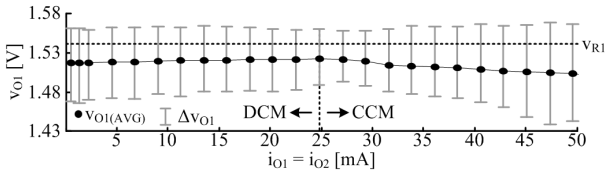


**Fig. 6**. First output's measured load regulation under balanced loads.

In discontinuous conduction, when $i_{O1}$ and $i_{O2}$ are both below 25 mA in Fig. 6, raising $v_{O2}$'s load reduces discontinuous time $t_{DCM}$ in Fig. 4, which shortens $t_{OSC}$ and the time $v_{O1}$'s load discharges $C_{O1}$. As a result, $t_{OSC}$'s reduction counters the effect of $i_{O1}$'s rise on $v_{O1}$ to produce less variation in $v_{O1}$'s low and average values. This means, load regulation is worse in continuous conduction.

Load-Dump Compensation: Response time $t_R$ in power supplies sets how long load dumps slew their outputs. So after a rising load dump $+\Delta i_{O1}$, the difference between the load and $i_{O1}$ (which is equivalent to $\Delta i_{O1}$) discharges $C_{O1}$ across $t_R$ to produce a falling variation $-\Delta v_{LD}$ in $v_{O1}$. After a falling load dump $-\Delta i_{O1}$, the difference between $i_{O1}$ and the load (which is equivalent to $\Delta i_{O1}$) charges $C_{O1}$ to produce a similar rising variation $+\Delta v_{LD}$. Unfortunately, these load dumps are often fast and wide, so $\pm\Delta v_{LD}$ can be ±7% to ±10%, high enough to overwhelm other effects and to, alone, limit a supply's accuracy [28]. This worsens when several outputs share one inductor because cycling between outputs extends $t_R$.

In this case, $v_{O1}$'s load regulation $-\Delta v_{LR}$ from Fig. 6 is significant by design. $\Delta v_{LR}$, however, does not affect $v_{O1(MIN)}$ because a fast rising load dump normally pulls $v_{O1}$ well below $v_{R1} - \Delta v_{LR}$ to $v_{R1} - \Delta v_{LD}$. But since a falling load dump raises $v_{O1}$ from its *loaded* level $v_{R1} - \Delta v_{LR}$, $-\Delta v_{LR}$ counters $+\Delta v_{LD}$ to reduce $v_{O1(MAX)}$ to $(v_{R1} - \Delta v_{LR}) + \Delta v_{LD}$. In other words, load regulation mitigates the effect of the falling load dump [28]–[29]. So adding a positive offset $v_{OS}$ to $v_{R1}$ that is similar, but opposite in magnitude to $-\Delta v_{LR}$ can reduce $v_{O1(MIN)}$ to $v_{OS} - \Delta v_{LD}$, and when $v_{OS}$ matches $\Delta v_{LR}$, reduce $v_{O1}$'s total variation $\Delta v_{O1(MAX)}$ to

$$\Delta v_{O1(MAX)} \equiv v_{O1(MAX)} - v_{O1(MIN)} = \pm\left|\Delta v_{LD} - \Delta v_{LR}\right|. \qquad (6)$$

This is why $v_{R1}$ in Fig. 2 is slightly above 1.5 V and $v_{O1}$ in Figs. 7 and 8 ripples about 1.5 V when loaded with 50 mA.

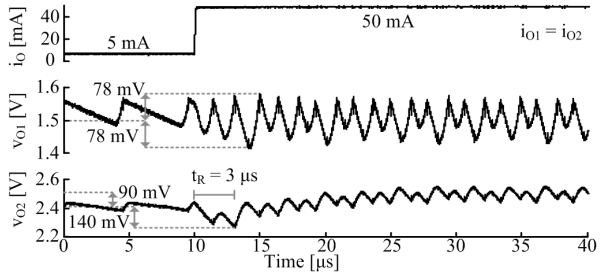


**Fig. 7**. Measured response to simultaneous rising 45-mA load dumps.

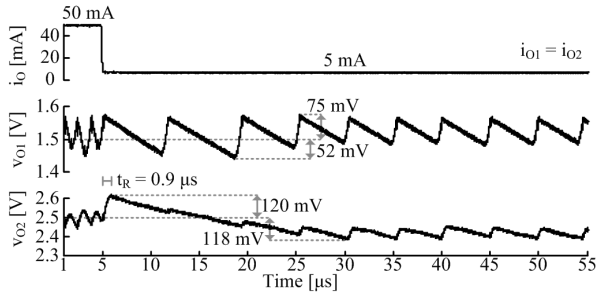


**Fig. 8**. Measured response to simultaneous falling 45-mA load dumps.

### *C. Master Voltage Loop*

Since $L_O$ carries more energy than either load requires, $i_L$ satisfies all small-signal variations in $v_{O1}$'s load. Insufficient or excess current in $L_O$ then produces small-signal alterations in $v_{O2}$ much like small changes in $v_{O2}$'s load would. $A_E$ in Fig. 2 senses these variations in $v_{O2}$ to generate an error $v_{ERR2}$ that adjusts $G_{OSC}$'s $i_L$ until $v_{O2}$ is again near its target $v_{R2}$.

Operationally, $v_{OSC}$ first sets $M_{O1}$'s flip-flop to connect $L_O$ to $v_{O1}$. When $v_{O1}$ rises to $v_{R1}$, $CP_{O1}$ resets $M_{O1}$'s flip-flop to disconnect $L_O$ from $v_{O1}$ and sets $M_{O2}$'s flip-flop to close $M_{O2}$ and connect $L_O$ to $v_{O2}$ after a dead time that the drivers insert. During this dead time, $M_{O2}$'s body diode steers $i_L$ into $v_{O2}$. $v_{OSC}$ then resets $M_{O2}$'s flip-flop and sets $M_{O1}$'s flip-flop to reconnect $L_O$ to $v_{O1}$ and start another cycle.

Stability: As mentioned earlier, $CP_{OSC}$, $M_P$, $M_N$, and $L_O$ realize an oscillator $G_{OSC}$ whose output is a current $i_L$ that ripples across $CP_{OSC}$'s $V_{HYS}/R_S$ and about $v_{ERR2}/R_S$. $CP_{OSC}$'s, $M_P$'s, and $M_N$'s delays are a small fraction of the oscillating period, so their effects are well above $f_{OSC}$. But $L_O$ is high at 12 µH, so $L_O$ and the voltages that $v_{IN}$, $v_{O1}$, and $v_{O2}$ impress across $L_O$ limit how fast $i_L$ responds to $v_{ERR2}$ variations. The resulting delay sets $G_{OSC}$'s bandwidth [30].

Because $L_O$ fully supplies $v_{O1}$ before feeding $v_{O2}$, the effect of $v_{O1}$'s loop on $i_L$ is to sink or subtract a portion of $i_L$. In other words, $i_{O1}$ is essentially another load to $L_O$. This means, the small-signal dynamics of $v_{O1}$'s loop appear as additional load variations to the loop that senses $v_{O2}$ to adjust $G_{OSC}$'s $i_L$.

$A_E$, $G_{OSC}$, and $C_{O2}$ close the loop that feeds $v_{O1}$'s load and

regulates $v_{O2}$. $C_{O2}$ is high at 560 nF to keep load dumps from deviating $v_{O2}$ too much. This means, $C_{O2}$ shunts $v_{O2}$'s load at a low-frequency pole $p_{O2}$. So to ensure the gain across the loop reaches unity at 20 dB/decade with nearly 90° of phase margin, $A_E$'s and $G_{OSC}$'s bandwidths are, by design, above the unity-gain frequency that $C_{O2}$, by design, establishes.

Load Regulation: Since $A_E$ amplifies $v_{O2}$'s error to continually adjust $G_{OSC}$'s $i_L$, $v_{O2}$'s average $v_{O2(AVG)}$ in Fig. 9 is near $v_{R2}$'s 2.5 V when $L_O$ is in continuous conduction, when both load currents are above 25 mA. Below 25 mA, when $L_O$ is in discontinuous conduction, $i_L$ reaches zero before $i_L R_S$ reaches $CP_{OSC}$'s lower threshold. $v_{O2}$'s load therefore continues to discharge $C_{O2}$ until $v_{O2}$'s amplified error $v_{ERR2}$ overcomes the difference. As a result, $v_{O2}$ drops, and as the loads continue to lighten, $i_L$'s ripple diminishes and $v_{O2}$ falls further.

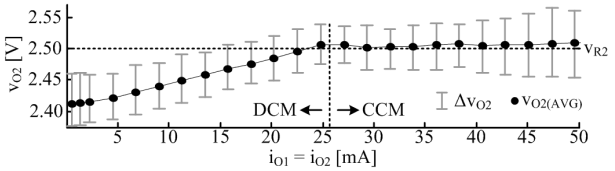


**Fig. 9**. Second output's measured load regulation under balanced loads.

## D. Cross Regulation

Load Disparity: For good regulation performance, the system should be able to skip outputs that do not require energy. This is why $v_{O1}$'s flip-flop in Fig. 2 does not set when both set and reset signals are high. This way, if $CP_{O1}$ senses $v_{O1}$ is already near or above $v_{R1}$, $v_{OSC}$ cannot set $M_{O1}$'s flip-flop to connect $L_O$ to $v_{O1}$. The flip-flop's low output therefore sets $v_{O2}$'s flip-flop to close $M_{O2}$ and connect $L_O$ to $v_{O2}$. Skipping $v_{O2}$ is more natural because, when $v_{O1}$'s load is much greater than $v_{O2}$'s load, $L_O$'s energy per cycle is not enough to satisfy $v_{O1}$'s load. As a result, $v_{O1}$ does not reach $v_{R1}$ until the following cycle. Extending $v_{O1}$'s connection time $t_{O1}$ to $t_{OSC}$ this way keeps $L_O$ from connecting to $v_{O2}$ across that cycle.

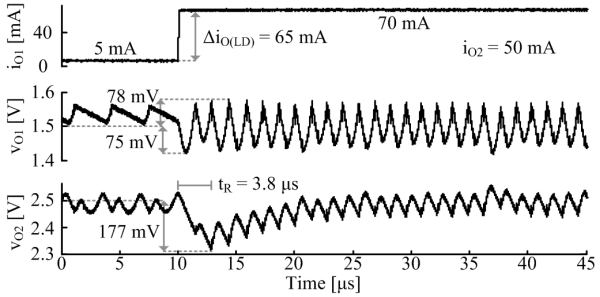


**Fig. 10**. Measured response to a rising 65-mA load dump at $v_{O1}$.

When load currents match, however, both outputs share $L_O$'s current evenly, so $v_{O1}$'s and $v_{O2}$'s switching frequencies $f_{O1}$ and $f_{O2}$ match $G_{OSC}$'s oscillating frequency $f_{OSC}$ in Fig. 5. When one load current is much lower than the other, however, the lighter load requires two or more cycles to droop its corresponding output to a level that warrants correction. As a result, the lightly loaded output skips cycles, like Figs. 10 and 11 show before 10 µs and Figs. 12 and 13 show after 40 µs. Although the variation in frequency is normally undesirable, this behavior is systemic, and therefore predictable and stable.

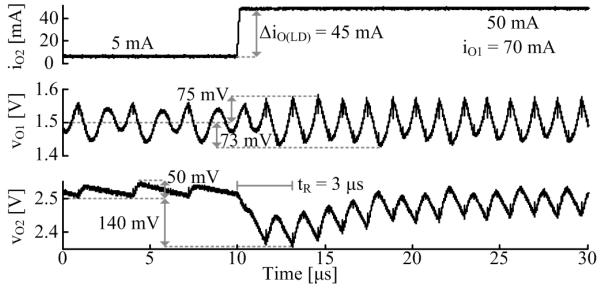


**Fig. 11**. Measured response to a rising 45-mA load dump at $v_{O2}$.

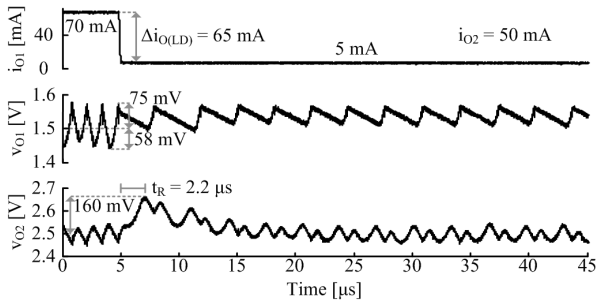


**Fig. 12**. Measured response to a falling 65-mA load dump at $v_{O1}$.

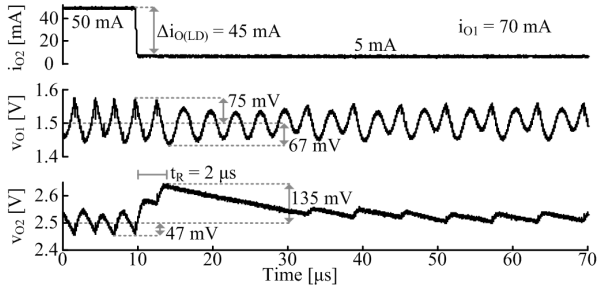


**Fig. 13**. Measured response to a falling 45-mA load dump at $v_{O2}$.

When $v_{O2}$'s load is 25 mA, for example, and $v_{O1}$'s load exceeds 7 mA, $i_{O1}$ is high and close enough to $i_{O2}$ for $v_{O1}$ to demand current every oscillating cycle. This is why $v_{O1}$'s $f_{O1}$ and $v_{O2}$'s $f_{O2}$ in Fig. 14 (black traces) match $i_L$'s $f_{OSC}$ above 7 mA when $i_{O2}$ is 25 mA. $L_O$ starts skipping $v_{O1}$ when $i_{O1}$ falls below 7 mA, when one cycle is enough to satisfy $v_{O1}$ for two cycles. This is why $f_{O1}$ falls under $f_{O2}$.

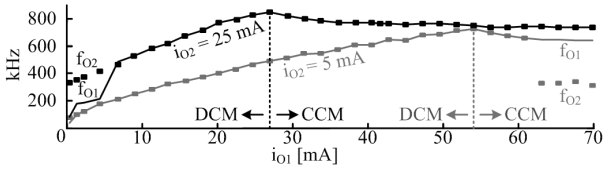


**Fig. 14**. Switching frequencies across load levels.

Similarly, when $i_{O2}$ is 5 mA and $i_{O1}$ is less than 60 mA, $i_{O2}$ is close enough to $i_{O1}$ for $v_{O2}$ to demand current every cycle. $f_{O1}$ and $f_{O2}$ in Fig. 14 (gray traces) therefore match $i_L$'s $f_{OSC}$ below 62 mA when $i_{O2}$ is 5 mA. $L_O$ starts skipping $v_{O2}$ above 62 mA because $v_{O1}$'s demand is so much greater than $v_{O2}$'s that $v_{O1}$'s load sinks $L_O$'s $i_L$ continuously across multiple cycles. In this case, $v_{O2}$ receives $i_L$ every other cycle.

Load Dumps: When $v_{O1}$'s load $i_{LD1}$ suddenly rises to a vastly higher level, $L_O$'s initial current cannot satisfy the higher load. $CP_{O1}$ and the flip-flops in Fig. 2 therefore skip $v_{O2}$ until $i_L$ satisfies $i_{LD1}$. As a result, load dump $\Delta i_{LD1}$ droops $v_{O1}$, like Fig. 10 shows, and $v_{O2}$ indirectly. And because $v_{O2}$ does not receive energy until $L_O$ satisfies $v_{O1}$, $v_{O2}$ recovers after $v_{O1}$ does. But since $G_{OSC}$'s hysteretic loop responds within $A_E$ and $CP_{OSC}$'s combined propagation delay, $i_L$ rises quickly to

recover $v_{O1}$ within one oscillating cycle and recover $v_{O2}$ 3.8 µs after $v_{O1}$'s load dump when oscillating frequency is 760 kHz.

When a heavy load suddenly disappears from $v_{O1}$, $CP_{O1}$ disconnects $L_O$ from $v_{O1}$ quickly enough to keep $v_{O1}$ in regulation. $L_O$'s excess current, however, charges $C_{O2}$ above $v_{O2}$'s target $v_{R2}$, like Fig. 11 demonstrates. Like before, though, $A_E$ and $CP_{OSC}$ respond quickly to recover $v_{O2}$ 2.2 µs after $v_{O1}$'s falling load dump. In other words, $v_{O1}$'s rising and falling load dumps, for the most part, only affect $v_{O2}$, but the hysteretic loop is fast enough to recover $v_{O2}$ within 3.8 µs.

Since the system always satisfies $v_{O1}$ first, fast and wide load dumps at $v_{O2}$ induce little to no effects on $v_{O1}$. $v_{O2}$'s rising and falling load dumps in Figs. 12 and 13, for example, lower and raise $v_{O2}$ out of regulation, but not $v_{O1}$. And like before, the hysteretic loop recovers $v_{O2}$ within 2–3 µs.

Since $A_E$ and $CP_{OSC}$'s combined delay is well within one oscillating cycle, $v_{O1}$'s and $v_{O2}$'s response to simultaneous load dumps in Figs. 7 and 8 is similar to the independent load dumps in Figs. 10–13. So $v_{O1}$ again recovers within one oscillating cycle and $v_{O2}$ within 1–3 µs.

## III. Implementation

Feedback resistors $R_{1T}$, $R_{1B}$, $R_{2T}$, and $R_{2B}$ in Fig. 15 translate reference voltages $v_{R1}$' and $v_{R2}$' to $v_{O1}$'s and $v_{O2}$'s actual targets $v_{R1}$ and $v_{R2}$ in Fig. 2. Comparator $CP_{ZCS}$ opens $M_N$ when $i_L$ into $M_N$'s resistance reaches zero to keep $i_L$ from reversing and push $L_O$ into discontinuous conduction. $v_{O1}$'s $CP_{O1}$ incorporates hysteresis $V_{H1}$ to keep noise in $v_{O1}$ from inadvertently tripping $CP_{O1}$. $V_{H1}$, however, also keeps $v_{O1}$'s ripple $\Delta v_{O1}$ from falling below $V_{H1}$'s lower threshold. This is acceptable because, with $V_{H1}$ at 10 mV, load-dump effects in $v_{O1}$ overwhelm $V_{H1}$ to determine $v_{O1}$'s accuracy.

### A. Current Sensor

The oscillator $G_{OSC}$ in Fig. 2 requires a current sensor. For testing purposes, the current sensor is the off-chip filter network in Fig. 15. Here, $R_{SI}$ and $C_{SI}$ and $R_{SO}$ and $C_{SO}$ filter $L_O$ and $R_{ESR}$'s voltage $v_L$ into voltages $v_{SI}$ and $v_{SO}$ like $L_O$ and $R_{ESR}$ filter $v_L$ into current $i_L$. So when $R_SC_S$ and $L_OR_{ESR}$ time constants match, $v_{SI} - v_{SO}$ is a linear translation of $i_L$ [31].

$C_{FI}$–$R_{FI}$ and $C_{FO}$–$R_{FO}$ high-pass filter $v_{SI}$ and $v_{SO}$ to keep their dc components from propagating through. $v_{CM}$ is a bias dc voltage that establishes $v_{FI}$ and $v_{FO}$'s common-mode level. So with an adjustable $v_{CM}$, $v_{FI}$ and $v_{FO}$ can be within the input common-mode range of the comparator they feed.

### B. Summing Comparator

Reducing $A_E$'s gain to one in Fig. 2 amounts to adding $v_{O2}$'s error $v_{O2} - v_{R2}$ to $CP_{OSC}$'s inverting input $v_I$: $(v_{O2} - v_{R2}) - v_I$. Summing comparator $CP_E$ in Fig. 15 does this with $(v_{O2} - v_{R2}) + (v_{FO} - v_{FI})$, where $v_{FO} - v_{FI}$ is $v_I$ in Fig. 2. But for the system to regulate $v_{O2}$ about $v_{R2}$ accurately, $v_{FO} - v_{FI}$'s dc component should be negligibly low. This is another reason why the current sensor high-pass filters $v_{SI}$'s and $v_{SO}$'s translation of $i_L$, to ensure $v_{FO} - v_{FI}$ is nearly zero at dc. This way, $CP_E$ and the loop can keep $v_{O2}$ near $v_{R2}$.

When $L_O$ is in discontinuous conduction, $i_L$ reaches zero before $i_L$'s translation $v_I$ in Fig. 2 reaches $CP_{OSC}$'s lower threshold. $v_{O2}$'s load therefore discharges $C_{O2}$ until $v_{O2}$'s droop finally trips $CP_{OSC}$ to start another cycle. When $v_{O2}$'s load is very light, discontinuous-conduction time $t_{DCM}$ between cycles (from Fig. 4) is long. So if $v_{O1}$'s load suddenly rises, response time $t_R$ is that much longer.

Feeding $v_{O1}$'s error $v_{O1} - v_{R1}$ into $CP_E$ in Fig. 15 allows $v_{O1}$'s error to trip $CP_E$ sooner for a faster response. In steady state, $v_{O1}$'s loop keeps $v_{O1}$ near $v_{R1}$, so $v_{O1} - v_{R1}$ is low at dc. Since $v_{FO} - v_{FI}$ is also low at dc, $CP_E$ keeps $v_{O2}$ near $v_{R2}$.

### C. Power Management

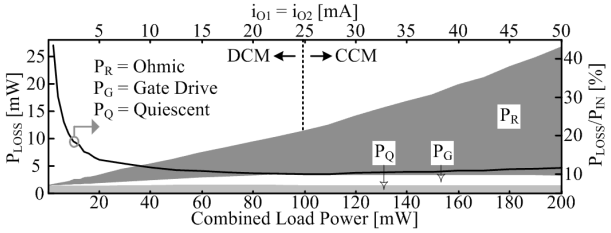


**Fig. 16**. Simulated power losses under balanced loads.

Resistances, switching gates, and the controller consume ohmic, gate-drive, and quiescent power $P_R$, $P_G$, and $P_Q$. So to minimize $P_R$ and $P_G$, transistor channel lengths are minimum at 0.6 µm and widths are wide enough to balance their ohmic and gate-drive losses, and therefore, consume the least power [32]. This way, $L_O$'s series resistance 400 mΩ and other ohmic losses in $P_R$ climb in Fig. 16 with load power from nearly zero to 22 mW, when the combined load is 200 mW. Logic and other gate-drive losses in $P_G$ rise with $f_{OSC}$ (from Fig. 5) in discontinuous conduction and flatten past 96 mW, when $f_{OSC}$ settles in continuous conduction. $CP_E$, $CP_{O1}$, and $CP_{ZCS}$ dissipate about 2 mW as $P_Q$ across load levels.

Like Fig. 17 shows, power-conversion efficiency $\eta_C$ peaks at 88% when $i_{O1}$ is 25 mA and $i_{O2}$ is 43 mA, when the combined load is 145 mW. $\eta_C$ remains above 85% when $i_{O2}$ pulls at least 25 mA or 62 mW and above 80% when $i_{O2}$ pulls more than 5 mA or 13 mW. $\eta_C$ is generally higher when $i_{O2}$ is greater than $i_{O1}$ because $M_{O2}$'s current–voltage overlap loss is lower. This is because $M_{O2}$'s initial voltage when it shorts is about 0.65 V (across its body diode) and $M_{O1}$'s is about 1.65 V

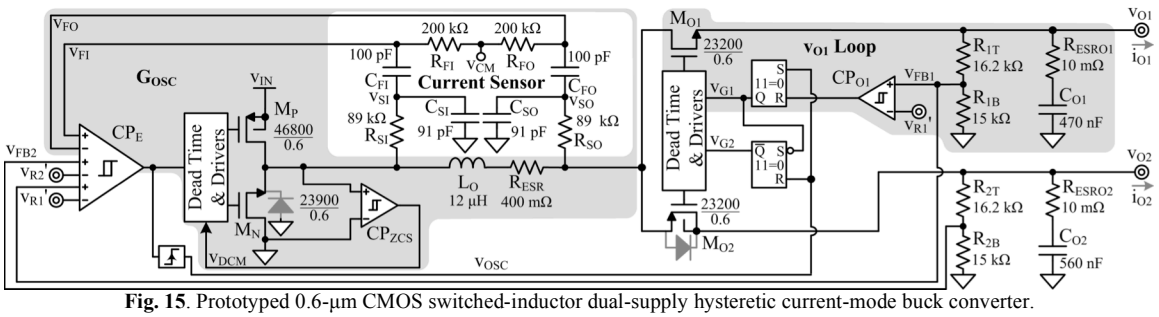


**Fig. 15**. Prototyped 0.6-µm CMOS switched-inductor dual-supply hysteretic current-mode buck converter.

(between $v_{O1}$ and $v_{O2}$ and $M_{O2}$'s body-diode voltage).

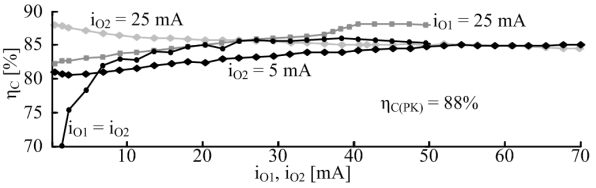


**Fig. 17**. Measured power-conversion efficiency across load levels.

## IV. PROTOTYPE

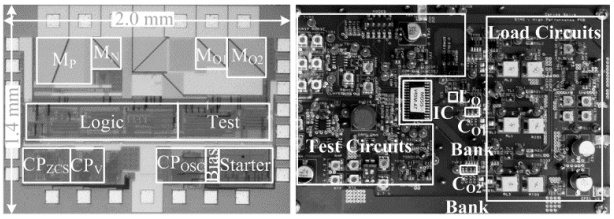


**Fig. 18**. Prototyped 0.6-µm CMOS die and two-layer board.

Everything but the current-sensor network, inductor, output capacitors, and feedback resistors in Fig. 15 are in the 1.4 × 2.0-mm$^2$ 0.6-µm CMOS die in Fig. 18. A finer-pitched CMOS process is possible, but also more costly, with lower breakdown voltages, and for proof of concept, unnecessary. The current sensor and feedback resistors are off chip for testing purposes. $L_O$ occupies 3.5 × 2.7 × 2.4 mm$^3$ of the board shown and incorporates 400 mΩ of equivalent series resistance $R_{ESR}$. $C_{O1}$ and $C_{O2}$ each occupy 1.6 × 0.81 × 0.91 mm$^3$ and incorporate 10 mΩ of series resistance.

Accuracy: Overall accuracy is the combined variation of a power-supply voltage in steady state across load levels and in response to load dumps. In this respect, $v_{O1}$'s worst-case variation with 470 nF across loads and in response to simultaneous and individual load dumps in Figs. 7–8 and 10–13 is ±78 mV or ±5% about 1.5 V. $v_{O1}$ suffers little to no effects when $v_{O2}$'s load suddenly changes because the system satisfies $v_{O1}$ before feeding $v_{O2}$. In other words, $v_{O1}$ exhibits minimal cross-regulation effects.

$v_{O2}$'s worst-case accuracy with 560 nF is +160/–177 mV or ±7% about 2.5 V. This variation is the result of individual load dumps at $v_{O1}$. $v_{O2}$ suffers these cross-regulation effects because $v_{O1}$'s load dumps drain or oversupply $L_O$ before the system can feed $v_{O2}$. $v_{O2}$'s variation in response to $v_{O2}$'s load dumps is lower at +135/–140 mV because $v_{O1}$'s response time to $v_{O1}$'s load dump delays $v_{O2}$'s response.

Higher capacitance reduces $v_{O1}$'s and $v_{O2}$'s steady-state ripples and load-dump variations. But to keep $C_{O1}$'s and $C_{O2}$'s resistances $R_{ESRO1}$ and $R_{ESRO2}$ and their ohmic losses at similar levels with higher capacitance, $C_{O1}$ and $C_{O2}$ require more space. The alternative is higher capacitance with the same volume, and as a result, higher resistance and power. Another way of reducing ripples and voltage variations is by shortening the oscillating period, except raising the converter's switching frequency also increases gate-drive losses. In other words, the tradeoff for improved accuracy is either space or power losses.

$v_{O2}$'s variation to simultaneous load dumps is lower at ±120 mV or ±5% because adding $v_{O1}$'s error into $CP_E$ in Fig. 15 accelerates $CP_E$'s response. $v_{O2}$'s total negative error in Fig. 7, however, is –90 mV from load regulation in discontinuous conduction and –140 mV from load-dump response. In other words, accuracy is worse when traversing from discontinuous to continuous conduction because the effects of load regulation and load dumps add to –230 mV.

Comparison: These output-voltage variations $\Delta v_{O(MAX)}$ result because, while power supplies react, load dumps $\Delta i_{O(LD)}$ slew output capacitors $C_O$. Applications ultimately dictate the depth and rate of these load dumps. So engineers try to save the cost of silicon and board area by designing fast power supplies. That way, output capacitance can be low and $C_O$ can occupy less space. In other words, response time $t_R$ is the underlying design variable that sets accuracy.

When assessing technologies, comparing $\Delta v_{O(MAX)}$, $\Delta i_{O(LD)}$, and $C_O$ can be misleading because the same design under different constraints produces different results. For example, a 100-mA load dump can vary the output of a 10-µs converter by 100 mV with 10 µF, 50 mV with 20 µF, and 25 mV with 40 µF. In other words, $\Delta v_{O(MAX)}$ for the same design and application can be any value $C_O$ prescribes. This is why $\Delta v_{O(MAX)}$ here is 2× to 3× higher than for competing technologies in Table I, because $C_O$ is more than 10× lower. In

**TABLE I**. COMPARISON OF THE STATE OF THE ART

| | [33] | [16] | [34] | [35] | [36] | [37] | [38] | [39] | This Work |
|---|---|---|---|---|---|---|---|---|---|
| **Tech.** | 0.5 µm | 0.35 µm | 0.25 µm | 40 nm | 55 nm | 65 nm | 0.35 µm | 0.5 µm | 0.6 µm |
| **Area** | 2.4 mm$^2$ | 3.84 mm$^2$ | 5.29 mm$^2$ | 4.00 mm$^2$ | 0.98 mm$^2$ | 1.86 mm$^2$ | 5.04 mm$^2$ | 4.40 mm$^2$ | 2.80 mm$^2$ |
| **$v_{IN}$** | 1.3–2.85 V | 2.7–3.3 V | 2.7–5 V | 2.7–3.6 V | 2.7–3.6 V | 3.4–4.3 V | 2.0–3.0 V | 1.2–2.2 V | 2.6[3]–4.2 V |
| **$v_O$** | 3, 3.6 V | 1.2, 1.8 V | 1.2, 1.8 V | 1.1–2.25 V | 1.8, 1.2 V | 1.2–2.8 V | 2.5–5 V | 3.0, 2.5 V | 1.5, 2.5 V |
| **$i_{O(MAX)}$** | 170[2] mA | 200 mA | 600 mA | 900 mA | 600 mA | 1150 mA | 400 mA | 100 mA | 120 mA |
| **$L_O$** | 1 µH<br>125 mΩ | 1 µH | 4.7 µH | 4.7 µH | 4.7 µH<br>200 mΩ | 2.2 µH | 10 µH<br>40 mΩ | 1 µH<br>100 mΩ | 12 µH<br>400 mΩ |
| **$C_O$** | 33–40 µF<br>85–80 mΩ | 22 µF | 47 µF | 4.7 µF | 4.7 µF<br>30 mΩ | 4.7 µF | 22 µF<br>300 mΩ | 10 µF<br>50 mΩ | 470–560 nF<br>10 mΩ |
| **Extra Dev.** | | | 3 µF | | | | | | |
| **$f_{SW}$** | 1 MHz | 1 MHz | 1.3 MHz | 1 MHz | 1 MHz | 1.2 MHz | 0.8 MHz | 0.5 MHz | 200–850 kHz |
| **$\Delta i_{O(LD)}$** | ±50 mA | ±90 mA | ±547 mA | ±200 mA | ±180 mA | ±150 mA | ±40 mA | ±50 mA | ±65 mA |
| **$t_R$** | 20[2] µs | 2[1] µs | 15[2] µs | 40[2] µs | 8[2] µs | 12[2] µs | 200[2] µs | 5[2] µs | 3.8 µs |
| **$\Delta v_{O(MAX)}$** | 40[2] mV | 33 mV | 60[2] mV | 60 mV | 100 mV | 50[2] mV | 200 mV | 30[1] mV | ±177 mV |
| **$\eta_{C(PK)}$** | 88% | 83% | 87% | 89% | 91% | 83% | 92% | 81% | 88% |
| **$\eta_{C(FL)}$** | 72%[2] | 72%[2] | 80%[2] | 86%[2] | 83%[2] | 83%[2] | 74%[2] | 80%[2] | 85% |
| **RFoM** | 22% | 108% | 13% | 3.4% | 63% | 46% | 1.9% | 29% | 100% |

[1]Uses linear regulator; [2]estimated values; and [3]when $v_{O1}$ = 1 V and $v_{O2}$ = 1.8 V.

practice, the application dictates how much $\Delta i_{O(LD)}$ the load requires and how much $\Delta v_{O(MAX)}$ the load can sustain, and with these, $t_R$ sets $C_O$, or in some cases, $C_O$ sets $t_R$. In other words, $\Delta i_{O(LD)}$ and $\Delta v_{O(MAX)}$ are independent application parameters and $t_R$ and $C_O$ are codependent design variables that are normally independent of $\Delta i_{O(LD)}$ and $\Delta v_{O(MAX)}$. So $t_R$ alone is a good way of assessing and comparing designs.

The system here responds quickly at 0.9–3.8 µs because the oscillator's response time is practically the time $L_O$'s $i_L$ requires to slew to its target. This is as fast as a switched inductor possibly can. [16] in Table I is slightly faster at 2 µs because a linear regulator is the one that responds to load dumps. This linear regulator, however, requires additional silicon area and power, so die size is 37% larger with 42% shorter channel lengths and peak and full-load efficiencies are 5% and 13% lower.

[39] is a close second at 5 µs, but die area is 57% larger and efficiencies are 7% and 5% lower. [36] is third at 8 µs, but with 91% shorter channel lengths $L_{MIN}$. [37] is next at 12 µs, but with 89% shorter $L_{MIN}$ and 5% and 2% lower efficiencies. [34] follows at 15 µs because a capacitor between outputs couples errors, like $CP_E$ here does, to accelerate response time. This capacitor, however, is off chip, die size is 89% larger with 58% shorter $L_{MIN}$, and efficiencies are 1% and 5% lower.

Relative Figure of Merit: Maximum current $i_{O(MAX)}$, peak and full-load efficiencies $\eta_{C(PK)}$ and $\eta_{C(FL)}$, maximum response time $t_{R(MAX)}$, and cost of silicon area $A_{SI}$, additional off-chip components $\Delta N_{OC}$, and process technology define the merits of a power supply. Although not always weighed evenly, a relative figure of merit (RFoM) should climb with $i_{O(MAX)}$, $\eta_{C(PK)}$, $\eta_{C(FL)}$, and minimum channel length $L_{MIN}$ (for lower cost) and fall with $t_{R(MAX)}$, $A_{SI}$, and $\Delta N_{OC}$:

$$\text{RFoM} \equiv \frac{i_{O(MAX)}\eta_{C(PK)}\eta_{C(FL)}L_{MIN}}{t_{R(MAX)}A_{SI}\left(1+\Delta N_{OC}\right)\text{PoR}}, \qquad (7)$$

where PoR is a normalizing point of reference. So when normalizing to this system, whose $i_{O(MAX)}$ is 120 mA, $\eta_{C(PK)}$ is 88%, $\eta_{C(FL)}$ is 85%, $L_{MIN}$ is 0.6 µm, $t_{R(MAX)}$ is 3.8 µs, $A_{SI}$ is 2.8 $mm^2$, and $\Delta N_{OC}$ is 0, PoR is 5.0616E3 and RFoM is 1.

Using this metric, [16]'s rating is slightly higher by 8% because 67% higher $i_{O(MAX)}$ and 47% lower $t_{R(MAX)}$ edge other deficiencies. (Note that [16]'s $t_{R(MAX)}$ is an unmeasured estimate.) [36]'s and [37]'s ratings are 37% and 54% lower than the system presented here primarily because $L_{MIN}$'s are 91% and 89% lower. [39]'s, [33]'s, and [34]'s ratings are 71%, 78%, and 87% lower because the balance between response times and efficiencies is less favorable. [35]'s rating is 96% lower because $L_{MIN}$ is 83% shorter and $t_{R(MAX)}$ is 10.5× higher and [38]'s ratings is 98% lower mostly because $t_{R(MAX)}$ is 53× higher. In other words, this work and [16] rate similarly high, except this work is more efficient and [16] is slightly faster.

## V. Conclusions

The 0.6-µm CMOS switched-inductor dual-supply system presented here responds to rising and falling 45–65-mA load dumps within 3.8 µs to keep its outputs within ±78 mV and +160 and –177 mV of their 1.5- and 2.5-V targets with 88% and 85% peak and full-load efficiencies. Response time is essentially the time the inductor current requires to slew to its target, which is as fast as any switched inductor possibly can. The system is so quick and stable because the hysteretic oscillator that ripples the inductor current about the loop-defined average responds within the propagation delay of a comparator: within one cycle. Response time is critical because faster supplies require less capacitance to supply load dumps and maintain accuracy. In literature, only [16] is slightly faster at 2 µs because a linear regulator bypasses the inductor to supply load dumps. [16]'s tradeoffs are 37% larger die, 42% shorter channel lengths, and 5% and 13% lower peak and full-load efficiencies. Sacrificing conversion efficiency, die area, and process technology for the sake of speed, however, shortens battery life and raises cost, which limits market penetration, profits, and overall impact.

## Acknowledgement

The authors thank J.D. Morris, B. Legates, T. Bonte, and Linear Technology for their sponsorship and support.

## References

[1] D. Puccinelli and M. Haenggi, "Wireless sensor networks: applications and challenges of ubiquitous sensing," *IEEE Circuits and Systems Magazine*, vol. 5, no. 3, pp. 19–31, 2005.

[2] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A.P. Chandrakasan, "A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System," *IEEE Jour. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, Apr. 2010.

[3] B. Bae, Y. Shim, K. Koo, J. Cho, J.S. Pak, and J. Kim, "Modeling and Measurement of Power Supply Noise Effects on an Analog-to-Digital Converter Based on a Chip-PCB Hierarchical Power Distribution Network Analysis," *IEEE Trans. Electromagnetic Compatibility*, vol. 55, no. 6, pp. 1260−1270, Dec. 2013.

[4] E. Sanchez-Sinencio and A.G. Andreou, *Low-Voltage/Low-power Integrated Circuits and Systems*, IEEE Press, New York, 1998.

[5] M.K. Stojcev, M.R. Kosanovic, and L.R. Golubovic, "Power management and energy harvesting techniques for wireless sensor nodes," *Int. Conf. Telecomm. in Modern Satellite, Cable, and Broadcasting Services*, pp.65−72, Oct. 2009.

[6] S. Hua and G. Qu, "Voltage setup problem for embedded systems with multiple voltages," *IEEE Trans. Very Large Scale Integration Systems*, vol. 13, no. 7, pp. 869−872, Jul. 2005.

[7] L. Yung-Hsiang and G. De Micheli, "Comparing system level power management policies," *IEEE Design & Test of Computers*, vol. 18, no. 2, pp. 10−19, Mar./Apr. 2001.

[8] J. Park, D. Shin, N. Chang, and M. Pedram, "Accurate modeling and calculation of delay and energy overheads of dynamic voltage scaling in modern high-performance microprocessors," *ACM/IEEE Int. Sym. Low-Power Electronics and Design*, pp. 419–424, Aug. 2010.

[9] G.A. Rincon-Mora, *Analog IC Design with Low-Dropout Regulators*, McGraw-Hill, New York, 2009.

[10] M. Ordonez, J.E. Quaicoe, and M.T. Iqbal, "Critical Parameters in the Transient Response of Synchronous Buck Converters," *IEEE Power Electronics Specialists Conference*, pp. 2189–2195, Jun. 2007.

[11] C.O. Mathúna, N. Wang, S. Kulkarni, and S. Roy, "Review of Integrated Magnetics for Power Supply on Chip (PwrSoC)," *IEEE Trans. Power Electronics*, vol. 27, no. 11, pp. 4799–4816, Nov. 2012.

[12] D. Kwon and G.A. Rincon-Mora, "Single-Inductor–Multiple-Output Switching DC–DC Converters," *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 56, no. 8, pp. 614–618, Aug. 2009.

[13] S. Chattopadhyay and S. Das, "A Digital Current-Mode Control Technique for DC–DC Converters," *IEEE Trans. Power Electronics*, vol. 21, no. 6, pp. 1718–1726, Nov. 2006.

[14] X. Duan and A.Q. Huang, "Current-mode variable-frequency control architecture for high-current low-voltage DC-DC converters," *IEEE Trans. Power Electronics*, vol. 21, no. 4, pp. 1133–1137, Jul. 2006.

[15] E. Bonizzoni, F. Borghetti, P. Malcovati, F. Maloberti, and B. Niessen, "A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter," *IEEE Int. Solid-State Circuits Conf.*, pp. 526–619, Feb. 2007.

[16] Y. Zhang and D. Ma, "A Fast-Response Hybrid SIMO Power Converter with Adaptive Current Compensation and Minimized Cross-Regulation," *IEEE Jour. Solid-State Circuits*, vol. 49, no. 5, pp. 1242–1255, May 2014.
[17] M.Y. Jung, S.H. Park, J.S. Bang, D.C. Park, S.U. Shin, and G.H. Cho, "12.5 An error-based controlled single-inductor 10-output DC-DC buck converter with high efficiency at light load using adaptive pulse modulation," *IEEE Int. Solid-State Circuits Conf.*, pp. 1–3, Feb. 2015.
[18] D. Ma, W.H. Ki, and C.Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE Jour. Solid-State Circuits*, vol. 38, no. 6, pp. 1007–1014, Jun. 2003.
[19] D. Ma and R. Bondade, "Enabling Power-Efficient DVFS Operations on Silicon," *IEEE Circuits and Systems Magazine*, vol. 10, no. 1, pp. 14–30, First Quarter 2010.
[20] M.H. Huang, Y.N. Tsai, and K.H. Chen, "Sub-1 V Input Single-Inductor Dual-Output (SIDO) DC–DC Converter With Adaptive Load-Tracking Control (ALTC) for Single-Cell-Powered Systems," *IEEE Trans. Power Electronics*, vol. 25, no. 7, pp. 1713–1724, Jul. 2010.
[21] H.P. Le, C.S. Chae, K.C. Lee, S.W. Wang, G.H. Cho, and G.H. Cho, "A Single-Inductor Switching DC–DC Converter With Five Outputs and Ordered Power-Distributive Control," *IEEE Jour. Solid-State Circuits*, vol. 42, no. 12, pp. 2706–2714, Dec. 2007.
[22] M.H. Huang and K.H. Chen, "Single-Inductor Multi-Output (SIMO) DC-DC Converters With High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices," *IEEE Jour. Solid-State Circuits*, vol. 44, no. 4, pp. 1099–1111, Apr. 2009.
[23] K.S. Seol, Y.J. Woo, G.H. Cho, G.H. Gho, and J.W. Lee, "A Synchronous Multioutput Step-Up/Down DC–DC Converter With Return Current Control," *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 56, no. 3, pp. 210–214, Mar. 2009.
[24] K.C. Lee, C.S. Chae, G.H. Cho, and G.H. Cho, "A PLL-based high-stability single-inductor 6-channel output DC-DC buck converter," *IEEE Int. Solid-State Circuits Conf.*, pp. 200–201, Feb. 2010.
[25] S.W. Wang, G.H. Cho, and G.H. Cho, "A high-stability emulated absolute current hysteretic control single-inductor 5-output switching DC-DC converter with energy sharing and balancing," *IEEE Int. Solid-State Circuits Conf.*, pp. 276–278, Feb. 2012.
[26] C.J. Solis and G.A. Rincon-Mora, "Nested hysteretic current-mode single-inductor multiple-output (SIMO) boosting buck converter," *IEEE Int. Conf. New Circuits and Systems*, pp. 1–4, Jun. 2013.
[27] N. Keskar and G.A. Rincon-Mora, "Designing an Accurate and Robust LC-Compliant Asynchronous ΣΔ Boost DC-DC Converter," *IEEE Int. Symp. Circuits and Systems*, pp. 549–552, May 2007.
[28] G.A. Rincon-Mora, *Power IC Design*, Lulu, Raleigh, 2009.
[29] R. Redl, B.P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," *Applied Power Electronics Conference and Exposition*, pp. 170–176, Feb. 1998.
[30] C.J. Solis and G.A. Rincon-Mora, "Stability analysis & design of hysteretic current-mode switched-inductor buck DC-DC converters," *IEEE Int. Conf. in Electronics, Circuits, and Systems*, pp. 811–814, Dec. 2013.
[31] H.P. Forghani-Zadeh and G.A. Rincon-Mora, "An Accurate, Continuous, and Lossless Self-Learning CMOS Current-Sensing Scheme for Inductor-Based DC-DC Converters," *IEEE Jour. Solid-State Circuits*, vol. 42, no. 3, pp. 665–679, Mar. 2007.
[32] S. Kim and G.A. Rincon-Mora, "Achieving high efficiency under micro-watt loads with switching buck dc-dc converters," *Jour. Low Power Electronics*, vol. 4, no. 2, pp. 229–240, Aug. 2009.
[33] D. Ma, W.H. Ki, C.Y. Tsui, and P.K.T. Mok, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode," *IEEE Jour. Solid-State Circuits*, vol. 38, no. 1, pp. 89–100, Jan. 2003.
[34] W. Xu, Y. Li, X. Gong, Z. Hong, and D. Killat, "A Dual-Mode Single-Inductor Dual-Output Switching Converter With Small Ripple," *IEEE Trans. Power Electronics*, vol. 25, no. 3, pp. 614–623, Mar. 2010.
[35] W.C. Chen, Y.P. Su, T.C. Huang, T.W. Tsai, R.H. Peng, K.L. Lin, K.H. Chen, Y.H. Lin, C.C. Lee, S.R. Lin, and T.Y. Tsai, "Single-Inductor Quad-Output Switching Converter With Priority-Scheduled Program for Fast Transient Response and Unlimited Load Range in 40 nm CMOS Technology," *IEEE Jour. Solid-State Circuits*, vol. 50, no. 7, pp. 1525–1539, Jul. 2015.
[36] Y.H. Lee, T.C. Huang, Y.Y. Yang, W.S. Chou, K.H. Chen, C.C. Huang, and Y.H. Lin, "Minimized Transient and Steady-State Cross Regulation in 55-nm CMOS Single-Inductor Dual-Output (SIDO) Step-Down DC-DC Converter," *IEEE Jour. Solid-State Circuits*, vol. 46, no. 11, pp. 2488–2499, Nov. 2011.
[37] C.W. Kuan and H.C. Lin, "Near-independently regulated 5-output single-inductor DC-DC buck converter delivering 1.2W/mm$^2$ in 65nm CMOS," *IEEE Int. Solid-State Circuits Conf.*, pp. 274–276, Feb. 2012.
[38] J. Kim, D.S. Kim, and C. Kim, "A Single-Inductor Eight-Channel Output DC–DC Converter With Time-Limited Power Distribution Control and Single Shared Hysteresis Comparator," *IEEE Trans. Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3354–3367, Dec. 2013.
[39] Y.J. Moon, Y.S. Roh, J.C. Gong, and C. Yoo, "Load-Independent Current Control Technique of a Single-Inductor Multiple-Output Switching DC–DC converter," *IEEE Transactions Circuits and Systems II: Express Briefs*, vol. 59, no. 1, pp. 50–54, Jan. 2012.

**Carlos J. Solis** (GSM'10) received his B.S. ans M.S. from the University of Puerto Rico at Mayaguez in 2010 and the Georgia Tech in 2012, respectively. He is currently pursuing his Ph.D. at the Georgia Tech Analog, Power, and Energy (GTAPE) research. His research interests include switching power supplies, and analog IC design.

**Gabriel A. Rincón-Mora** (StM'90, GSM'93, M'97, SM'01, F'11) worked for Texas Instruments in 1994-2003, was an Adjunct Professor at Georgia Tech in 1999-2001, and has been a Professor at Georgia Tech since 2001 and a Visiting Professor at National Cheng Kung University in Taiwan since 2011. He is also a Fellow of the IET and his scholarly products include 9 books, 4 book chapters, 38 patents issued, over 170 publications, over 26 commercial power-chip designs, and over 110 invited talks. He is also a Fellow of IET.