Autonomous and Programmable
12-W 10-kHz Single-Cell Li-Ion Battery Tester

Qian Zhi, Gabriel A. Rincón-Mora, *Fellow, IEEE*, and Pengyu Gu

Abstract—**Portable electronics like laptops are ubiquitous nowadays and they depend on batteries for power. Unlike traditional power supplies, batteries have limited capacity, cycle life, power capability, and many other restrictions. To improve battery performance or select the best battery for an application, engineers need to accurately extract the battery's parameters through a series of experiments. Existing battery testers often fall short in current flexibility, accuracy, and battery voltage range, thus cannot accommodate all the necessary experiments and different battery types with a single setup. In this paper, a 12-W battery tester using linear charger/discharger and bipolar power supply is proposed. The tester can provide programmable current profile up to 3.3 A and 10 kHz with a wide battery voltage range to accommodate for different battery types. The tester can also regulate battery voltage and perform constant voltage charge and discharge. A prototype is implemented, and the testing capabilities are demonstrated with common battery experiments using a commercial 18650 cylindrical battery. The experimental results show the tester's excellent current accuracy and flexibility.**

Index Terms—**Programmable tester, Li-ion batteries, charger, discharger, alternating current, internal resistance, state of charge (SoC).**

I. BATTERIES IN MICROELECTRONICS

BATTERIES are popular energy sources to portable electronics such as cellphones, wireless headphones, and laptops. Components inside the device, including the digital-signal processors (DSPs), data converters, power amplifiers, antennas, and sensors, depend on the battery to operate as shown in Fig. 1. As the world's demand for microelectronics continue to grow, the battery market is expected to expand steadily. It is projected that the global market size for lithium-ion batteries will double in the next five years to $91.9 billion [1].

Despite the continuous development of battery technologies, there are still many challenges and limitations. The parameters that restrict a battery's performance and applications include capacity, cycle life, series resistance, self-discharge, power capability, and energy density [2-5]. To understand the battery's limitations and explore methods to improve battery performance, it is necessary to experimentally extract the battery's parameters and conduct rigorous testing [6].

However, battery testing procedures are often lengthy and prone to errors, which calls for an accurate and autonomous tester. For example, the cycle life test for a typical Li-ion battery
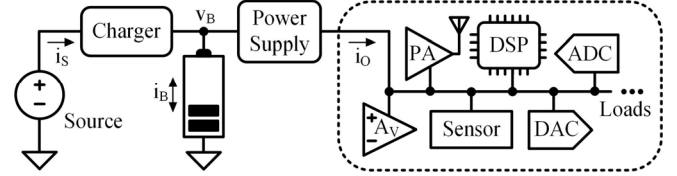
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Fig. 1. Battery-powered microelectronic system.

requires hundreds of charge-discharge cycles, which can take months to complete [7, 8]. Furthermore, the necessary experiments to fully characterize a battery require the tester to source/sink programmable current with high accuracy, which cannot be done with conventional power supplies. Batteries like lithium ions also have strict requirements on the operating voltage, and a constant current–constant voltage (CC–CV) charge is necessary to prevent overcharging.

Among the battery testers investigated, [9-11] can source and sink programmable current. [9, 10] can source and sink a large current, which is necessary when testing batteries with high power capability such as electric vehicle batteries. However, they are both limited in current ripple frequency and battery voltage range. Commercial linear testers [12, 13] have high accuracy and wide battery voltage range, but their slow response time limits the maximum current ripple frequency that can be applied.

In this paper, we propose a compact 12-W battery tester that is capable of charging and discharging the battery with arbitrary current profile up to 3.3 A and 10 kHz. The proposed tester has a high bandwidth, high accuracy, seamless CC–CV transition, and can discharge the battery below 0 V. The tester is based on the linear charger proposed by our group in [14].

The rest of the paper is organized as follows: Section II discusses the tester circuit and operation. Section III demonstrates the testing capability. Section IV reviews and compares the tester's performance with the state of the art.

II. PROPOSED BATTERY TESTER

A. Charger

A linear charger is implemented to source programmable current for the battery as shown in Fig. 2. The linear charger contains two negative feedback loops: a current loop to regulate battery current i_B and a voltage loop to regulate battery voltage v_B. The current loop consists of transconductance amplifier A_{GP}, MOSFET M_P, resistor R_P, R_{P1}, R_{P2}, and R_{P3}. The voltage loop consists of op amp A_{VP}, diode D_P, MOSFET M_P, current-sense resistor R_S, and battery internal resistance R_B.

During constant current (CC) operation, the voltage loop is off because v_B is lower than the reference voltage v_{BH}, and A_{VP} outputs a voltage close to the negative power supply, forcing diode D_P to be off. Meanwhile, the current loop has high gain

Fig. 2. Proposed charger.

R_P	1.2 Ω	A_{GP}	LM13700
R_{P1}	1 kΩ	D_P	EMP11FH
R_{P2}	1 kΩ	A_{VP}	THS4081
R_{P3}	500 Ω	M_P	RD3L140SP
R_S	100 mΩ		

Fig. 3. Simulated loop gain in CC, CV, and CC−CV.

due to the high impedance at v_{GH}. A_{GP}'s input voltage v_{NH} is regulated to be approximately equal to v_{PH}, which is set by the reference voltage v_{RH}. v_{NH} is then level-shifted by the resistor divider R_{P1} and R_{P2} to reach a higher voltage at v_C. The voltage across R_P induces a current i_B to flow to the battery. R_{P1} and R_{P2} are chosen to be relatively high resistance to ensure most of the current through R_P flows into the battery. R_{P3} compensates for the voltage drop across R_{P1} due to the input current of A_{GP} and $R_{P3} = R_{P1} \parallel R_{P2}$.

To analyze the current loop gain, the current loop is "broken" at node v_C. When a small signal is injected, the voltage-divided fraction of the signal reaches v_{NH} and gets amplified by A_{GP}'s transconductance G_{GP}. The output current flows into the total impedance at the gate of M_P and determines the gate voltage v_{GH}. M_P responds to v_{GH} by pulling current i_B, which flows through R_P and sets the voltage v_C. The current loop gain is

$$A_{LGI} = \left[\frac{R_{P2} \parallel R_{GI}}{R_{P1} + \left(R_{P2} \parallel R_{GI} \right)} \right] G_{GP} Z_{GH} \left(\frac{g_{MP} R_P}{1 + g_{MP} R_P} \right), \quad (1)$$

where R_{GI} is the input resistance of A_{GP} and g_{MP} is the transconductance of M_P. Z_{GH} is the total impedance at v_{GH}:

$$Z_{GH} = R_{GO} \parallel Z_{V(CL)} \parallel \frac{1}{sC_{GH}}, \quad (2)$$

where R_{GO} is the output resistance of A_{GP}, C_{GH} is the gate capacitance of M_P, and $Z_{V(CL)}$ is the closed-loop impedance of the voltage loop.

The small signal gain of the current and voltage loops during CC operation are shown in Fig. 3(a). The current loop has one low-frequency pole p_G at the gate of M_P at around 1 kHz. All the other parasitic poles occur above 0-dB frequency f_{0dB}, which results in a stable phase margin of 90° and a bandwidth of 10 MHz. The voltage loop's gain is below -50 dB during CC operation and does not interfere with the current loop. The total loop gain is the sum of the voltage and current loop gains, which is approximately equal to A_{LGI} during CC operation.

During constant voltage (CV) operation, $v_B \approx v_{BH}$ and A_{VP}'s output voltage rises. Therefore, D_P becomes forward biased and turns on the voltage loop. Z_{GH} becomes small as A_{VP}'s low output impedance dominates the total gate impedance. Therefore, the current loop gain is collapsed. Meanwhile, the voltage loop regulates v_B to the reference voltage v_{BH} through the negative feedback path.

To analyze the voltage loop gain, the loop is "broken" at v_B. When a small signal is injected, it will be amplified by A_{VP} before passing through the voltage divider formed by the diode impedance Z_{DP} and $Z_{I(CL)} \parallel (1/sC_{GH})$. The gate voltage of M_P

sets battery current i_B, which flows into R_B to determine v_B. The voltage loop gain is

$$A_{LGV} = \left(\frac{A_{VP}}{1 + \dfrac{s}{p_{AVP}}} \right) \left[\frac{Z_{I(CL)} \parallel \dfrac{1}{sC_{GH}}}{Z_{DP} + \left(Z_{I(CL)} \parallel \dfrac{1}{sC_{GH}} \right)} \right] \left(\frac{g_{MP} R_B}{1 + g_{MP} R_P} \right), \quad (3)$$

where p_{AVP} is A_{VP}'s internal pole, and $Z_{I(CL)}$ is the current loop's closed-loop impedance.

The small signal gain of the current and voltage loops during CV operation are shown in Fig. 3(b). The internal pole of the op amp p_{AVP} is the dominant pole while the gate pole is pushed to unity-gain frequency due to the low impedance at v_G, resulting in a stable phase margin of 45°. The current loop gain is below -30 dB across the frequency spectrum and does not interfere with the voltage loop operation.

When the charger transition from CC to CV operation, the total impedance at v_G decreases as D_P becomes forward biased. Therefore, A_{LGI} decreases and A_{LGV} increases simultaneously. As shown in Fig. 3(c), the current loop's dominant pole p_G is pushed to a higher frequency as the gate impedance decreases. The voltage loop interacts with the current loop and introduces a zero-pole pair (z_{LGV}, p_{LGV}) in A_{LGI}. The phase margin is always higher than 90 degrees because z_{LGV} precedes p_{LGV}. On the other hand, A_{LGV} only has one dominant pole p_{AVP} with all other zeros/poles above f_{0dB} as shown in Fig. 3(d), thus has a stable phase margin of 90 degrees.

To further investigate the zero-pole pair in A_{LGI}, $Z_{V(CL)}$ in (2) can be expressed as

$$Z_{V(CL)} = Z_{V(OL)} \parallel \frac{Z_{V(OL)}}{A_{LGV}}, \quad (4)$$

where $Z_{V(OL)}$ is the open-loop impedance looking into D_P. When A_{LGV} is high, $Z_{V(OL)}/A_{LGV}$ dominates the closed-loop impedance and $Z_{V(CL)}$ increases as A_{LGV} decreases. Because $Z_{V(CL)}$ dominates the total gate impedance at low frequencies, Z_{GH} will increase. Therefore, A_{GP}'s output current will flow into a higher impedance, which introduces a zero z_{LGV}. When C_{GH}'s impedance dominates Z_{GH} at higher frequencies, the effect of the zero is reversed and a reversal pole p_{LGV} is introduced.

B. Discharger

The charger topology described previously is modified to form a discharger using a negative supply voltage as shown in Fig. 4. The negative supply provides the needed headroom for R_N, M_N,

Fig. 4. Proposed discharger.

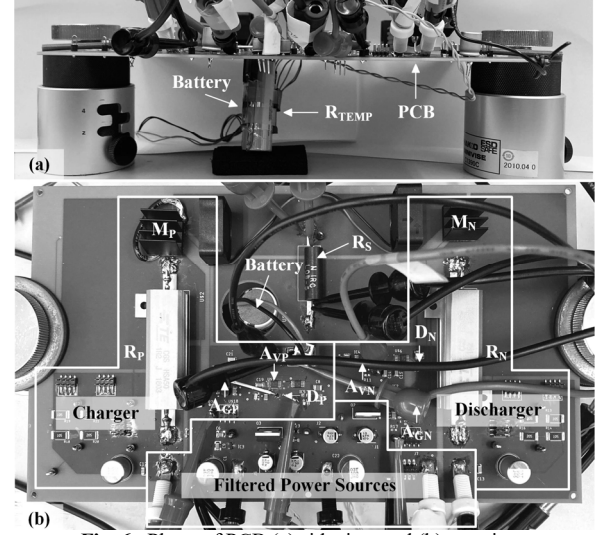| R_N | 1.2 Ω | A_{GN} | LM13700 |
R_{N1}	2 kΩ	D_N	EMP11FH
R_{N2}	1 kΩ	A_{VN}	THS4081
R_{N3}	667 Ω	M_N	RD3L150SN
R_S	100 mΩ		

Fig. 5. Full tester schematics.

Fig. 6. Photo of PCB (a) sideview and (b) top view.

TABLE I
TEST BATTERY SPECIFICATIONS

	PL-052025	IMR18650	NCR18650B
Chemistry	Li-Polymer	$LiMn_2O_4$	-
Cell Type	Pouch	Cylindrical	Cylindrical
Size	20.5/25.5/5 mm	Std. 18650	Std. 18650 Cell
Capacity	170 mAh	2500 mAh	3250 mAh
Voltage	3.0-4.2 V	2.75-4.2 V	2.5-4.2 V
Std. Charge	170 mA	1.25 A	1.625A

and R_S to discharge the battery below 0 V without pushing M_N into triode region or decreasing the discharge current. The current loop consists of transconductance amplifier A_{GN}, MOSFET M_N, resistor R_N, R_{N1}, R_{N2}, and R_{N3}. The voltage loop consists of op amp A_{VN}, diode D_N, MOSFET M_N, current-sense resistor R_S, and R_B. The major difference is that A_{GN} is connected in inverting amplifier configuration to generate a negative voltage v_D with a positive reference voltage v_{RL}.

During CC operation, D_N is reverse-biased, and the voltage loop is turned off. The current loop has high gain due to high gate impedance. As v_B decreases close to the reference voltage v_{BL}, the diode starts conducting and the gate impedance decreases due to A_{VN}'s low output resistance. Therefore, the voltage loop gains strength while the current loop loses strength. During CV operation, the voltage loop dominates, and the current loop gain is diminished by the low gate impedance. The small signal gain of the discharger resembles the charger circuit shown in Fig. 3, thus will not be repeated here.

C. Prototype

The charger and discharger described above are designed and implemented with a PCB. A prototype tester is completed with benchtop instruments as shown in Fig. 5. Reference voltage v_{RH}, v_{RL}, v_{BH}, and v_{BL} are provided by function generators. The charge current and discharge current are sensed using Kelvin connection with a 100 mΩ current-sense resistor R_S. The charger/discharger output voltage v_O and battery voltage v_B are acquired using digital multimeters (DMMs) and oscilloscopes. Battery temperature T_B is acquired using a thermistor. The experimental setup is shown in Fig. 6.

The circuit components are chosen to accommodate battery current up to 3.3 A. The minimum regulation current needs to overcome the noise current injected into the battery. The noise current is measured to be 50 mA_{RMS}, thus the minimum regulation current is determined to be 10× higher at 500 mA. The supply voltage v_{DD} and v_{SS} are chosen to minimize the drain-source voltage of the MOSFETs while guaranteeing operation in saturation, so that the conduction loss and heat generation is reduced. To further manage the heat produced by the MOSFETs, heat sinks and small fans are used to improve the heat transfer between the MOSFETs and the ambient air, maintaining MOSFET temperature below 50 °C.

The DC power supplies, function generators, DMMs, and oscilloscopes are controlled by a PC using LabVIEW through the GPIB interface. To accommodate for rigorous testing, all experiment procedures are programmed in LabVIEW to achieve fully autonomous testing. The acquired data is exported in Excel format at the end of the experiment for analysis.

Both hardware and software protections are implemented in the prototype tester to ensure the tested Li ion operates within the safe voltage, current, and temperature range and prevent potential hazards such as irreversible performance degradation, thermal runaway, or even explosion [15-17]. The voltage loops of the proposed circuit regulate v_B between v_{BH} and v_{BL} to avoid overcharging and overdischarging. The power supply's current limit is set to the maximum i_B to prevent overcurrent. LabVIEW software is programmed to terminate the experiment when monitored v_B, i_B, or T_B exceed the user-specified range.

III. TESTING CAPABILITY

The prototype tester is used to perform common tests with three commercial Li ions detailed in Table I. All test batteries are cycled five times prior to testing to ensure stable capacity decay. Because the test procedures and the tester's operation are the same for all three batteries, the results from NCR18650B are presented for demonstration in the following discussion.

A. Energy

A battery's energy information can be extracted through a charge-discharge cycle as shown in Fig. 7. The cycle can be divided into five sections: CC charge $t_{C(CC)}$, CV charge $t_{C(CV)}$,
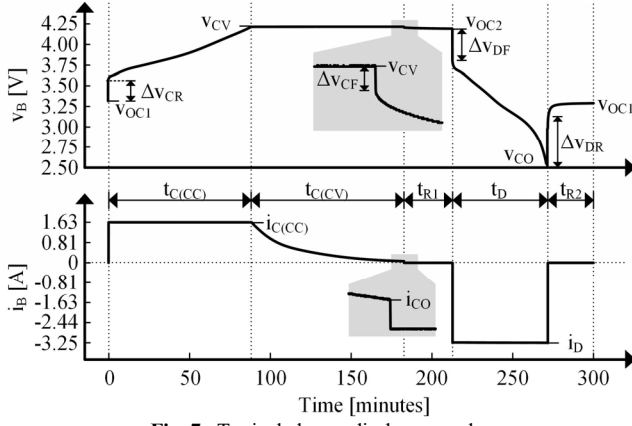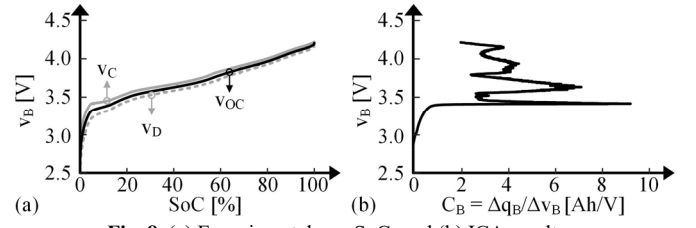
Fig. 7. Typical charge-discharge cycle.

Fig. 8. (a) Experimental v_{OC}-SoC, and (b) ICA results.

Fig. 9. (a) Pulsed charge/discharge cycle, and (b) two charge pulses.

rest t_{R1}, discharge t_D, and rest t_{R2}. The fully depleted battery's initial open-circuit voltage is v_{OC1}. During $t_{C(CC)}$, constant charge current $i_{C(CC)}$ is applied to the battery and v_B rises. During $t_{C(CV)}$, v_B is held at v_{CV} while charge current i_C is slowly decreased to the chosen cutoff level i_{CO}. The fully charged battery is rested for t_{R1} while v_B undergoes relaxation to reach open-circuit voltage v_{OC2}.

During t_D, the battery is discharged with constant current i_D to discharge cutoff voltage v_{CO}. The fully discharged battery is rested during t_{R2}, and the open-circuit voltage of the battery returns to the initial value v_{OC1}. The sharp rise/drop Δv_{CR}, Δv_{CF}, Δv_{DF}, and Δv_{DR} are due to the voltage across internal resistance R_B when a current is suddenly applied or removed.

Capacity: The charge capacity is the amount of charge $q_{B(TOT)}$ that can be extracted from a fully charged battery:

$$q_{B(TOT)} = \int_0^{t_D} i_D dt . \tag{5}$$

For demonstration, the parameters i_C, v_{CV}, i_{CO}, i_D, v_{CO}, t_{R1}, and t_{R2} are 1.625 A, 4.2 V, 65 mA, 3.25 A, 2.5 V, 30 minutes, and 30 minutes. i_D is integrated to obtain a capacity of 3187 mAh.

Energy Efficiency: The energy efficiency for the charge-discharge cycle is the ratio of the energy that can be extracted from the battery during discharge (E_D) and the energy that is delivered to the battery during charge (E_C):

$$\eta_E = \frac{E_D}{E_C} = \frac{\int_0^{t_D} i_D v_B dt}{\int_0^{t_C} i_C v_B dt} . \tag{6}$$

The energy efficiency is usually much lower than 100% due to energy loss through R_B. E_C, E_D, and η_E for the cycle described previously are calculated to be 44.0 kJ, 37.7 kJ, and 85.5%, respectively.

State-of-Charge: A battery's state of charge (SoC) is the fraction of remaining charge compared to the total charge capacity and can be calculated as

$$SoC = SoC_0 + \frac{\Delta q_x}{q_{B(TOT)}} = SoC_0 + \frac{\int_0^{t_x} i_B dt}{q_{B(TOT)}} , \tag{7}$$

where SoC_0 is the initial SoC and Δq_x is the charge injected or extracted from the battery during t_x. When the battery is initially discharged to the cutoff voltage v_{CO}, its SoC_0 is defined to be zero. Therefore, the battery's SoC at any instance can be calculated by integrating the measured i_B if $q_{B(TOT)}$ is known.
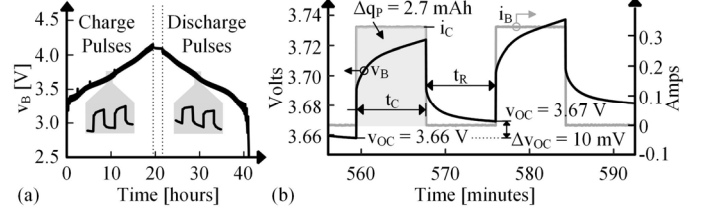
Estimating the battery's SoC is important as it provides the user with information on usable charge left in the battery. One method to estimate the battery's SoC is through the relationship between open-circuit voltage v_{OC} and SoC [18, 19]. To obtain this relationship, the charge-discharge cycle shown in Fig. 7 is modified with low i_C and i_D so that the voltage across R_B is small [18]. For demonstration, i_C and i_D are chosen to be C/20 (162.5 mA) and the rest time t_{R1} and t_{R2} are chosen to be 2 hours.

The battery's SoC with respect to time is calculated from measured i_B and $q_{B(TOT)}$ using (7) with SoC_0 defined to be zero. v_B is then plotted against SoC, and the charge voltage curve v_C and discharge voltage curve v_D are averaged to obtain v_{OC} as shown in Fig. 8(a). v_C is at a slightly higher voltage compared to v_D due to R_B. The estimated v_{OC} does not consider the hysteresis effect of the battery and assumes a constant v_{OC} at an SoC whether the battery was charged or discharged [20].

Similarly, Incremental Capacity Analysis (ICA) uses a charge-discharge cycle with low current to observe the battery's ability to hold charge. ICA investigates the amount charge increment (Δq_B) for a voltage increment (Δv_B), which can also be interpreted as the capacitance of the battery C_B at an instance. For demonstration, Δq_B is fixed to be 2.71 mAh, corresponding to 1 minute of CC charging at C/20 (162.5 mA). The $\Delta q_B/\Delta v_B$ curve derived from v_C in Fig. 8(a) is shown in Fig. 8(b).

The nonlinearity of v_B in Fig. 8(a) translates to the peaks and troughs of C_B in Fig. 8(b). The peaks in the ICA plot correspond to the region where v_C rises slowly with SoC and have been linked to specific chemical reactions in Li-ion batteries [18]. Therefore, ICA can reflect the electrochemical properties of the battery and be used to estimate its state of health [21].

Another method to extract the relationship between v_{OC} and SoC is shown in Fig. 9. The battery is fully charged using alternating intervals of current pulse t_C and rest t_R. v_{OC} can be obtained at the end of each t_R. Similarly, the battery is discharged negative current pulses. For demonstration, the current pulse duration and rest time are both set to be 10 minutes. The amplitude of the charge current (i_C) and discharge current is set to be C/10 (325 mA).

For a Li-ion battery with known chemical properties, the diffusion coefficient of the lithium ions can also be obtained using the open-circuit voltage change Δv_{OC} with respect to the charge variation Δq_P and time t_C during a pulse. This method is
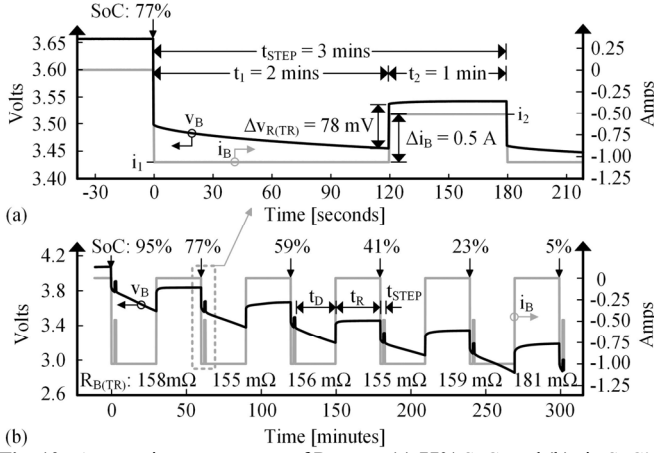
(a)

(b)

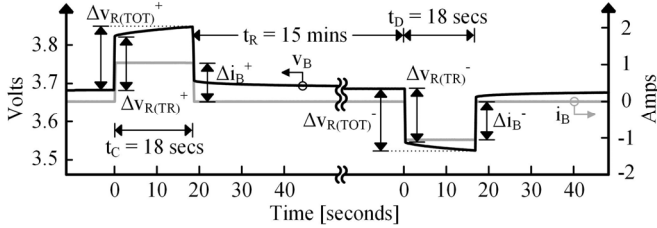**Fig. 10.** Automatic measurement of $R_{B(TR)}$ at (a) 77% SoC, and (b) six SoC's.

Fig. 11. Current pulses to measure $R_{B(TR)}$ and $R_{B(TOT)}$ in both directions.

commonly referred to as the Galvanostatic Intermittent Titration Techniques (GITT) [22, 23].

B. Internal Resistance

Internal resistance R_B is a parameter that depends on temperature, SoC, and cycle life [24]. R_B is a major source of power loss during battery operation and limits the battery's power capability. Therefore, it is necessary to measure R_B to accurately characterize a battery. Several common methods to measure R_B are discussed in this section.

<u>Transient Resistance:</u> The battery's transient resistance $R_{B(TR)}$ is the resistance on the conducting path and can be observed when i_B increases or decreases sharply. One common method to measure $R_{B(TR)}$ is by applying two load currents that simulate the battery's real operating conditions as shown in Fig. 10(a). The test battery is discharged with i_1 during t_1 and i_2 during t_2. $R_{B(TR)}$ is the ratio of the instantaneous voltage change $\Delta v_{R(TR)}$ and current change Δi_B:

$$R_{B(TR)} = \frac{\Delta v_{R(TR)}}{\Delta i_B}. \tag{8}$$

For demonstration, $R_{B(TR)}$ is obtained automatically at six different SoC's as shown in Fig. 10(b). The current step is applied during the interval t_{STEP}. i_1, i_2, t_1, t_2 are chosen to be 1 A, 0.5 A, 2 minutes, and 1 minute, respectively. After each t_{STEP}, the battery is discharged for t_D to a new SoC and rested for t_R (30 minutes). It can be observed that $R_{B(TR)}$ is significantly larger at 5% SoC, which is caused by the depletion of charge carriers. $R_{B(TR)}$ remains stable across the other SoC's.

Hybrid Pulse Power Characterization (HPPC) is another test profile that can be used to obtain $R_{B(TR)}$. As shown in Fig. 11, a charge current pulse of duration t_C is applied to the battery, followed by a period of rest t_R and a discharge current pulse of duration t_D. t_C and t_D are small, so the battery's SoC remains approximately constant. $\Delta v_{R(TR)}$ is the instantaneous voltage rise due to $R_{B(TR)}$. In addition, chemical reactions like charge
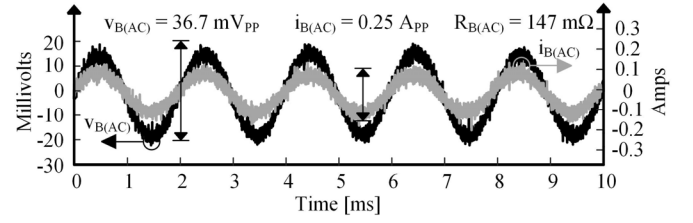
Fig. 12. Sinusoidal excitation to measure $R_{B(AC)}$.
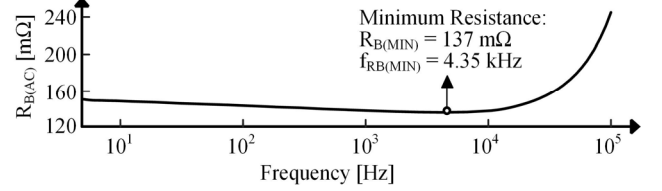
Fig. 13. AC resistance spectrum.

transfer and ionic diffusion in Li ions contribute to the total internal resistance $R_{B(TOT)}$. Assuming change in SoC contributes to negligible v_B rise, $R_{B(TOT)}$ including the effect of chemical reactions [25] can be calculated using the voltage change across the entire pulse $\Delta v_{R(TOT)}$ and the current pulse amplitude Δi_B:

$$R_{B(TOT)} = \frac{\Delta v_{R(TOT)}}{\Delta i_B}. \tag{9}$$

For demonstration, t_C and t_D are chosen to be 18 seconds each with an amplitude of 1 A, and t_R is 15 minutes. The pulses are applied when the battery's SoC is approximately 50%. $R_{B(TR)}$ during charge and discharge are calculated to be 150 mΩ and 152 mΩ. $R_{B(TOT)}$ during charge and discharge are calculated to be 176 mΩ and 175 mΩ.

<u>AC Resistance:</u> The battery's AC resistance $R_{B(AC)}$ can be measured by applying a sinusoidal current of amplitude $i_{B(AC)}$, commonly chosen at 1 kHz, and measuring the corresponding sinusoidal voltage response $v_{B(AC)}$. $i_{B(AC)}$ is chosen so that $v_{B(AC)}$ is less than 20 mV to preserve linearity [26]. Fig. 12 shows $i_{B(AC)}$ generated by the prototype tester and the recorded $v_{B(AC)}$. Using

$$R_{B(AC)} = \frac{v_{B(PP)}}{i_{B(PP)}}, \tag{10}$$

$R_{B(AC)}$ is calculated to be 147 mΩ at 1 kHz, 50% SoC.

$R_{B(AC)}$ can be measured across a frequency range by varying the frequency of the excitation signal. The test battery's $R_{B(AC)}$ is measured from 5 Hz to 100 kHz with 10 points per decade at 50% SoC, and the resulting resistance spectrum is shown in Fig. 13. It can be observed that a minimum resistance $R_{B(AC)}$ occurs at approximately 4.5 kHz. $R_{B(AC)}$ rises sharply at higher frequency due to the wire inductance.

C. Other Tests

Several battery tests that the tester can perform but are not demonstrated due to time or safety concerns are discussed here:

<u>Overdischarge:</u> Overdischarge is a common form of battery abuse and its effects on Li ions include capacity degradation, increased self-discharge, and internal short circuit [16]. To measure the capacity degradation due to overdischarge, the capacity test described previously is performed before and after the battery is discharged below the specified cutoff voltage. The tester's capability to discharge the battery below 0 V allows various degrees of overdischarge to be investigated. The capacity degradation is the change in capacity.
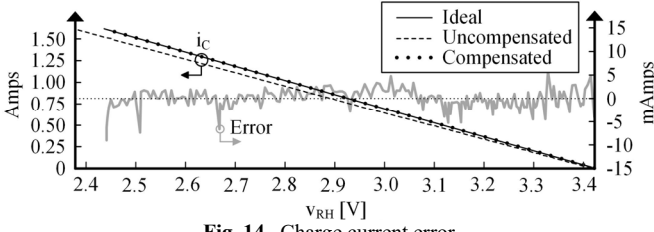
Fig. 14. Charge current error.

Fig. 15. Current loop step response.

Relaxation: A battery's relaxation behavior is often investigated to determine the needed rest time t_R after charge/discharge for the battery to reach equilibrium. To investigate the effect of relaxation, the battery is charged/discharged to the desired SoC, and the current is removed. Different parameters of the battery can then be measured and compared when t_R is varied. For example, [27] investigates the accuracy of SoC estimation using v_{OC} when t_R is changed. [28] compares the accuracy of EIS performed on the battery after different t_R.

Cycle life: Cycle life is defined as the number of charge-discharge cycles a battery can endure before its capacity reduces to a predefined percentage (commonly 80%) of the initial capacity. To perform a cycle life experiment, the test battery is repeatedly charged and discharged with the cycle shown in Fig. 7. The charge current and discharge current can be defined by the user to investigate the effect of current profiles on battery performance [29, 30].

D. Fault Detection

It is important to detect faulty Li-ion batteries to prevent potential hazards. A faulty Li ion typically shows an abnormal decrease in capacity or increase in resistance [2]. The abnormal capacity degradation can be detected by measuring the battery's capacity across multiple full discharges using (5). The internal resistance can be measured by injecting a small sinusoidal current and observing the voltage response. A battery with resistance higher than the typical range can be deemed as faulty.

Models that describe battery behaviors with electrical circuit components can also be used to detect faults [6, 31, 32]. The voltage and current data measured by the tester can be fitted to the battery model to generate estimated values for the battery's inductive, capacitive, and resistive components. Values that lie outside the typical range can indicate the battery as faulty.

IV. PERFORMANCE AND LIMITATIONS

A. Output Current/Voltage Accuracy

The charge/discharge current values are determined by control voltages v_{RH} and v_{RL} when current loop regulates. v_{RH} and v_{RL} are compensated due to the gain and offset error of the system. The compensated control signals are

$$v_{RH} = \alpha_H \left(v_{DD} - i_C R_P \right)\left(\frac{R_{P2}}{R_{P1} + R_{P2}} \right) + \beta_H , \tag{11}$$

$$v_{RL} = -\alpha_L \left(v_{SS} + i_D R_N \right)\left(\frac{R_{N2}}{R_{N1}} \right) + \beta_L , \tag{12}$$

where α_H, β_H are the charger's gain and offset compensation, and α_L, β_L are the discharger's gain and offset compensation. The system is calibrated by sweeping v_{RH} and v_{RL} separately. i_C from the ideal, uncompensated, and compensated signals are shown in Fig. 14. For a standard i_C of 1.625 A and i_D of 3.25 A,
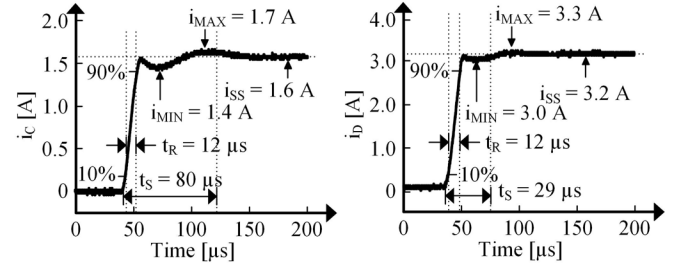
the current error before compensation is 5.9% and 3.1%. After compensation, the error is less than 0.46% for i_C and 0.31% for i_D. To investigate the tester's consistency across cycles, the battery is charged (with constant i_C of 812.5 mA) and discharged for 40 cycles. Measured i_C shows no significant variation from cycle to cycle, and the 3σ limit for i_C across 40 cycles is calculated to be ±1.8 mA.

The output voltage accuracy during CV charge/discharge is degraded by electronic noise, component heating, and the offset and gain error of op amp A_{VP} and A_{VN}. After first-order compensation for the gain and offset error, the output voltage during CV charge at 4.2 V is sampled at 1 kHz and averaged. The worst-case remaining voltage error is measured to be 0.048%.

B. Output Current Rise Time

The tester's maximum output current frequency depends on the rise/fall time of the current, which is affected by the current-loop bandwidth and slew rate. Since the current loop has a wide bandwidth of 10 MHz, the rise time will be mostly limited by slew rate due to the time it takes for A_{GP}/A_{GN} to charge and discharge the gate capacitance of M_P/M_N. Therefore, the worst-case output current frequency limit is for full-swing AC signals. For a 3.3 A_{pk-pk} sinusoidal current with an offset of 1.625 A, the maximum frequency without significant distortion is observed to be approximately 10 kHz.

The step response of the charge/discharge current loops are measured to determine the slew rate of the system as shown in Fig. 15. Excitation v_{RH} and v_{RL} are applied so that i_C and i_D transition from 0 A to 1.63 A and 3.25 A, respectively. The rise time t_R for i_C and i_D measured from 10% to 90% of the steady state current i_{SS} are approximately 12 μs. The 5% settling time t_S for i_C and i_D are 80 μs and 29 μs. The maximum current (i_{MAX}) and minimum current (i_{MIN}) is 1.7 A and 1.4 A when i_C settles, and 3.3 A and 3.2 A when i_D settles. The slew rate is calculated to be 140 mA/μs.

C. Measurement Accuracy

The voltage measurement accuracy is mainly limited by various sources of noise and the components' temperature drift. The PCB components such as resistors, MOSFETs, and amplifiers inject electronic noise to the circuit. The noise voltage at the battery terminal is measured to be 6.2 mV. Accounting for the DMM's error of 0.063%, the worst-case voltage measurement accuracy is 0.31% for a minimum v_B of 2.5 V. The effect of noise is reduced as the voltage is sampled at 1 kHz and averaged. The voltage measurement resolution is limited by the DMM to be 2.5 μV.

Battery current i_B is converted to a voltage with current-sense resistor R_S and measured by the DMM. The current

TABLE II
STATE-OF-THE-ART SINGLE-CELL LI-ION BATTERY TESTERS

	[12]	[13]	[9]	[10]	[11]	This Work
Topology	Linear	Linear	Hybrid	Switched	Switched	Linear
Battery Current Range	5 A	6 A	600/200 A	60 A	0.66 A	3.3 A
Battery Voltage Range	-5-5 V	0-6 V	1.5-4.2 V	1.5-4.5 V	17 V	0-4.2 V
Applied Current Error	0.02%	-	0.04%	1.5%	10%	0.46%
Applied Voltage Error	0.02%	0.015%	-	-	-	0.048%
AC Frequency	-	-	5.0 kHz	2.0 kHz	950 Hz	10 kHz
Slew Rate	17-50 mA/μs	12 mA/μs	7.5 A/μs	-	-	140 mA/μs

measurement accuracy is limited by current noise and the variation of R_S. The chosen R_S has a value of 100 mΩ, tolerance of 1%, and temperature coefficient of 50 ppm/C°. The tolerance error is minimized by measuring R_S with the DMM prior to the experiment. The maximum temperature rise of R_S within the design current range (50 mA to 3.3 A) is 20 C°, resulting in a 0.1% change to the resistance. The current noise is measured to be 50 mA$_{RMS}$, which dominates the current measurement error. The measurements are averaged to reduce the effect of noise.

Battery temperature T_B is obtained by measuring the resistance of a high-accuracy thermistor mounted to the surface of the test battery. Because the battery temperature remains within the range 20 °C to 30 °C throughout the experiments, the worst-case resistance error based on the datasheet is 1.27%, resulting in a temperature measurement error less than 0.38 °C.

D. Limitations

The proposed tester uses linear charger/discharger topology, and its efficiency limits the maximum current supported by the tester. The charger's efficiency is the ratio of the power delivered to the battery and the power drawn from the supply. Considering the dominating power loss from M_P, R_P, and R_S, the theoretical efficiency is calculated to be 54.6-61.5% during a standard charge at 1.625 A. The efficiency variation is due to v_B's variation during charge. The charger's efficiency is measured to be 57.7% when v_B = 3.86 V and i_B = 1.625 A. On the other hand, the discharger's efficiency is not well-defined as the power drawn from the battery is fully dissipated.

The efficiency of the proposed tester and the corresponding power loss limits the maximum charge/discharge current to 3.3 A without overheating the MOSFETs. Several methods to achieve higher battery current include better thermal management, adaptive supply voltage to decrease MOSFET losses [31], and parallel branches of charger/discharger to distribute current stress [9].

E. Comparison with the State of the Art

Table. II summarize the performance of the battery tester proposed in this work and the state of the art (SoA). [9] achieves programmable current by combining the charge current from a DC-DC converter with a current sink consists of 12 parallel linear dischargers. The tester can sink current up to 600 A and source current up to 200 A with a current error of 0.04 %. However, the tester's AC current frequency is limited to 5 kHz and the minimum battery voltage is 1.5 V.

In [10], a battery tester that can output programmable current is implemented by controlling multiple buck converters to generate the AC and DC components of the current separately. The system achieves a peak current of 120 A, but the current

accuracy of the system is limited to 1.5% and the highest AC current frequency is 2 kHz. A similar system with two buck converters is implemented in [11] and a high current error of 10% is observed in the system.

Commercial battery testers in [12, 13] use linear topologies and operate in the similar power range as the proposed testers. [12] displays lower applied voltage and current error than the proposed solution. However, the rise time of the current is higher, which limits the maximum AC current frequency that can be applied to the battery. Similarly, [13] shows a lower applied voltage error, yet its current rise time is much slower. [13] has the same 0 V minimum discharge voltage while [12] can discharge batteries to -5 V.

Because the SoA testers' dimensions are not specified and they operate at different power levels, the considerations for form factors are discussed. Component size and heat management are two main factors that limit the overall solution size. Because heat generation is proportional to power loss, linear testers require more robust heat management systems compared to the more efficient switched testers. On the other hand, switched testers require bulky inductors while linear testers have smaller individual components. The proposed solution has a dimension of 140×241×27 mm^3 without the benchtop instruments. Additional PCB area is given to M_P/M_N and R_P/R_N to lower heating and fit the heat sinks and small fans.

V. CONCLUSIONS

The 12-W battery tester proposed in this paper can automatically perform various common battery tests with a single setup. The tester exhibits excellent stability and a wide battery voltage range. The current loop's 10-MHz bandwidth allows the tester to generate arbitrary charge/discharge current up to 10 kHz, the highest among the state of the art. The generated current is within 0.46% of the desired value during a standard charge/discharge, which is comparable to the existing testers. Additionally, the tester's voltage loop provides reliable battery voltage regulation and seamless CC–CV transition.

Further works include (i) Integration of sensing and charger/discharge circuit to decrease solution size and minimize parasitic capacitances. (ii) Implement adaptive supply voltage [33] to decrease heat dissipation, increase tester efficiency, and increase maximum current level. (iii) Incorporate parallel branches of charger/discharger to accommodate higher current.

REFERENCES

[1] "2021 lithium ion battery market - size, share, COVID impact analysis and forecast to 2027," *Research and Markets*, March 2021.

[2] M. Ouyang *et al.*, "A dynamic capacity degradation model and its applications considering varying load for a large format Li-ion battery," *Applied Energy,* vol. 165, pp. 48-59, March 2016.

[3] A. H. Zimmerman, "Self-discharge losses in lithium-ion cells," *IEEE Aerospace and Electronic Systems,* vol. 19, no. 2, pp. 19-24, 2004.

[4] D. Zhang *et al.*, "Studies on capacity fade of lithium-ion batteries," *Journal of Power Sources,* vol. 91, no. 2, pp. 122-129, Dec. 2001.

[5] J.-S. Kim *et al.*, "Optimization for maximum specific energy density of a lithium-ion battery using progressive quadratic response surface method and design of experiments," *Scientific Reports,* vol. 10, no. 1, p. 15586, Sep. 2020.

[6] D.-I. Stroe *et al.*, "Generalized Characterization Methodology for Performance Modelling of Lithium-Ion Batteries," *Batteries,* vol. 2, no. 4, p. 37, 2016.

[7] A. Bessman *et al.*, "Aging effects of AC harmonics on lithium-ion cells," *Journal of Energy Storage,* vol. 21, pp. 741-749, Feb. 2019.

[8] L. W. Juang *et al.*, "Investigation of the influence of superimposed AC current on lithium-ion battery aging using statistical design of experiments," *Journal of Energy Storage,* vol. 11, pp. 93-103, June 2017.

[9] P. WeBkamp, P. HauBmann, and J. Melbert, "600-A Test System for Aging Analysis of Automotive Li-Ion Cells With High Resolution and Wide Bandwidth," *IEEE Transactions on Instrumentation and Measurement,* vol. 65, no. 7, pp. 1651-60, July 2016.

[10] R. Soares *et al.*, "An Experimental Setup with Alternating Current Capability for Evaluating Large Lithium-Ion Battery Cells," *Batteries,* vol. 4, no. 3, p. 38, 2018.

[11] M. Bayati *et al.*, "Sinusoidal-Ripple Current Control in Battery Charger of Electric Vehicles," *IEEE Transactions on Vehicular Technology,* vol. 69, no. 7, pp. 7201-7210, 2020.

[12] Arbin Instruments, "Laboratory Battery Testing Systems for Cell Applications," LBT21084 datasheet, Sep. 2017.

[13] Chroma Systems Solutions, "Battery Reliability Test System," 17216-6-6 datasheet.

[14] M. Chen and G. A. Rincon-Mora, "Accurate, Compact, and Power-Efficient Li-Ion Battery Charger Circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 53, no. 11, pp. 1180-1184, 2006.

[15] C. Wu *et al.*, "A Review on Fault Mechanism and Diagnosis Approach for Li-Ion Batteries," *Journal of Nanomaterials,* vol. 2015, p. 631263, Oct. 2015.

[16] R. Guo *et al.*, "Mechanism of the entire overdischarge process and overdischarge-induced internal short circuit in lithium-ion batteries," *Scientific Reports,* vol. 6, no. 1, p. 30248, July 2016.

[17] Y. Chen *et al.*, "A review of lithium-ion battery safety concerns: The issues, strategies, and testing standards," *Journal of Energy Chemistry,* vol. 59, pp. 83-99, 2021.

[18] C. Zhang *et al.*, "A Generalized SOC-OCV Model for Lithium-Ion Batteries and the SOC Estimation for LNMCO Battery," *Energies,* vol. 9, no. 11, 2016.

[19] R. Zhang *et al.*, "State of the Art of Lithium-Ion Battery SOC Estimation for Electrical Vehicles," *Energies,* vol. 11, no. 7, 2018.

[20] V. J. Ovejas and A. Cuadras, "Effects of cycling on lithium-ion battery hysteresis and overvoltage," *Scientific Reports,* vol. 9, no. 1, p. 14875, Oct. 2019.

[21] T. Kalogiannis *et al.*, "Incremental Capacity Analysis of a Lithium-Ion Battery Pack for Different Charging Rates," *ECS Transactions,* vol. 77, no. 11, pp. 403-412, July 2017.

[22] A. Nickol *et al.*, "GITT Analysis of Lithium Insertion Cathodes for Determining the Lithium Diffusion Coefficient at Low Temperature: Challenges and Pitfalls," *Journal of The Electrochemical Society,* vol. 167, no. 9, p. 090546, June 2020.

[23] W. Weppner and R. A. Huggins, "Determination of the Kinetic Parameters of Mixed-Conducting Electrodes and Application to the System Li3Sb," *Journal of The Electrochemical Society,* vol. 124, no. 10, pp. 1569-1578, Oct. 1977.

[24] H.-G. Schweiger *et al.*, "Comparison of several methods for determining the internal resistance of lithium ion cells," *Sensors (Basel),* vol. 10, no. 6, pp. 5604-5625, 2010.

[25] A. Barai *et al.*, "A study of the influence of measurement timescale on internal resistance characterisation methodologies for lithium-ion cells," *Scientific Reports,* vol. 8, no. 1, p. 21, Jan. 2018.

[26] N. Lohmann *et al.*, "Electrochemical impedance spectroscopy for lithium-ion cells: Test equipment and procedures for aging and fast characterization in time and frequency domain," *Journal of Power Sources,* vol. 273, pp. 613-623, 2015.

[27] M. Messing, T. Shoa, and S. Habibi, "Lithium-Ion Battery Relaxation Effects," in *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, pp. 1-6, June 2019.

[28] A. Barai *et al.*, "A study on the impact of lithium-ion cell relaxation on electrochemical impedance spectroscopy," *Journal of Power Sources,* vol. 280, pp. 74-80, April 2015.

[29] M. J. Smith, D. T. Gladwin, and D. A. Stone, "Experimental analysis of the influence of high-frequency ripple currents on dynamic charge acceptance in lead-acid batteries," in *IECON*, pp. 7140-7145, Oct. 2017.

[30] K. Uddin *et al.*, "The effects of high frequency current ripple on electric vehicle battery performance," *Applied Energy,* vol. 178, pp. 142-154, 2016.

[31] C. Cheng *et al.*, "Extraction of Intrinsic Parameters of Lead-Acid Batteries Using Energy Recycling Technique," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4765-4779, May 2019.

[32] C. Cheng *et al.*, "Time-Domain Modeling of Constant Phase Elements for Simulation of Lithium Battery Behavior," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7573-7587, Aug. 2019.

[33] P. Liu and L. Chien, "A High-Efficiency Integrated Multimode Battery Charger With an Adaptive Supply Voltage Control Scheme," *IEEE Transactions on Power Electronics,* vol. 33, no. 8, pp. 6869-6876, 2018.

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