Small Saturating Inductors for More Compact Switching Power Supplies

Luke Milner* Non-member
Gabriel A. Rincón-Mora* Non-member

Abstract: Other than by reducing power, extending battery life in portable microelectronics amounts to increasing power efficiency, which when coupled with accuracy, translates to increasing filter inductance. The problem with higher inductances is magnetic cores require more space to prevent the onset of saturation, so accuracy and efficiency (via their need for bulky inductors) hamper the miniaturization benefits gained from chip integration. This paper illustrates the time-domain and efficiency effects of inductor saturation in switched-inductor dc-dc converters and shows how they can accommodate saturation (with up to 65% reduction in inductance) with minimal impact on battery life and accuracy. Extending the useful range of an inductor in this fashion not only reduces PCB area and volume to a fraction (e.g., 30–50%) of what an otherwise larger unsaturated inductor would require but also helps bridge the integration gap that enables practical system-on-chip (SoC) implementations.

Keywords : Inductors, Saturation, Switching Supplies, DC-DC Converters

1. Small Switched-Inductor Power Supplies

Switching supply circuits often demand more space than many emerging portable applications have available. Foregoing the supply circuit, however, is not an option because boosting or bucking a source voltage is typically a basic necessity, especially when (*i*) drawing energy from high-energy but low-voltage sources like miniaturized fuel cells (1)–(3) and solar cells (4)–(5) and (*ii*) supplying energy-saving, dynamically adaptive systems (6)–(7). One challenge with building an efficient and accurate supply circuit, within the context of volume, is the need for large inductors because they transfer energy with minimal power losses and suppress voltage ripples in the output. Even in micropower systems, these components often double or triple the area and volume of the circuit (8)–(9). The fact that many state-of-the-art subsystems cannot tolerate the variance or voltage level of a single, common supply exacerbates the problem because several point-of-load (PoL) supply circuits (and their inductors) require even more space (10)–(11).

This paper proposes and verifies experimentally that switching supplies can accommodate smaller inductors by allowing their cores to saturate and therefore extending their useful power range while still requiring little space. By conforming switching converters into smaller spaces, emerging miniaturized platforms can now benefit from the high conversion efficiencies (i.e., extended battery-life performance) of switched-inductor circuits. Since small supplies facilitate integration, more converters can also fit into one unit, allowing a system to reap the efficiency and performance advantages of point-of-load regulation. Because the extent and consequences of inductor saturation in switching converters were unclear in prior literature, many state-of-the-art designs do not enjoy such improvements in battery life and regulation performance, limiting advances in biomedical implants, wireless microsensors, and other tiny applications. For those reasons, Sections II and III first describe how inductors saturate and why power-supply designers avoid saturation and Sections IV and V then illustrate and verify the actual time-domain and efficiency effects of saturation in switching power supplies. Section VI evaluates the results obtained and Section VII draws relevant conclusions.

2. Inductor Saturation

A switching dc-dc converter, be it an inverting or non-inverting buck, boost, or buck-boost circuit, transfers energy from an input source V_{IN} to a load (i.e., an output v_O) by energizing (from V_{IN}) and de-energizing (to v_O) an inductor L_O in alternate phases, as Fig. 1a generally depicts. More specifically, a constant energizing voltage V_E across L_O energizes L_O, increasing its current i_L (where i_L is $L_O dv_L/dt$) and flux λ_L. Reversing the voltage across L_O in the form of de-energizing voltage V_{DE} releases L_O's energy and causes i_L and λ_L to decrease, but not along the initial energizing path, as Fig. 1b shows.

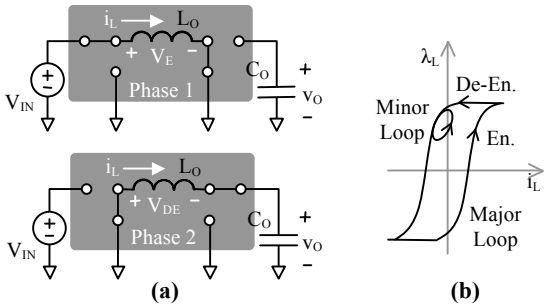

Fig. 1. (a) Energizing and de-energizing inductor L_O (b) means flux increases and decreases along L_O's hysteresis loop.

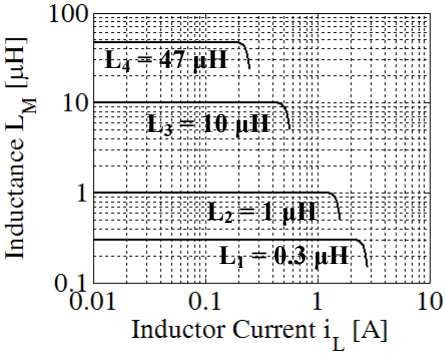

Fig. 2. Typical inductance-saturation graph (17).

As L_O repeatedly energizes and de-energizes, i_L and λ_L traverse along a hysteresis loop, which means L_O releases less energy than it stored in its energizing cycle (where the area in the loop represents the energy lost in the core (12)–(13)). (Note L_O also loses power across the equivalent series resistance ESR of the copper coil.) Beyond a threshold current, the flux in the core begins to saturate, causing the range of i_L (i.e., ripple current Δi_L) and the hysteresis loop to expand (13)–(16), which is to say both L_O's Δi_L and core losses increase. Another way to describe this

* Georgia Tech Analog, Power, & Energy IC Lab
777 Atlantic Drive NW, Atlanta, GA, USA 30332

effect is through inductance because the increase in Δi_L is equivalent to a decrease in L_O. Datasheets, for example, illustrate that inductance decreases at higher currents (17), as Fig. 2 shows, albeit with little insight into the actual time-domain operation and power-efficiency effects of saturation.

3. Power-Loss Argument

Switched-inductor circuits are ideally lossless because the power switches experience nearly negligible voltage (and therefore power) drops and L_O and C_O introduce next to no series resistances in the power path. In practice, however, the feedback controller draws quiescent current from the supply, the drivers lose energy in charging and discharging the parasitic gate capacitance of the switches, and L_O's average and ripple currents $i_{L(avg)}$ and Δi_L dissipate Ohmic conduction losses P_C across the finite resistances that the switches, L_O, and C_O actually present:

$$P_C = R_{EQ1} i_{L(avg)}^{\ 2} + R_{EQ2}\left(\frac{\Delta i_L^{\ 2}}{12}\right), \qquad (1)$$

where R_{EQ1} and R_{EQ2} are the combined stray resistances L_O, C_O, and the power switches introduce in $i_{L(avg)}$'s path through L_O and Δi_L's path into C_O, respectively, and $\Delta i_L^{\ 2}/12$ is the root-mean-squared (RMS) value of i_L's ripple, which is triangular in nature (18). When considering the high efficiency objectives of the supply and the reduction of energy delivered to the output that saturating L_O causes, limiting the sum of these losses is important. As a result, because magnetic core losses and Δi_L (and its derivative losses across R_{EQ2} in P_C) increase when L_O saturates, designers typically select the core's cross-sectional area and volume to be large enough to sustain (without saturating) the flux associated with the highest expected i_L. They further oversize L_O to offset the fact that the saturation characteristics in datasheets are absent or poorly specified. The underlying aim of this paper is to show that such design practices are overly cautious, which is to say designs can survive the saturating effects of smaller inductors and, in consequence, reap the benefits of higher integration.

4. Actual Saturated Response

Representative Circuit: Because all dc-dc converters energize and de-energize inductors in the same way: by applying quasi-constant positive and negative voltages across a power inductor in alternating cycles across a switching period (19)-(23), the power inductor of all switching dc-dc converters similarly conduct dc and triangular ripple currents $i_{L(avg)}$ and Δi_L. Therefore, the buck converter in Fig. 3 (and Fig. 4a), just like any other switching dc-dc supply, is a good means of verifying and demonstrating how i_L in switched-inductor circuits generally responds to saturating conditions. The only differentiating factor between these switching circuits, from the perspective of i_L, is the magnitude of energizing and de-energizing voltages V_E and V_{DE}. In the buck case, L_O (from Fig. 4b) energizes from V_{IN} to v_O with PMOS power switch M_P so V_E equals $V_{IN} - v_O$, and de-energizes to v_O from ground with NMOS power switch M_N so V_{DE} is $-v_O$. As in all switching converters, in addition to L_O and its connecting switches M_P and M_N, the supply circuit also includes output capacitor C_O, drivers, and a feedback controller, the last two of which (and in some cases, also M_P and M_N) are often embedded in a common integrated circuit (IC).

Time-Domain Response: With respect to inductor saturation and power efficiency, what is important is i_L's dc and ripple currents $i_{L(avg)}$ and Δi_L, in other words, i_L's steady-state time-domain waveform. From this perspective, the dynamics of the control loop (e.g., feedback amplifier, etc.) are irrelevant. As a result, to decouple the effects of the controller from L_O's saturation effects on $i_{L(avg)}$ and Δi_L, the foregoing discussion and measurements assume a pulse-width modulated (PWM) square-wave signal v_{PWM} is available and ready to drive L_O's energizing and de-energizing switches in the power stage. That is to say, a function generator defines and sources the control signal in Fig. 3 (v_{PWM}) that the dead-time block uses to produce the non-overlapping gate voltages that drive M_P and M_N.

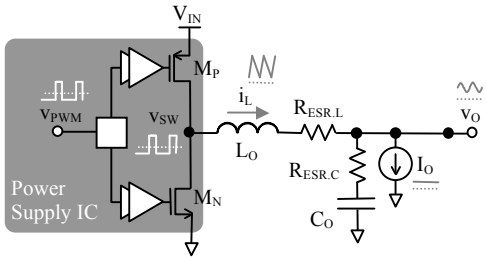

Fig. 3. Switching buck dc-dc converter.

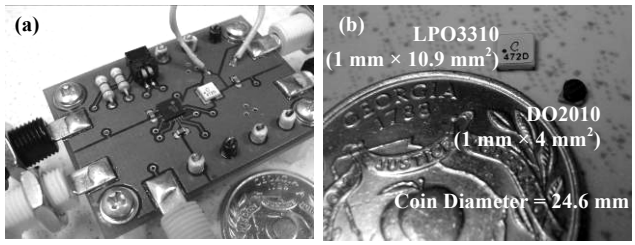

Fig. 4. (a) Switching converter printed circuit board (PCB) built to test (b) inductors LPO3310 and DO2010.

Because the circuit impresses time-invariant energizing and de-energizing voltages V_E and V_{DE} across L_O, instantaneous inductance L_M determines i_L's rising and falling slopes, that is, di_L^{+}/dt is V_E/L_M and di_L^{-}/dt is V_{DE}/L_M. As such, the effects of saturation manifest as changes in i_L's slope across time (24). Fig. 5, for example, illustrates that the rising and falling slopes of i_L in the buck converter of Fig. 3 are constant as long as i_L remains below 2 A. Once above this threshold, L_O saturates and both rising and falling slopes increase, the degree of which L_O's effective inductance determines. Measuring this instantaneous inductance L_M amounts to sampling i_L (via a Hall-effect probe, for example) and its slope across time (with an oscilloscope). Fig. 5 therefore demonstrates that L_M is constant when the core is unsaturated and decreases with increasing i_L only when L_M saturates, when i_L surpasses 2 A in this case. In practical terms, as graphically shown, saturation increases current ripple Δi_L.

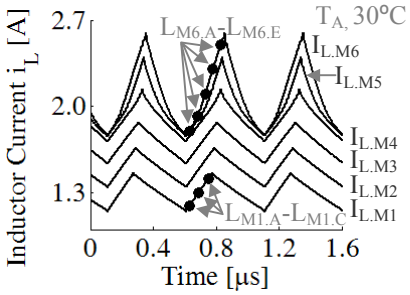

Fig. 5. Experimental inductor-current waveforms as a 1-µH inductor saturates.

Inductance Variation: By repeatedly calculating inductance at several points on each waveform for increasing values of average inductor current $i_{L(avg)}$ at various ambient temperatures, Fig. 6 maps (from experimental measurements) how L_M changes across instantaneous and average i_L values and temperature. These results show that L_M decreases from a nominal non-saturated value (L_{NS})

of 1.1 µH to a *constant* and lower saturated value (L_S) of 0.35 µH when the core saturates, which represents a 65% reduction in L_M. The bimodal piecewise linear response of i_L's rising and falling slopes in the saturated waveforms of Fig. 5 graphically corroborate that L_M drops to a constant (L_S). L_M does not decrease below L_S because saturating the magnetic core is equivalent to replacing it with an air core the inductance of which is roughly 0.35 µH. Fig. 6, however, further reveals that the onset of saturation decreases with $i_{L(avg)}$, which previously reported literature did not show (24)–(27). Increasing temperature (from 30 to 90 °C, for example) also has similar effects on the onset of saturation; that is, higher temperatures induce a lower saturation threshold (14). The last two effects are not mutually exclusive, though, because higher $i_{L(avg)}$ increases the power lost in L_M as heat, so temperature also rises with $i_{L(avg)}$. Nevertheless, the result is the same: the onset of saturation decreases with higher $i_{L(avg)}$ and higher ambient temperatures.

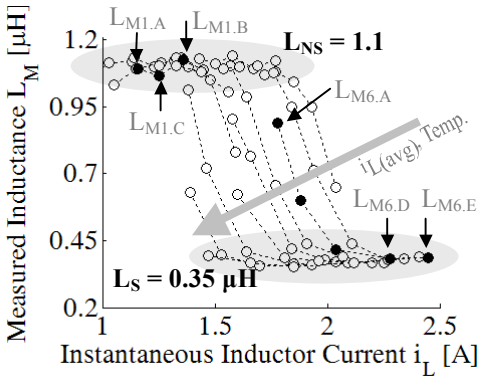

Fig. 6. Measured (and overlapped) inductances across current and temperature (at 30, 60, and 90 ºC).

5. Power Efficiency in Saturation

The effect of saturation on efficiency is noticeable but often tolerable. To start, conduction losses P_C increase with increasing current ripple Δi_L, but this only happens when $i_{L(avg)}$ (i.e., output current I_O) is sufficiently high to induce saturation, and even then, Δi_L only increases by a factor of 3, given the 65% reduction in L_O when the core saturates. Consider that P_C (according to Eq. 1) is 771 mW when R_{EQ} is 300 mΩ, $R_{ESR.C}$ is 50 mΩ, $i_{L(avg)}$ is 1.6 A, and Δi_L is 350 mA, and tripling Δi_L, as saturation would, increases P_C by 2.7% to 792 mW.

As stated earlier, core losses also increase with saturation, and this loss is the difference between L_O's stored and delivered energy in the alternating cycles of the converter. The area (A_{HYS}) enclosed by the minor λ_L-i_L hysteresis loop that i_L creates in Fig. 1 (as i_L rises and falls each cycle) represents this loss (13), (28), which means small hysteresis loops indicate low core losses. Fig. 7 extracts this λ_L-i_L information from Fig. 5 by extrapolating and integrating inductor voltage v_L from the measured data (13), (29)–(30), where v_L is the difference between energizing (or de-energizing) voltage V_E (or V_{DE}) and the voltage across L_O's ESR, which is $i_L R_{ESR.L}$ (because Faraday's Law dictates that v_L represents the rate of change of magnetic flux-linkage through the inductor's core). Therefore, accounting for the resistive voltage drop and integrating the remaining voltage is a way to calculate the flux that is plotted in Fig. 7.) Multiplying the energy loss by the converter's switching frequency f_{SW} yields inductor-core power loss $P_{L.CORE}$:

$$P_{L.CORE} = f_{SW} \oint i_L \mathrm{d}\lambda_L = f_{SW} A_{HYS} . \qquad (2)$$

Experimental results in Fig. 7 show that the minor λ_L-i_L hysteresis loop first shifts up and to the right with increasing $i_{L(avg)}$ (because λ_L and i_L increase) and then distorts and widens with $i_{L(avg)}$ past saturation (as core losses and Δi_L increase), which (31) corroborates. Before the core saturates, since $P_{L.CORE}$ (calculated by integrating the closed contours of Fig. 7) remains constant and P_C rises with $i_{L(avg)}$, the percentage of $P_{L.CORE}$ in the total power lost in L_O (P_L) decreases with $i_{L(avg)}$ from 24%, in this case, to 13% when $i_{L(avg)}$ increases from 1.3 to 1.7 A. (Note P_L is the average of the product of i_L and v_L, which is also the sum of conduction losses $R_{ESR.L} i_L^2$ and $P_{L.CORE}$). In saturation, $P_{L.CORE}$ increases from 63 to 158 mW, and from 13% of P_L back to 23%. In effect, saturation negates the decreasing impact of the core on efficiency as $i_{L(avg)}$ increases, but only to a similar extent that decreasing $i_{L(avg)}$ does when not saturated, which means saturation is not necessarily detrimental to the converter's efficiency performance.

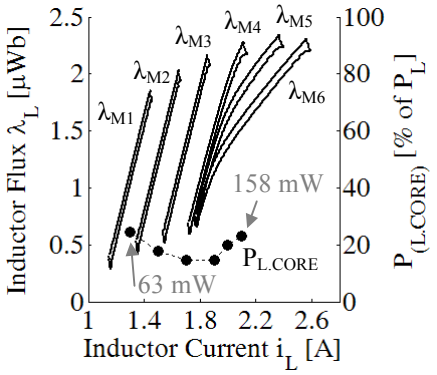

Fig. 7. Flux-current loops and resulting impact of core losses.

In the end, core saturation degrades efficiency, although only to a certain extent, and because current ripple Δi_L increases, output voltage ripple Δv_O also increases, which means saturation also degrades converter accuracy. The converter remains functional in saturation, however, efficiently regulating v_O in spite of slow and sudden changes in line voltage and load. Efficiency and accuracy are therefore legitimate trade-offs for volume, especially since the propensity for large currents and saturation in portable applications is low.

6. Discussion

Ultimately, the benefit of reducing inductance is smaller volume. The inductor used in the above experiments, for instance, which was a 3.3 × 3.3 × 1.0 mm^3 (10.9 mm^3) LPO3310 with a ferrite core (similar to the on-package inductor used in (32)), a nominal inductance of 1.0 µH, and a nominal saturation limit of 1.6 A, was still effective past its saturation point to 2.1 A. The actual (practical) limit, which exceeds 2.1 A, is when the inductor overheats, which depends on several factors like printed-circuit-board (PCB) layout, inductor package, and duration of large loads. For reference, consider that among inductors that do not saturate at 2 A, the smallest (as inferred from (17)) is 20% larger at 12.4 mm^3, despite its smaller footprint. Similarly, a DO2010 behaves like an LPO3310 up to at least 2 A, and the smallest inductor with a 2-A rating (ME3215) requires twice the area and more than 3 times the volume; in other words, a DO2010 yields 50% and 67% drop in area and volume, respectively. This reduction is of paramount importance because the inductor typically dominates the area and volume of most converter circuits (8)–(9), (32). Of course, these savings, as Table 1 summarizes, vary with manufacturer and technology, and the inductors considered here for proof of concept may not be optimal for a given application.

Table 1. Comparison of Inductor Size and Performance

	LPO3310	DO2010	ME3215
L_O	1.0 µH	1.0 µH	1.0 µH
R_{DC}	76 mΩ	200 mΩ	58 mΩ
Area	10.9 mm^2	4.0 mm^2	8.0 mm^2
Volume	10.9 mm^3	4.0 mm^3	12.0 mm^3
I_{RATED}	1.6 A	1.8 A	*2.3 A*
$I_{EXP.}$*	*2.1 A*	*2.1 A*	

While high efficiency is desirable at all load levels, efficiency at light-to-moderate loads in portable applications is vital and more important than at peak loads. Wireless CDMA handsets, for instance, normally idle at low-to-moderate power levels and consume peak power only a fraction of the time, which is why their peak-to-average-power ratios (PAPR) are high (33). In other words, idling consumes most of the energy stored in the battery so light- (not peak-) load efficiency ultimately determines operational life (34). Many wireless microsensor applications exhibit even larger PAPRs because data collection and transmission is less frequent. What all this means is that trading some peak-power efficiency for reductions in PCB real estate (by using smaller inductors) is justifiable and optimal for many portable applications.

Saturation also degrades converter accuracy because a higher inductor ripple current Δi_L induces a larger ripple voltage across C_O (Δv_O), increasing the systematic noise content in the output of the converter. In the presented converter, because switching frequency f_{SW} was constant at 2 MHz, saturation tripled Δi_L, inducing Δv_O to increase by a corresponding percentage (e.g. from 3.2mV to 8.5mV when C_O and $R_{ESR.C}$ are 10µF and 20mΩ, respectively). While this degradation in accuracy is important, it may not be as critical in systems where linear, low-dropout regulators buffer (and filter) the converter to supply power to sensitive analog blocks (18), reducing the ripple by 30–40 dB. In the case converter accuracy is nonetheless important, modifying the loop's control strategy to regulate i_L's ripple Δi_L by modulating f_{SW}, as in hysteretic converters whose response to load dumps is substantially faster than competing schemes (35), circumvents this accuracy degradation, albeit at the expense of a slightly variable f_{SW}.

7. Conclusions

This paper demonstrates that a 3.3 × 3.3 × 1.0-mm^3 (10.9-mm^3) ferrite-core 1.0-µH inductor rated for 1.6 A operates well in switching dc-dc converters past its saturation point to 2.1 A, and that saturating inductors can reduce PCB area and space by 50% and 67%, respectively, over competing alternatives, while increasing total peak-power conduction losses by 2.7% from 771 to 792 mW. Experimental results further show that inductance decreases from 1 µH to no less than 0.35 µH, and that the onset of saturation decreases with higher average currents and ambient temperatures, which previous studies did not show. While a few percentage-points increase in peak-power efficiency is appreciable, its impact on battery life can be, for the most part, negligible in mobile devices because they tend to idle most of the time, which means light- (not peak-) load efficiency is critical. The point is that using a smaller inductor may save as much real estate as the converter IC (itself) requires, and the savings multiply in point-of-load (PoL) architectures where several inductors may be necessary. Freeing space in this way might even enable subsystems to adopt dynamic scaling schemes (6)–(7), which increase power efficiency when and where it matters most. The benefits of extending the operational limits of an inductor are even more prominent in system-on-chip (SoC) solutions because using above-the-die (in-package) magnetic cores, which exhibit low saturation thresholds, eliminates the PCB real estate that off-chip inductors would otherwise demand.

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Luke Milner (Non-member) received a B.S. and an M.S.E.E in 2004

and 2006, respectively, from Georgia Tech, where he is currently pursuing a Ph.D. as a graduate research assistant in the Georgia Tech Analog, Power, & Energy IC Lab. In 2005, he worked in the Power Technology Group at NSC in Santa Clara, CA, and his research continues to focus on integrated dc-dc converters for portable electronics.

Gabriel A. Rincón-Mora (Non-member) (B.S., M.S., Ph.D., IET

Fellow) worked for Texas Instruments in '94-'03, was appointed Adjunct Professor for Georgia Tech in '99-'01, and became a full-time faculty member at Georgia Tech in '01. His scholarly products include 8 books, 1 book chapter, over 125 scientific publications, 27 patents, over 26 commercial power management chip designs, and over 55 international speaking engagements. He received the "National Hispanic in Technology Award," "Charles E. Perry Visionary Award," a "Commendation Certificate" from the Lieutenant Governor of California, IEEE CASS Service Award, and Robins Air Force Base's "Orgullo Hispano" and "Hispanic Heritage" awards. He was inducted into Georgia Tech's "Council of Outstanding Young Engineering Alumni," elected IEEE CASS Distinguished Lecturer for '09-'10, and featured on the cover of Hispanic Business magazine as one of "The 100 Most Influential Hispanics." He has been Associate Editor for IEEE's TCAS II for '08-'11; Editorial Board Member for JOLPE since 2009; Chairman of Atlanta's IEEE SSCS-CASS Chapter since 2005; is Technical Committee Member for IEEE's CASS ASP and PECAS; Steering Committee Member for IEEE's MWSCAS; was General Chair for SRC's Energy and Power ICs Workshop in '09; Circuit Design Vice Chair for IEEE's '08 ICCDCS; Technical Program Chair for IEEE's '07 MWSCAS-NEWCAS; Technical Program Co-Chair for IEEE's '06 MWSCAS; Vice Chairman of Atlanta's SSCS-CASS Chapter in '04; and SBIR Selection Committee Review Panelist for NSF in '03-'07.