
Optimized Frequency Shaping Circuit Topologies for LDOs

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Abstract

Typical low drop-out (LDO) regulator architectures suffer from an inherent load regulation performance limitation. This limitation manifests itself through limited dc open-loop gain and results from stringent closed-loop bandwidth requirements. The frequency response of the system is highly sensitive to the loading conditions thereby making proper compensation a laborious endeavor. This paper discusses and addresses the limitation on regulating performance imposed by frequency compensation.

Several LDO circuit topologies are subsequently developed to this end. They enhance load regulation performance by relaxing the dc open-loop gain restrictions. The circuit structures essentially alter the frequency response of the system via the error amplifier. A low drop-out regulator adopting an embodiment of the proposed technique was fabricated in the MOSIS 2 μm process technology. The system, designed for an output capacitor of 4.7 μF, was stable with an equivalent series resistance (ESR) ranging from 0 to 12 Ω, bypass capacitors adding from 0 to 2.2 μF, and a load-current ranging from 0 to 50 mA.

I. Introduction

The motivation behind the study of low drop-out (LDO) regulators is driven by the growing demand for higher performance power supply circuits. An increasing number of low voltage applications require the use of LDOs, i.e., cellular phones, pagers, laptops, camera recorders, etc. [1]. Such a low voltage environment demands that LDOs meet stringent specifications. However, loading conditions and stability requirements limit the dc open-loop gain and consequently load regulation performance. This translates to restricted overall accuracy and/or more rigorous requirements on the other specification parameters of the regulator. Mitigating this restriction is especially important for portable battery operated products, a growing market demand sector. These applications require low voltage operation as well as low quiescent current flow to maximize the efficiency and the longevity of single low voltage battery cells [2]. Simultaneously, the demands on regulators become more strict because of consequential reductions in dynamic range [3, 4]. Low voltage and low quiescent current flow operation, unfortunately, tend to degrade the overall performance of power supply circuits. As a result, accuracy is adversely affected thereby requiring improvement.

Figure 1 illustrates the basic components of a linear regulator and its associated load. The regulator is composed of an error amplifier, a pass element, and feedback resistors. The load of the system is comprised of an output load-current and associated output impedance, an output capacitor

and associated equivalent series resistance (ESR), and bypass capacitors. The variable nature of the load makes frequency compensation a difficult task. This results because ESR varies (from one capacitor to the next) as well as load-current and bypass capacitors. The ESR of the bypass capacitors is typically neglected because they are usually high frequency capacitors; in other words, they have low ESR values [5]. The pass device is modeled as a circuit element exhibiting a transconductance of g_{mp} and an output resistance of $R_{o\text{-}pass}$. The dashed line denoted by "A" is an electrical short during normal operation. However, it is an open circuit for the purpose of ac analysis.

II. Frequency Response

The open-loop system of Figure 1 must be unity gain stable, considering V_{ref} and V_{fb} to be the input and the output voltages respectively (open circuit at "A"). The open-loop frequency response of the system is characterized by three poles and one zero, a potentially unstable system. For the majority of the load-current range, the poles and the zero can be approximated to be the following:

$$P_1 \approx 1/2\pi R_{o-pass}C_o \approx \frac{\lambda I_L}{2\pi C_o}, \quad (1)$$

$$P_2 \approx 1/2\pi R_{esr}C_b, \quad (2)$$

$$P_3 \approx 1/2\pi R_{oa}C_{par}, \quad (3)$$

and

$$Z_1 \approx 1/2\pi R_{esr}C_o, \quad (4)$$

where I_L is the load-current and λ refers to the channel length modulation parameter of a PMOS pass device (the reciprocal of the early voltage (V_A) similarly applies to a PNP transistor). Figure 2 illustrates the typical frequency response of the system assuming that the output capacitor (C_o) is larger

than the bypass capacitors (C_b). Unfortunately, the response varies with load-current by affecting P_1, with ESR by affecting Z_1 and P_2, and with bypass capacitors by further affecting P_2, as intimated by equations (1) - (4).

III. Load Regulation Performance Limit

Load regulation performance (output resistance of the regulator, R_o) is a function of the open-loop gain (A_{ol}) of the system and can be expressed as

$$R_o = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \qquad (5)$$

where ΔV_{LDR} is the output voltage variation arising from a load-current variation of ΔI_o, $R_{o\text{-}pass}$ is the output resistance of the pass device, and β is the feedback factor. Resistors R_1 and R_2 have been neglected, as done for equation (2), because for most of the current range $R_{o\text{-}pass}$ is significantly smaller. This results because (1) load-current is in the mA range and (2) the pass device has a minimum channel length (necessary to decrease turn-on resistance and increase output current capability) thereby degrading λ. The regulator yields better load regulation performance as the open-loop gain increases [6]. However, the gain is limited by the closed-loop bandwidth of the system and the open-loop unity gain frequency (UGF). The gain-bandwidth product (GBW) is not constant for this system. As a result, the UGF is not a function of GBW but a function of gain, P_1, Z_1, and P_2. The minimum UGF is bounded by the response time required by the system during transient load-current variations [5]. Furthermore, the UGF is also bounded at the high frequency end by the parasitic poles of the system, i.e., the internal poles of the amplifier and pole P_3. For instance, if the UGF is at 1 MHz and the parasitic poles are assumed to be located at higher frequencies, then the gain at 1.0 kHz has to be less than approximately 40 - 45 dB when Z_1 and P_2 are located at 10 and 100 kHz respectively, as shown in Figure 2. Moving the parasitic poles to higher frequencies is difficult because of the low quiescent

current flow restriction (arising from battery operated products) and because of the inherently large size of the pass device (necessary for high output current capabilities). UGF and load regulation are further constrained as a result. In conclusion, open-loop gain is restricted by the stringent specifications of the UGF and the frequency response implications of the load. Simulations verified the above described limitations.

IV. Enhancement

4.1 Pole/Zero Pair Generation

The dc open-loop gain of the system can be augmented, however, by adding a pole/zero pair as shown in Figure 3. For a given unity gain frequency (UGF), the upper limit of the open-loop gain can be increased by manipulating the frequency response as depicted by trace B of the Figure. The basic idea is for the gain to drop quickly as the frequency increases so that a larger dc gain is possible. Hence, regulation is improved while keeping the UGF away from parasitic poles. The placement of the extra pole and zero must take into account that P_1, P_2, and Z_1 are functions of the output capacitance, the equivalent series resistance (ESR) of the output capacitor, and the load-current. However, the fact that P_2 and Z_1 track each other (both are inversely proportional to R_{esr}) can be used to optimize the design. It is further noted that the phase shift must be kept below 180 ° at frequencies equal to and lower than the UGF to maintain stability, as dictated by Nyquist criterion [7]. Simulations confirmed the aforementioned properties of the system with the implementation of the additional pole/zero pair.

The design location of the additional pole and zero depends on the gain of the system and the variability of Z_1 and P_2. The achievement of maximum gain comes at the expense of restricted ESR range. This range is important for its variation is dependent on the type of capacitor and the fabrication process. Typically, relatively inexpensive capacitors exhibit the worst ESR variation. Given a constant UGF, maximum gain occurs when P_x and Z_x are maximally displaced from each other in frequency. This is because the drop in gain per decade of frequency in mid-band is larger when P_x is at lower

frequencies and Z_x is at higher frequencies. Thus, maximum gain can be achieved efficiently if Z_1 and P_2 are guaranteed to be between P_x and Z_x throughout their entire range. For this to be true, the ESR must be greater than some finite non-zero number. However, Z_1 and P_2 tend to infinity as the ESR is allowed to approach zero. Consequently, the frequency differential between P_x and Z_x is limited by the phase requirements of the system, less than 180° phase shift. If the ESR is bounded by a finite lower limit guaranteeing Z_x to be greater than Z_1, then the phase minimum is defined by P_x and Z_1 (otherwise defined by P_x and Z_x).

The intrinsic transient response parameter of the system is the overshoot resulting from a transient load-current step. This, in turn, is mainly limited by the output capacitor, the load-current change, the closed-loop bandwidth, and the slew-rate associated with the gate of the power PMOS. Settling time is not as important as maximum overshoot for overall accuracy is not affected. Settling time could only become an issue when considering noise injection as a result of a sudden load-current change.

4.2 Circuit Realizations

The adjusted circuit architecture needs to provide a new function, namely, adding a pole/zero pair in the frequency response of the open-loop system. One way to achieve this goal is to actually incorporate it into the frequency response of the error amplifier by way of active components. In essence, the amplifier serves to shape the frequency behavior of the system as well as provide gain. The amplifier alone is not necessarily required to be stable. This is because the second pole of the amplifier is required to be at the parasitic frequency realm of the system; thus, phase-margin for the amplifier alone is not required to meet conventional stability requirements.

Parallel Amplifier Structure: One method of integrating the pole/zero pair response into the amplifier is to have dual amplifiers connected in parallel as shown in Figure 4. One amplifier has high gain and whose bandwidth determines the location of P_x while the other has lower gain (whose magnitude determines the location of Z_x) and higher bandwidth. The output impedance of both

amplifiers need to be relatively low for proper operation. The main concept revolves around feed-forwarding the ac signal through a bypass path constituted by the amplifier with lower gain. The transfer function of both amplifiers and the resulting response of the system are shown in Figure 4 (b). The gain-bandwidth product of the high gain amplifier can be utilized to determine the necessary gain of the other amplifier to introduce Z_x at the desired frequency, as shown by the following relation,

$$GBW_1 = \frac{A_1}{2\pi P_x} = \frac{A_2}{2\pi Z_x} \quad \text{or} \quad \frac{A_1}{A_2} = \frac{P_x}{Z_x}, \tag{6}$$

where A_1 and A_2 correspond to the gain of amplifier one and two respectively while GBW_1 corresponds to the gain-bandwidth product of amplifier one. It is observed that the bandwidth of the second amplifier constitutes a parasitic pole in the overall system. Furthermore, the frequency where P_x resides is dependent on the dominant pole of amplifier one, which is subject to process variations. However, the ratio of P_x and Z_x exhibits less variation since it is mainly determined by component matching issues, if designed carefully. The main disadvantage of the circuit is complexity. Consequently, the realization of the two amplifiers may prove to be costly in terms of quiescent current flow. This results from more current sensitive transistor paths to ground because there are two amplifiers. Figure 5 shows the simulation results of a macro-model circuit implementing the parallel amplifier structure. There is roughly a 17 dB improvement in the dc open-loop gain of the system with the additional pole/zero pair for a given unity gain frequency (UGF). Load regulation performance improved from 41 to 12 mV / 100 mA, corresponding to a 71 % reduction. Since the dc open-loop gain is itself linearly dependent on $R_{o\text{-}pass}$, load regulation is independent of $R_{o\text{-}pass}$,

$$\Delta V_{LDR} \equiv I_L R_o \approx I_L \frac{R_{o-pass}}{A_1 g_{mp} R_{o-pass}} = \frac{I_L}{A_1 g_{mp}}, \tag{7}$$

where ΔV_{LDR} is the variation in voltage due to the output current and g_{mp} is the transconductance of the pass device.

Frequency Shaping Amplifier: A pole/zero pair can also be generated through the use of a feed-forward capacitor in a folded topology as shown in Figure 6 (a). At low frequencies, the amplifier is unaffected by the feed-forward capacitor (C_{ff}). Thus, the gain is that of a typical folded topology, which is characteristically high. At high frequencies, the capacitor acts like an electrical short giving rise to the gain of a non-cascoded architecture (lower gain). The corresponding small signal model of the circuit is represented in Figure 6 (b). The gain of the amplifier (A_v) is described by

$$A_v \approx g_{m1} R_o = g_{m1}[R_{Load} || R_x] \approx g_{m1} R_x, \tag{8}$$

where g_{m1} is the transconductance of Mp1, R_{Load} is the output resistance of the mirror load, and R_x is

$$R_x = \frac{r_{ds3}[1+g_{m3}r_{ds2}]}{1+sr_{ds3}C_{ff}} + r_{ds2} = \frac{\left\langle s + \frac{r_{ds2}+r_{ds3}[1+g_{m3}r_{ds2}]}{r_{ds3}r_{ds2}C_{ff}} \right\rangle r_{ds2}}{s+\frac{1}{r_{ds3}C_{ff}}}, \tag{9}$$

where g_{m3} is the transconductance of Mn3 and r_{ds2} (r_{ds3}) is the output resistance of transistor Mn2 (Mn3). Consequently, the locations of the pole and the zero are

$$Z_x \approx \frac{g_{m3}}{2\pi C_{ff}} \tag{10}$$

and

$$P_x \approx \frac{1}{2\pi r_{ds3} C_{ff}}. \tag{11}$$

The cascoding element's transconductance (g_{m3}) needs to be small, which implies the use of MOS devices instead of bipolar transistors in a biCMOS environment. Figure 7 illustrates the simulated frequency response of an LDO using the error amplifier architecture of Figure 6 (a). It is noted that the dc open-loop gain is a function of load-current because the open-loop output resistance of the regulator is dominated by the early voltage of the power PMOS transistor. As a result, the output resistance of the pass device is larger ($R_{o\text{-}pass} \propto 1 / I_{Load}$) and therefore the gain is higher at lower output currents.

The frequency shaping amplifier can also take a couple of other forms within the same folded architecture, as is illustrated by the different loading structures in Figure 8. A variation of the feed-forward concept is embodied in the circuit of Figure 8 (a). Small signal analysis shows that the pole and the zero locations for this structure are described by

$$Z_x \approx \frac{1}{2\pi RC_{ff}} \tag{12}$$

and

$$P_x \approx \frac{1}{2\pi[R + r_{o3}]C_{ff}}, \tag{13}$$

where r_{o3} is the output resistance of Qn3. Yet another realization of the pole/zero pair is illustrated in Figure 8 (b). This circuit takes advantage of the input and the output impedance of the mirror load, composed of Mp4 and Mp5, to help shape and define the frequency response of the amplifier. The corresponding pole and zero locations are described by

$$Z_x = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}}\right\rangle C} \tag{14}$$

and

$$P_x = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}} + r_{ds4}\right\rangle C}, \qquad (15)$$

where g_{m5} is the transconductance of Mp5 and r_{ds4} is the output resistance of Mp4. Simulations of the frequency response produced results that closely resemble those illustrated in Figures 5 and 7.

The frequency response of these amplifiers introduces a single parasitic pole to the overall system. This parasitic pole is formed by the loading capacitor of the amplifier and $(1/g_{mp5} + R)$ for Figure 8 (b). The pole has moved up in frequency as a result of adding the pole/zero pair. Its former location was defined by the output resistance of MP4, which has a larger value than $(1/g_{mp5} + R)$. The new location of the pole may be at lower frequencies, however, if the amplifier drives the gate of the large power PMOS transistor directly, i.e., the pass device in the linear regulator structure.. The severity of this problem can be alleviated by buffering the output of the amplifier and thus isolating the large capacitive load from the amplifier. In essence, the large capacitive load is moved to a low impedance point. The effects of process variations on performance manifest themselves through deviations in transconductance and transistor output impedance, which in turn define the locations of the pole and the zero as well as the parasitic pole.

A low drop-out regulator using the frequency shaping amplifier was fabricated in MOSIS 2 μm CMOS process with a p-base layer. The circuit is illustrated in Figure 9. The topology uses a single stage low voltage amplifier with the pole/zero generation structure of Figure 8 (b). The load of the differential pair is a level shifted current mirror. A current efficient buffer is used to isolate the high gate capacitance of the power PMOS device (Mpo) from the gain stage. The operation of this buffer is described in detail in [8]. The corresponding frequency response is shown in Figure 10. The ac performance follows the behavior predicted by analysis; in other words, the gain drops at rates of either 20 or 40 dB per decade of frequency (for frequencies higher than the dominant pole) while maintaining phase margin. In particular, stability was maintained for various combinations of bypass capacitors (0.1

to 2.2 μF), equivalent series resistance ($0 < ESR \leq 12\ \Omega$), and load-current (0 to 50 mA). As a result of these various loading conditions, the frequency response experiences a medley of different curves that fall within the parameters specified by the complex system of poles and zeros analyzed.

V. Conclusion

Enhancing regulator performance is especially important when considering that the demand for mobile battery operated products is increasing. Such applications entail low voltage and low quiescent current flow characteristics. As a result, specifications become more stringent in a reduced dynamic range environment while, unfortunately, maintaining innate circuit performance limitations [9]. This paper discusses one major limitation to accuracy, in particular, load regulation. This arises because of the frequency response requirements of the closed-loop bandwidth and the unity gain frequency. The bandwidth is constrained by the transient requirements and the unity gain frequency is further restricted by the location of the parasitic poles of the system. As a result, open-loop gain and therefore load regulation performance is limited. The paper develops circuit topologies to improve this performance parameter. The resulting circuits are also appropriate for a low voltage environment. The advantages and characteristics of these structures were verified through circuit analysis and simulations. The system implementing the pole/zero pair simulated to have an improvement in dc open-loop gain of approximately 17 dB and a load regulation performance improvement of roughly 71 %. A prototype circuit was fabricated and the behavior of the frequency response exhibited the characteristics described by analysis. The circuit was stable for a variety of loading conditions.

References

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Figure Captions

Figure 1. System model under loading conditions.

Figure 2. LDO frequency response under loading conditions.

Figure 3. System's frequency response with an additional pole/zero pair.

Figure 4. Parallel amplifier pole/zero pair realization.

Figure 5. Simulation of the LDO implementing the parallel amplifier structure.

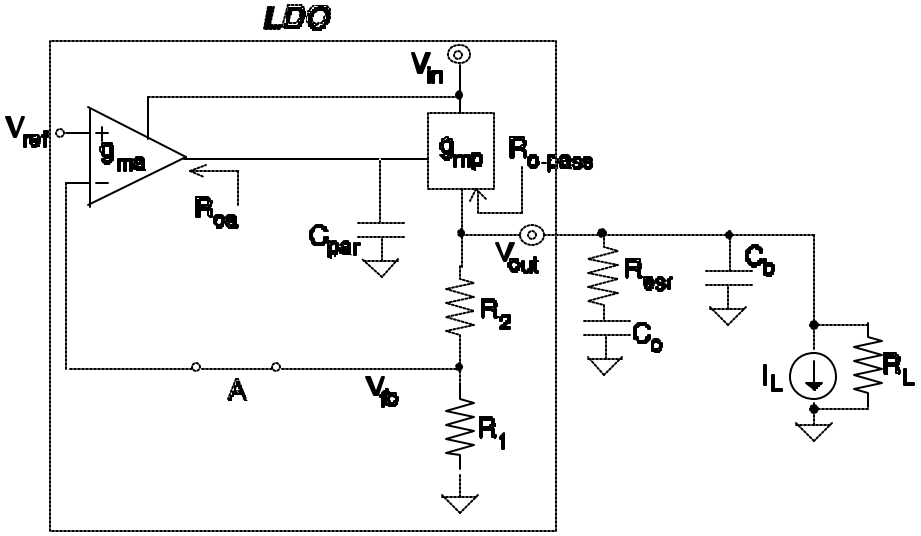
Figure 6. Pole/zero pair generation by a feed-forward capacitor.

Figure 7. Simulation of the LDO implementing the feed-forward capacitor structure.

Figure 8. Variations of the frequency shaping amplifier.

Figure 9. Prototype low drop-out regulator using the frequency shaping amplifier.

Figure 10. Frequency response of the prototype circuit.



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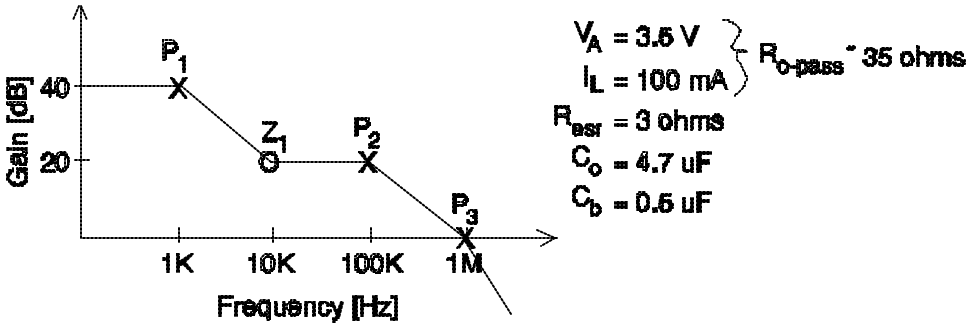


Figure 2. LDO frequency response under loading conditions.

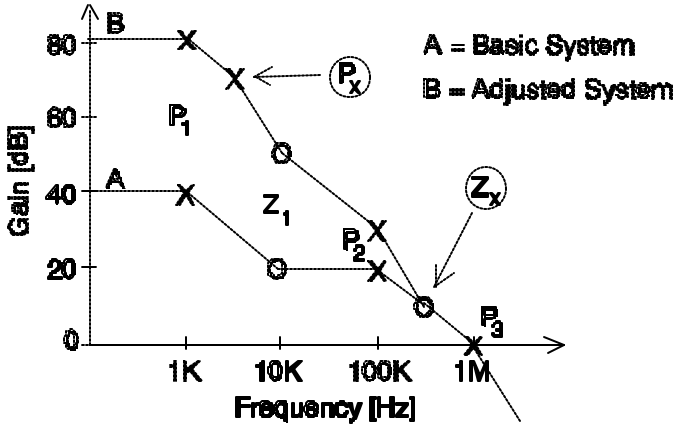


Figure 3. System's frequency response with an additional pole/zero pair.

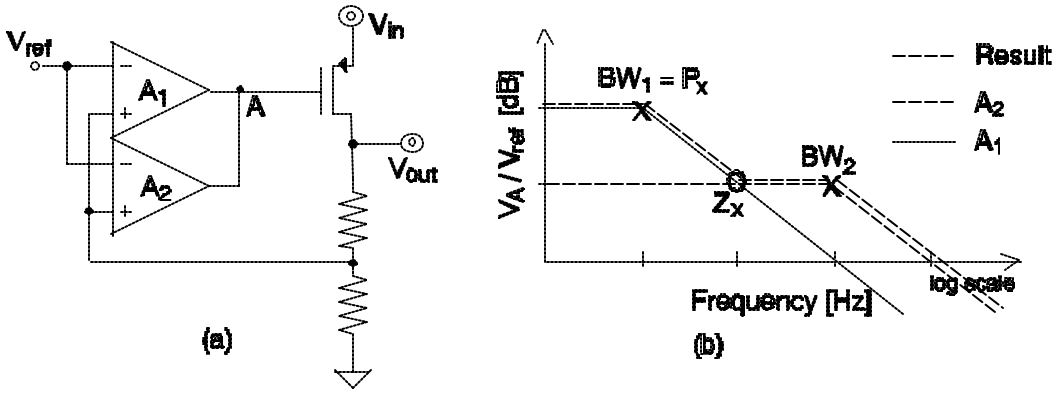


Figure 4. Parallel amplifier pole/zero pair realization.

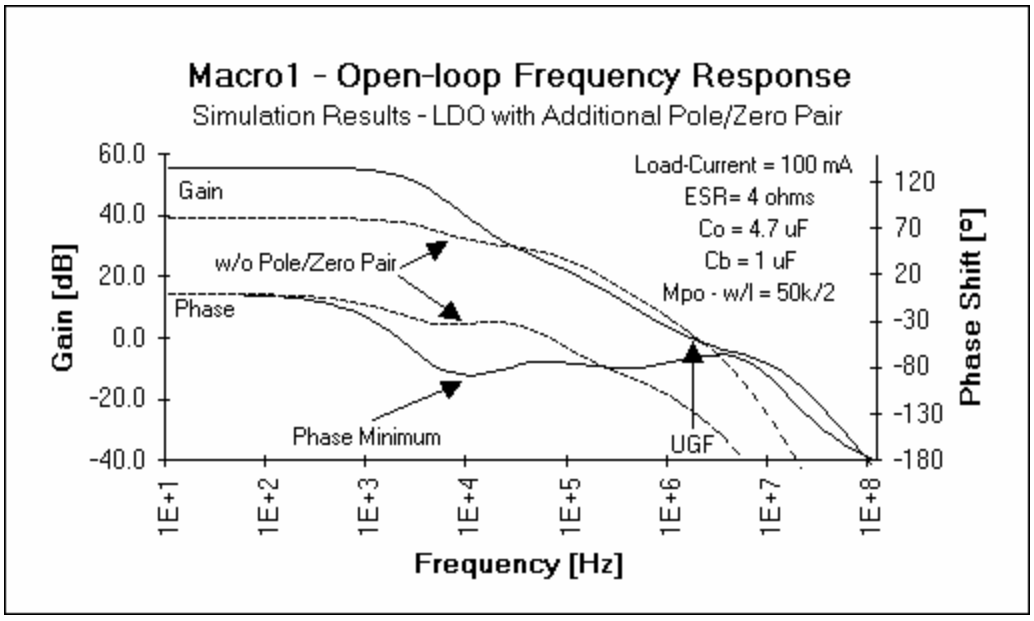


Figure 5. Simulation of the LDO implementing the parallel amplifier structure.

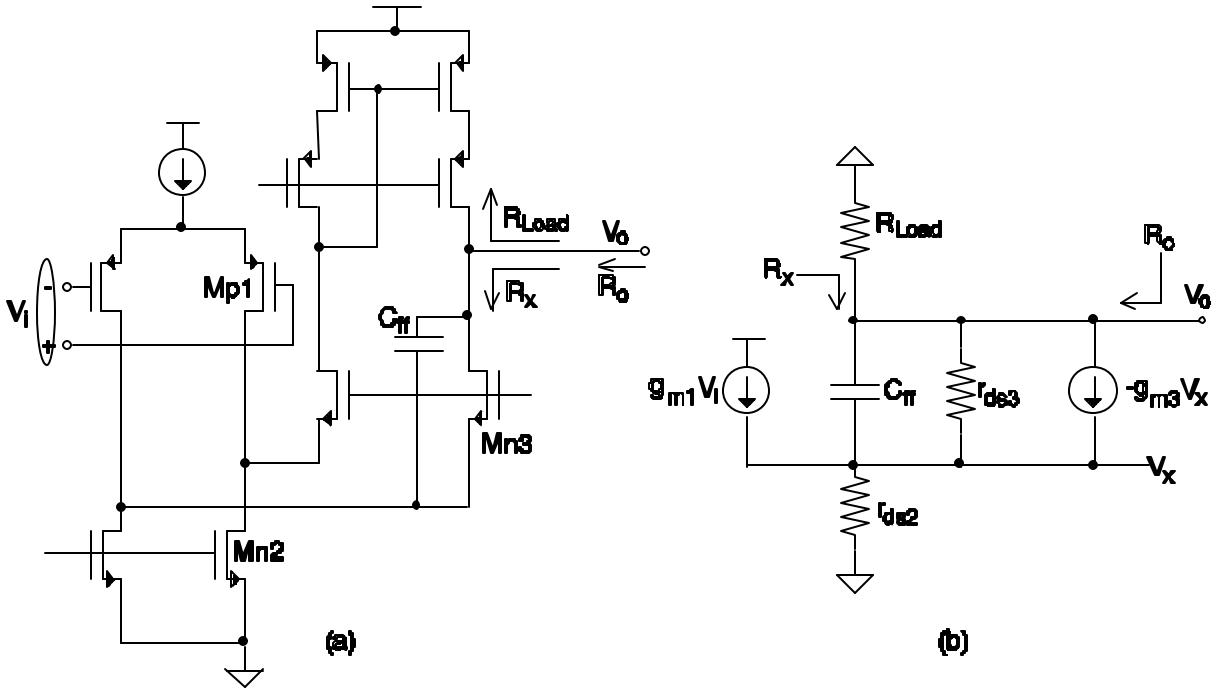


Figure 6. Pole/zero pair generation by a feed-forward capacitor.

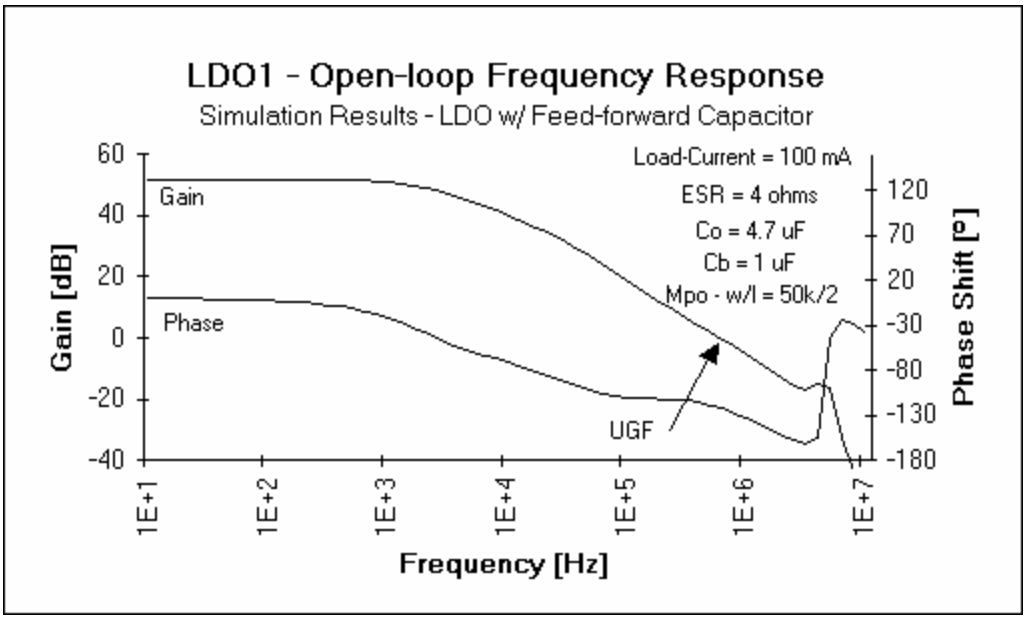
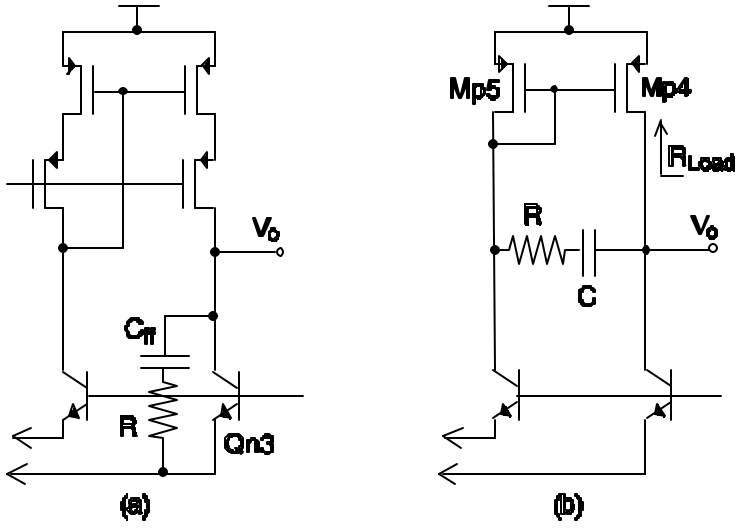


Figure 7. Simulation of the LDO implementing the feed-forward capacitor structure.



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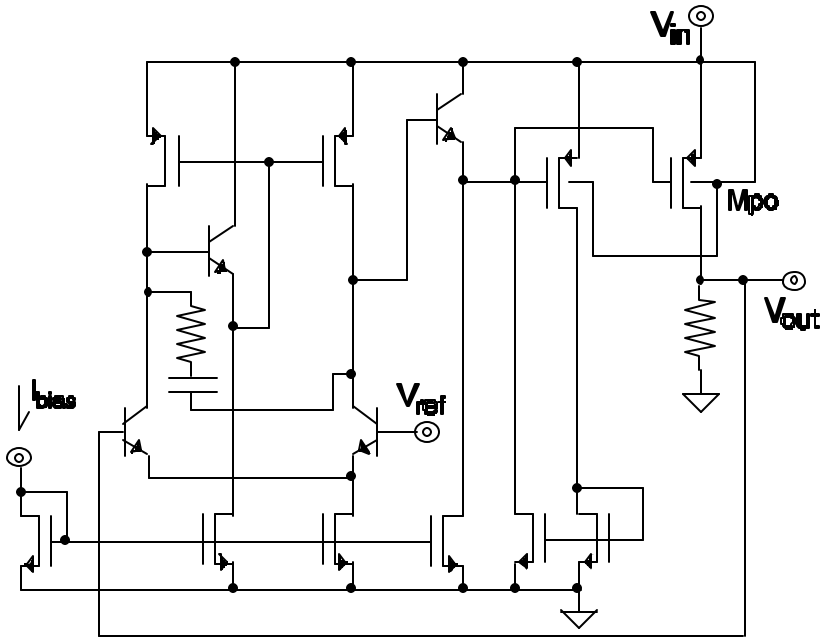

Figure 9. Prototype low drop-out regulator using the frequency shaping amplifier.

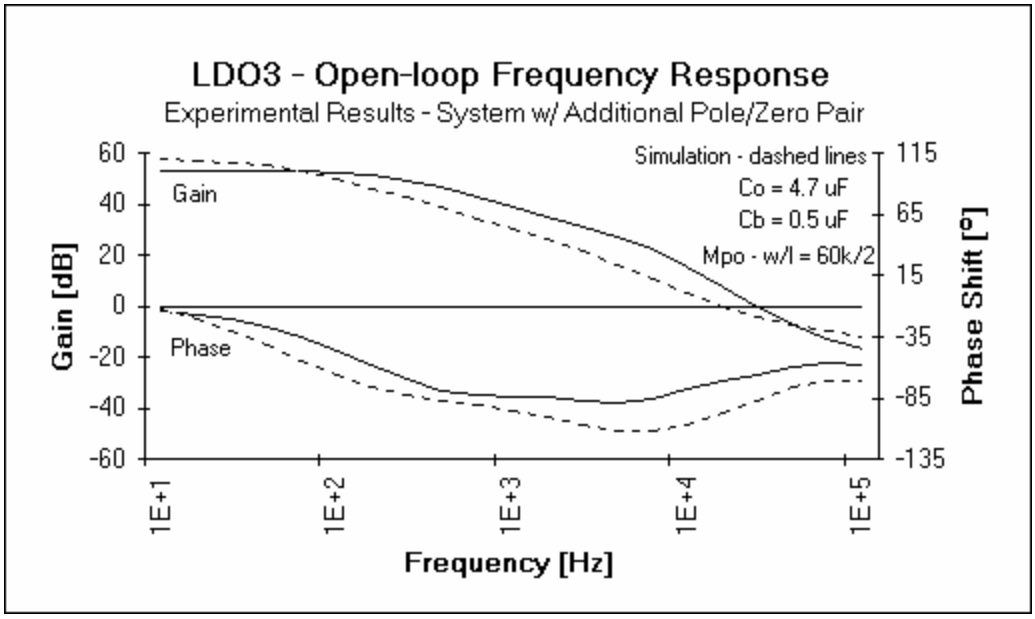

Figure 10. Frequency response of the prototype circuit.