Design of Switched-Inductor Charging Regulator for Resistive On-Chip Thermoelectric Generators

Tianyu Chang, *Graduate Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Fellow, IEEE*

***Abstract*—On-chip thermoelectric generators (TEGs), unlike bulky off-chip TEGs, are easy to integrate and tiny. A CMOS switched-inductor charging regulator (SLCR) both harvests TEG power & draws battery power to supply Internet-of-Things (IoT) wireless microsensors. However, on-chip TEGs output millivolts, carry MΩ source resistance R_S, and produce nW power, which demand SLCR to boost low voltage, manage leakage, & maintain high efficiency. Design of such CMOS SLCR power stage often needs prolonged exhaustive tweaking & trial-and-error process. To tackle these challenges, this brief proposes a fundamental theory on the design of nW CMOS SLCR for low-voltage high-R_S applications. With closed-form equations, this theory predicts the optimal power switch, optimal inductor, and optimal current profile, such that SLCR can harvest from the lowest voltage with highest efficiency. This brief provides experimental results with a 180-nm CMOS SLCR power stage prototype. With the theory, an optimal CMOS SLCR power stage can be designed with closed-form equations, without extensive trial-and-error efforts.**

Keywords*—Switched inductor, CMOS, low-voltage, low-power, power supply, charger, thermoelectric generator, energy harvesting.

I. Emerging TEG-Sourced Microsystems

Thermoelectric generators (TEG) can supply tiny IoT wireless microsensors. TEGs are modelled as a dc source voltage v_S & a source resistance R_S as in Fig. 1 [1]. TEG outputs maximum power P_{MPP} if its terminal voltage v_{IN} equals Maximum Power Point (MPP) voltage v_{MPP}, which is half v_S [1–2]. Based on whether P_{MPP} is more or less than load power P_O, Switched-Inductor Charging Regulator (SLCR) in Fig. 1 delivers excess P_{MPP} to battery v_B or draws power P_B from v_B to supply P_O [3–4]. Operation & design theory of the SLCR are in Section II.

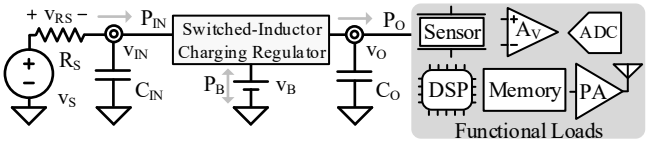

Fig. 1. On-chip TEG powered battery-assisted IoT microsystem.

Since IoT microsensors are in millimeter scale [5], off-chip TEGs' bulky sizes (9–42 cm^2) is a bottleneck for reducing overall system volume. Also, off-chip TEGs are fabricated with BiTe or PbTe, which are difficult to integrate with semiconductor processes [6–9]. On-chip TEGs are made of Si, poly-Si, or poly-SiGe using CMOS, BiCMOS, or CMOS-MEMS. This shrinks the size of on-chip TEGs to 3–70 mm^2, which is 12–1400× smaller than off-chip TEGs [10–13].

However, on-chip TEG's R_S is much higher and can reach 0.7–1.3 MΩ, while the R_S of off-chip TEGs can be 0.16–4 Ω [6–13]. High R_S limits on-chip TEGs' P_{MPP} to 1.8–17 nW/°C^2, this is 3300–220000× less than that of off-chip TEGs. For an on-chip TEG co-integrated with a nearby IC System-on-Chip (SoC), the SoC may generate an on-chip temperature gradient ΔT of 1–8 °C [14–15], which provides ΔT for the nearby on-chip TEG. So, this paper targets v_S & P_{MPP} generated by less than 8 °C ΔT, which is feasible on chip. With 8 °C ΔT & a typical 1-MΩ R_S, v_S & P_{MPP} are less than 500 mV & 62.5 nW. Table I compares on-chip & off-chip TEGs in detail.

Table I: Comparison of On-Chip and Off-Chip TEGs

Material	Size	On Chip	v_S	R_S	P_{MPP}	Ref.
Bi-Te	29 × 29 mm^2	OFF	30 mV/°C	4.0 Ω	56 μW/°C^2	[6]
Bi-Sb-Te	63 × 63 mm^2	OFF	15 mV/°C	160 mΩ	350 μW/°C^2	[7]
Bi-Te	61 × 71 mm^2	OFF	40 mV/°C	1.0 Ω	400 μW/°C^2	[8]
PbTe-BiTe	56 × 56 mm^2	OFF	28 mV/°C	970 mΩ	210 μW/°C^2	[9]
Poly-Si	3 × 3 mm^2	ON	160 mV/°C	1.3 MΩ	4.9 nW/°C^2	[10]
Poly-Si	3 × 1 mm^2	ON	150 mV/°C	700 kΩ	8.0 nW/°C^2	[11]
Si	11 × 1.5 mm^2	ON	250 mV/°C	900 kΩ	17 nW/°C^2	[12]
Poly-SiGe	14 × 5 mm^2	ON	74 mV/°C	760 kΩ	1.8 nW/°C^2	[13]

On-chip TEGs pose strict challenges. First, leakage of the SLCR must be below nW. Second, SLCR must harvest energy from millivolt v_{IN}. Third, efficiency must be high at nW level.

A theory that guides the design of all variables so an SLCR can harvest from low v_{IN} & high R_S with the highest efficiency is missing in [16–20]. This leads to prolonged trial-and-error design, & the design may not be optimal after extensive effort.

To address this, this brief presents a fundamental theory on the design of nW CMOS SLCR for low-v_{IN} high-R_S TEGs to achieve the highest efficiency possible. Key contributions are:

1) Closed-Form Design Theory: this brief provides in-depth loss analysis & closed-form formulae that determine the highest-efficiency design of every design variable (i.e., CMOS switches, inductor L_X, & peak L_X current $i_{L(PK)}$).
2) Experimental Results: this brief shows experimental results with a 180-nm CMOS prototype, which can harvest from 25-mV input voltage and its peak nW-efficiency is 77%.

Sections II & III derive the theory & show measured data. Sections IV & V compare performance & draw conclusions.

II. Low-v_{IN} High-R_S CMOS Design

A. Charging Regulator

CMOS SLCR schematic is shown in Fig. 2. With nW P_{MPP}, SLCR is in Discontinuous Conduction Mode (DCM). An idle IoT sensor may need as low as 11-nW P_O from about 1-V v_O [3]. If P_{MPP} exceeds P_O, the SLCR is in over-sourced mode. In

The authors are with School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, U.S.A. E-mail: tchang78@gatech.edu, rincon-mora@gatech.edu. The work is supported by Texas Instruments.

this mode, M_S is closed. If v_O demands power, M_{G2} & M_{O2} boosts v_{IN} to v_O. Otherwise, M_{G2} & M_B boosts v_{IN} to v_B. Inductor current i_L is shown in Fig. 3. E_{SO} & E_{SB} are energy packets delivered to v_O & v_B. t_{ES} & t_S are L_X's energize time & switching period. t_{DO} & t_{DB} are L_X's drain time to v_O & v_B.

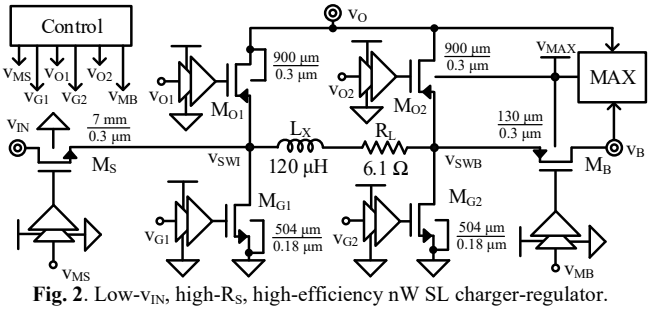

Fig. 2. Low-v_{IN}, high-R_S, high-efficiency nW SL charger-regulator.

IoT sensors may need 1-mW P_O when transmitting [20]. If P_O exceeds P_{MPP}, the SLCR is in under-sourced mode. M_S & M_{O2} are open if SLCR sends energy from v_B to v_O. M_B, M_{G2}, M_{G1}, & M_{O1} bucks or boosts v_B to v_O. i_L in this mode is shown in Fig. 4. E_B are energy packets from v_B that supply the extra power v_O needs. t_{EB} & t_{DB} are L_X's energize & drain time when drawing power from v_B. Power transferred from v_S or v_B to v_O is $P_{O(S)}$ or $P_{O(B)}$. $P_{O(S)}$ plus $P_{O(B)}$ equals the total load power P_O.

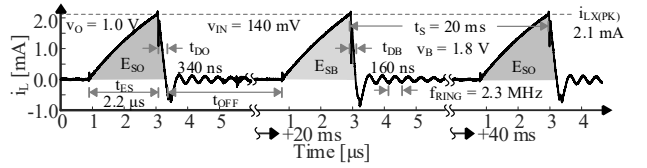

Fig. 3. Measured over-sourced i_L profile.

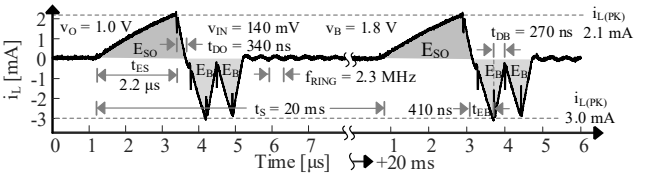

Fig. 4. Measured under-sourced i_L profile.

Fixed Energy Packet: this brief aims at design theory but not control. But for completeness, this sub-section outlines the control of the SLCR. Detailed controller design is in [4].

Controller like [4] (in Fig. 5) implements the "fixed energy packet" scheme. Main purposes of this scheme are: (1) Draw energy packets E_{SO}, E_{SB}, & E_B of their respective fixed sizes; (2) MPP tracker like in [17] sets v_{MPP}. CP_{MPP} sets how often energy packets are drawn from v_S such that v_{IN} is nearing v_{MPP}, which happens with a particular t_S; (3) CP_O regulates v_O within a hysteretic window around v_{REF}. If $P_{MPP} > P_O$, v_O rises until CP_O trips high and then SLCR releases energy to v_B; (4) CP_M sets operation mode; (5) $CP_{ZCD(B)}$ & $CP_{ZCD(O)}$ are Zero-Current Detection comparators for correct DCM operation.

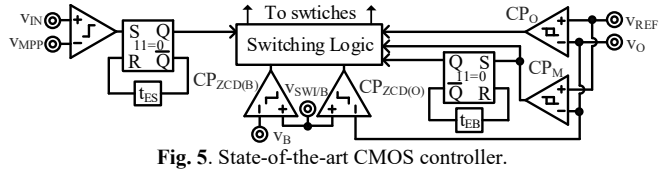

Fig. 5. State-of-the-art CMOS controller.

Importance of fixing energy packets is: maximizing DCM efficiency means minimizing fractional loss of each individual packets since the packets are identical. This section derives the optimal switches, L_X, & $i_{L(PK)}$ at nW so energy packets are the least-lossy. Section IV.A shows the effect of controller power.

B. Least-Lossy Switches

MOS switches' resistances R_{MOS} & gate capacitances C_G incur ohmic & charge losses P_{MR} & P_{MC}. P_{MR} is inverse-proportional to MOS width W_{MOS}, and P_{MC} is proportional to W_{MOS} [21]:

$$P_{M(R)} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 R_{MOS}\left(\frac{t_{E/D}}{t_{SW}}\right) \equiv \frac{k_{M(R)}}{W_{MOS}}, \quad (1)$$

$$P_{M(C)} = C_G v_{GD}^2 f_{SW} = (C_G'' L_{MIN} W_{MOS}) v_{GD}^2 f_{SW} \equiv k_{M(C)} W_{MOS}, \quad (2)$$

where $t_{E/D}$ is L_X's energize/drain time, t_{SW} & f_{SW} are switching period & frequency, C_G'' is C_G per unit area, L_{MIN} is minimum channel length, v_{GD} is gate-drive voltage, and $k_{M(R)}$ & $k_{M(C)}$ are coefficients that lumps every term except W_{MOS}.

Since P_{MPP} is nW, MOS switches' sub-threshold leakage $P_{M(L)}$ is noticeable. MOS switches leak across off-time t_{OFF} as Fig. 3 shows. With nW P_{MPP}, SLCR draws infrequent energy packets, so t_{OFF} is almost t_{SW}. So, $P_{M(L)}$ is inverse-proportional to MOS leakage resistance $R_{M(L)}$. Since $R_{M(L)}$ is also inverse-proportional to W_{MOS}, $P_{M(L)}$ is proportional to W_{MOS} as in (3):

$$P_{M(L)} = \left(\frac{v_{LK}^2}{R_{M(L)}}\right)\left(\frac{t_{OFF}}{t_{SW}}\right) \approx \frac{v_{LK}^2}{R_{M(L)}} \equiv k_{M(L)} W_{MOS}, \quad (3)$$

where v_{LK} is the voltage across a switch in off-state, and $k_{M(L)}$ is the coefficient. To manage $P_{M(L)}$ & reduce the total loss of MOS switches, the optimal W_{MOS} (denoted as W_{MOS}') balances leakage $P_{M(L)}$ and $P_{M(C)}$ with $P_{M(R)}$. W_{MOS}' is expressed as:

$$W_{MOS}' = \sqrt{\frac{k_{M(R)}}{k_{M(C)} + k_{M(L)}}}. \quad (4)$$

M_B exemplifies this trade off in Fig. 6. M_B's optimal width W_B' balances the rising $P_{M(C)}$ & $P_{M(L)}$ with the falling $P_{M(R)}$, & lowest total loss is 20 pW. All switches are optimally designed in the same way and their widths are in Fig. 2. Lowest MOS loss P_M (denoted as P_M') occurs if $P_{M(R)}$ equals $P_{M(C)}$ plus $P_{M(L)}$:

$$P_M' = P_{M(R)}' + P_{M(C)}' + P_{M(L)}' = 2P_{M(R)}' = 2\sqrt{k_{M(R)}(k_{M(C)} + k_{M(L)})}, \quad (5)$$

where $P_{M(R)}$', $P_{M(C)}$', and $P_{M(L)}$' are the MOS ohmic, charge, and leakage losses with optimal width W_{MOS}'.

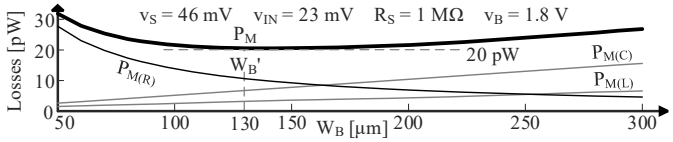

Fig. 6. Simulated ohmic, charge, leakage losses of MOS power switch M_B.

C. Least-Lossy Inductor & Peak Current

Inductor: Theory on optimizing L_X is absent in [16–20, 22]. Tiny IoT sensors limit L_X's size to millimeters. For a given volume, L_X's ESR R_L is about proportional to L_X, as in Fig. 7.

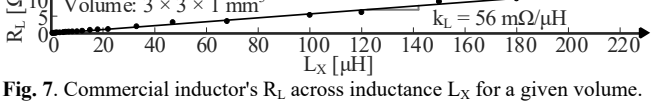

Fig. 7. Commercial inductor's R_L across inductance L_X for a given volume.

Equation (6) depicts this relation, and k_L is the coefficient:

$$R_L \equiv k_L L_X. \quad (6)$$

For a given inductor energy packet E_L, or $0.5L_X i_{L(PK)}^2$, because E_L scales quadratically with $i_{L(PK)}$, so $i_{L(PK)}$ falls with $1/L_X^{0.5}$ and t_E & t_D rises with $L_X^{0.5}$, as (7) & (8) shows:

$$i_{L(PK)} = \sqrt{\frac{2E_L}{L_X}}, \tag{7}$$

$$t_{E/D} = \left(\frac{dt}{di_L}\right) i_{L(PK)} = \left(\frac{L_X}{v_{E/D}}\right)\sqrt{\frac{2E_L}{L_X}} = \frac{\sqrt{2E_L L_X}}{v_{E/D}}, \tag{8}$$

where $v_{E/D}$ are L_X's energize/drain voltages. R_L incurs ohmic loss $P_{L(R)}$. According to (6)–(8), $P_{L(R)}$ rises with $L_X^{0.5}$:

$$P_{L(R)} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 R_L \left(\frac{t_E + t_D}{t_{SW}}\right) \equiv k_{L(R)} \sqrt{L_X}. \tag{9}$$

where $k_{L(R)}$ is the coefficient. Similarly, applying (7) and (8) to (5) reveals that for a given E_L, P_M' reduces with $1/L_X^{0.25}$:

$$P_M' = 2\sqrt{k_{M(R)}\left(k_{M(C)} + k_{M(L)}\right)} \propto \sqrt{i_{L(PK)}^2 t_{E/D}} \equiv \frac{k_M'}{\sqrt[4]{L_X}}, \tag{10}$$

where k_M' is the coefficient. Thus, an optimal L_X (denoted as L_X') balances $P_{L(R)}$ & P_M' to minimize ($P_{L(R)}$ + P_M'). Fig. 8 shows this trade-off and labels L_X'. L_X' can be expressed as:

$$L_X' = \sqrt[3]{\left(\frac{k_M'}{2k_{L(R)}}\right)^4}. \tag{11}$$

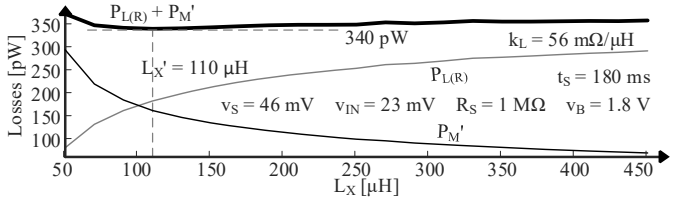

Fig. 8. Simulated optimal MOS switches' loss P_M' & ESR loss $P_{L(R)}$ across L_X.

This work uses a 120-μH L_X because it is the closest to the ideal 110-μH L_X' in the targeted 3 × 3 × 1 mm³ inductor series.

Peak Current: optimal $i_{L(PK)}$ minimizes fractional loss σ_{LOSS} of the SLCR. σ_{LOSS} is the fraction of the input power P_{IN} that is lost. This brief analyzes losses from optimal MOS switches, R_L, & switch-node parasitic capacitance C_{SW}:

$$\sigma_{SL} \equiv \frac{P_{LOSS}}{P_{IN}} \approx \frac{P_M'}{P_{IN}} + \frac{P_{L(R)}}{P_{IN}} + \frac{P_{CSW}}{P_{IN}} = \sigma_M + \sigma_{L(R)} + \sigma_{CSW}, \tag{12}$$

where σ_M, $\sigma_{L(R)}$, σ_{CSW} are fractional losses of optimal switches, R_L, C_{SW}. σ_{SL} is SLCR's total fractional loss. In DCM, P_{IN} is:

$$P_{IN} = v_{IN} i_{IN(AVG)} = v_{IN}\left[\left(0.5 i_{L(PK)}\right)\left(\frac{t_E + t_D}{t_{SW}}\right)\right] \propto i_{L(PK)}^2, \tag{13}$$

where $i_{IN(AVG)}$ is average input current. $i_{L(PK)}$ is proportional to t_E & t_D in DCM, thus, P_{IN} scales with $i_{L(PK)}^2$ in DCM. P_{CSW} only depends on f_{SW}, therefore, σ_{CSW} falls with $1/i_{L(PK)}^2$:

$$\sigma_{CSW} = \frac{P_{CSW}}{P_{IN}} = \frac{0.5 C_{SW} v_{SW}^2 f_{SW}}{P_{IN}} \equiv \frac{k_{\sigma CSW}}{i_{L(PK)}^2}, \tag{14}$$

where $k_{\sigma CSW}$ is the coefficient.

P_M' scales with $k_{M(R)}^{0.5}$, $k_{M(R)}$ scales with $i_{L(PK)}^2 t_{E/D}$, and $t_{E/D}$ scales with $i_{L(PK)}$ in DCM as (5), (1), & (8) indicates. Thus, $k_{M(R)}$ is proportional to $i_{L(PK)}^3$ and σ_M falls with $1/i_{L(PK)}^{0.5}$:

$$\sigma_M = \frac{P_M'}{P_{IN}} = \frac{2\sqrt{k_{M(R)}\left(k_{M(C)} + k_{M(L)}\right)}}{P_{IN}} \equiv \frac{k_{\sigma M}}{\sqrt{i_{L(PK)}}}, \tag{15}$$

where $k_{\sigma M}$ is the coefficient.

$P_{L(R)}$ scales with $i_{L(PK)}^2(t_E+t_D)$ as equation (9) suggests. In DCM, t_E and t_D scales with $i_{L(PK)}$. Therefore, $P_{L(R)}$ scales with $i_{L(PK)}^3$ and $\sigma_{L(R)}$ scales with $i_{L(PK)}$ as equations (16) reveals:

$$\sigma_{L(R)} = \frac{P_{L(R)}}{P_{IN}} = \left(\frac{2R_L}{3v_{IN}}\right) i_{L(PK)} \equiv k_{\sigma L(R)} i_{L(PK)}, \tag{16}$$

where $k_{\sigma L(R)}$ is the coefficient.

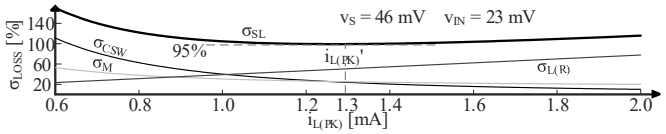

Fig. 9. Simulated fractional ohmic, charge, and leakage losses across $i_{L(PK)}$.

Because $\sigma_{L(R)}$ rises with $i_{L(PK)}$ while σ_{CSW} and σ_M fall with $i_{L(PK)}$, there exists an optimal $i_{L(PK)}$ that minimizes the total fractional loss σ_{SL}. Fig. 9 shows this trade off and labels the optimal $i_{L(PK)}$ (denoted as $i_{L(PK)}'$). $i_{L(PK)}'$ can be expressed as:

$$i_{L(PK)}' = \sqrt[3]{\left(\frac{k_{\sigma M} + \sqrt{k_{\sigma M}^2 + 32 k_{\sigma L(R)} k_{\sigma CSW}}}{4k_{\sigma L(R)}}\right)^2}. \tag{17}$$

The theory derives closed-form formulae (17), (11), (4) to achieve the least-lossy energy packet. This leads to the least-lossy power stage, thanks to the fixed-energy-packet scheme. $i_{L(PK)}'$ is also optimized across v_S, and simulated $i_{L(PK)}'$ and the simulated optimal σ_{SL} across v_S, are both shown in Fig. 10.

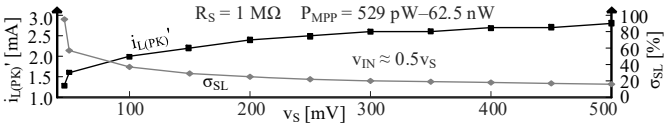

Fig. 10. Simulated optimal peak inductor current $i_{L(PK)}'$ and σ_{SL} across v_S.

D. Maximum-Supply Selector

Higher voltage between v_B & v_O is called v_{MAX}. The purpose of the maximum-supply selector is to bias M_{O2} & M_B's bulk with v_{MAX}. Fig. 11 shows its schematic, & its operation is like that in [23]. v_{MAX} is shorted to v_O or v_B through M_{VO} or M_{VB}.

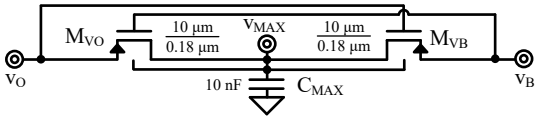

Fig. 11. Schematic of the maximum-supply selector.

Since v_{MAX} supplies gate drivers, so M_{VO} and M_{VB}'s widths should be wide enough so their channel resistances drop little voltage when supplying average driver current. A 10 nF C_{MAX} at v_{MAX} supplies instant driver current. 10-μm channel width ensures that instant voltage drop at v_{MAX} is less than 20 mV.

E. Prototype

180-nm CMOS die in Fig. 12 integrates power switches, gate drivers, & maximum-supply selector (except C_{MAX}). PCB in Fig. 12 shows the IC, L_X, C_{IN}, C_O, & C_{MAX}. Typical batteries like Li-ion batteries survive less than 2k recharge cycles [1]. Since IoT sensor's battery need to survive up to 182k recharge cycles, batteries for this application are often capacitors [1]. A 10-nF capacitor C_B functions as battery for testing purposes only. System-level C_B selection is in [3]. 1-μF C_{IN} leads to ±3 mV v_{IN} ripple, which causes 1.5% error from the actual P_{MPP}.

An off-chip TEG is 60–309× bulkier than off-chip passives (capacitors & L_X), since off-chip passives occupy 14 mm² in total. So, off-chip passives don't refute the area saved by using on-chip TEGs. On PCB, a voltage source & a 1-MΩ resistor emulate v_S & R_S. External FPGA controls the prototype.

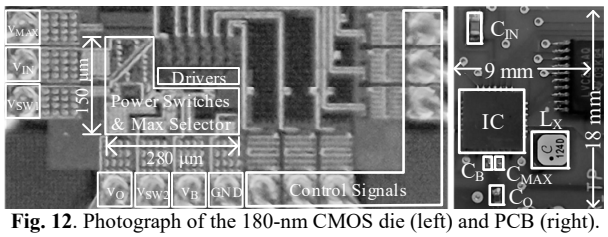

Fig. 12. Photograph of the 180-nm CMOS die (left) and PCB (right).

III. Power Management

A. Power Losses and Efficiency

Over-Sourced: Because the focus of this brief is the design theory, but not control. Thus, an FPGA externally implements the controller in Fig. 5. Fig. 13 shows measured σ_{LOSS}.

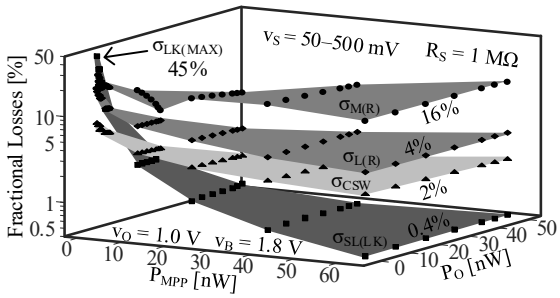

Fig. 13. Measured over-sourced fractional losses across P_{MPP} and P_O.

With higher P_{MPP}, MOS switches' fractional ohmic loss $\sigma_{M(R)}$ dominates. This is because W_{MOS} are optimally reduced to suppress leakage, which leads to increased R_{MOS}. R_L's fractional loss $\sigma_{L(R)}$ is next because the tiny L_X measures a high R_L of 6.1 Ω. Keithley 6485 Pico-Ammeter with ±10-fA resolution measures the total leakage loss $P_{SL(LK)}$ of the SLCR. C_O, C_B, & C_{MAX} leak 60–70 pW in total, while the IC leaks 220–230 pW. Measured total fractional leakage is labelled as $\sigma_{SL(LK)}$. Because $P_{SL(LK)}$ is fixed & does not scale with P_{MPP}, so $\sigma_{SL(LK)}$ rises from 0.4% to 45% as P_{MPP} drops from 62.5 nW to 625 pW. This is why optimizing leakage loss is important.

The total power an SLCR delivers is P_O plus P_B. Thus, this brief defines ideality factor η_I as in (18) to assess the SLCR's overall efficiency in over-sourced mode:

$$\eta_I = \frac{P_O + P_B}{P_{MPP}} = (P_O + P_B)\left(\frac{R_S}{v_{MPP}^2}\right) = (P_O + P_B)\left[\frac{R_S}{(0.5v_S)^2}\right]. \quad (18)$$

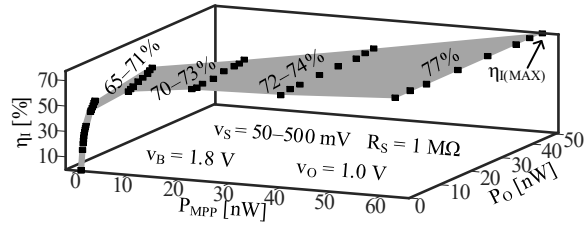

Fig. 14. Measured over-sourced η_I across P_{MPP} and P_O.

Fig. 14 shows measured η_I across P_{MPP} and P_O. Measured maximum ideality factor $\eta_{I(MAX)}$ is 77% when v_S is 500 mV and P_{MPP} is 62.5 nW. As v_S and P_{MPP} reduces, $\sigma_{SL(LK)}$ starts to dominate as shown in Fig. 13. As a result, η_I reduces sharply. η_I drops to 0% as v_S and P_{MPP} reduces to 50 mV and 625 pW.

Under-Sourced: efficiency η_C in under-sourced mode is $P_{O(B)}$ (defined in Section II.A) compared to P_B drawn from v_B:

$$\eta_C \equiv \frac{P_{O(B)}}{P_B}. \quad (19)$$

Similar strategy as in Section II.C that balances $P_{M(R)}$ & $P_{M(C)}$ also applies in under-sourced mode to find $i_{L(PK)}$'. The only difference is MOS switches are designed for nW over-sourced mode, so W_{MOS} should be treated as constant in this mode.

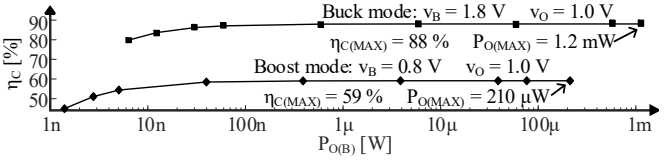

Fig. 15. Measured under-sourced η_C in buck- and boost-mode across $P_{O(B)}$.

Measured η_C when v_B is 1.8 V (or 0.8 V) that bucks (or boosts) to the 1.0-V v_O is shown in Fig. 15. $i_{L(PK)}$' in buck mode is 3.0 mA. FPGA fixes each E_B to the 3.0-mA $i_{L(PK)}$', and adjusts the number of E_B delivered per unit time to adjust $P_{O(B)}$. Max η_C is 88% even with small switches, and maximum output power $P_{O(MAX)}$ is 1.2 mW. $i_{L(PK)}$' in boost mode is 580 µA since M_B's v_{GD} is only 0.8 V, so its high R_{MOS} limits $i_{L(PK)}$'. When boosting, $\eta_{C(MAX)}$ is 59% & $P_{O(MAX)}$ is 210 µW.

B. Minimum Input Voltage $v_{IN(MIN)}$

Measured charging profiles across 30–70-mV v_S are shown in Fig. 16. Initial battery voltage $v_{B(I)}$ is 1.0 V. When measuring charging profiles, all energy packets from v_S transfer to v_B and FPGA adjusts t_S to keep v_{IN} at half v_S. $v_{B(MAX)}$ is the maximum voltage v_B can reach. In this work, $v_{B(MAX)}$ is the 1.8-V CMOS breakdown voltage V_{BD}. In Fig. 16, 50 mV is the lowest v_S such that v_B can be charged to 1.8 V. This means $v_{IN(MIN)}$ is 25 mV and the minimum P_{MPP} is 625 pW. For testing concerns only, SLCR is shut off externally in the lab when v_B hits V_{BD}.

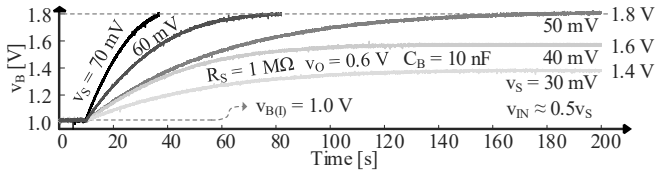

Fig. 16. Measured charging profiles across v_S.

IV. Discussion & State-of-the-Art Comparison

A. Controller Power Consumption

Although this brief aims at theory, for completeness, this sub-section discusses impacts of controller power P_{CNTR}. For a controller like [4] & Fig. 5, Table II cites the P_{CNTR} breakdown in [4] & [24], & Fig. 17 shows simulated η_I including P_{CNTR}.

Majority of the controller burns 47 pJ/Cycle as in [4], and state-of-the-art voltage reference could burn as low as 2.22 pW [24]. Despite P_{CNTR} degrades η_I the most when v_{IN} & P_{MPP} are low as Fig. 17 shows, the simulated $v_{IN(MIN)}$ with P_{CNTR} is about 28 mV while that without P_{CNTR} is 23 mV. This means P_{CNTR} only degrades $v_{IN(MIN)}$ by 5 mV, or equivalently, 22%.

When v_{IN} & P_{MPP} are higher, P_{CNTR} degrades η_I less, by about 8%. Simulated $\eta_{I(MAX)}$ with P_{CNTR} is about 76%. To cold-start, prior art like [1] uses a starter circuit to build up high voltage on a small capacitor, from which bootstraps the SL afterwards.

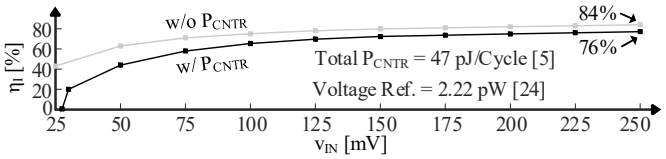

Fig. 17. Simulated η_I with and without controller power consumption P_{CNTR}.

TABLE II: POWER BREAKDOWN OF STATE-OF-THE-ART CONTROLLER

Block	Power	Block	Power	Block	Power
CP_{MPP}	8.3 pJ/Cycle	CP_M	9.7 pJ/Cycle	CP_O	8.6 pJ/Cycle
$CP_{ZCD(B)}$	8.4 pJ/Cycle	$CP_{ZCD(O)}$	12 pJ/Cycle	Voltage Ref.	2.22 pW

B. State-of-the-Art

Table III lists the state-of-the-art and shows simulated impacts of P_{CNTR} on performance for this work. Design in [16] neglects MOS leakage so $P_{IN(MIN)}$ are at µW level. Design in [17] reduces MOS leakage by cascoding switches. But cascoding switches in series doubles $P_{M(R)}$ & $P_{M(C)}$. Also, the optimal design theory for cascoded switches is absent in [17].

TABLE III: STATE-OF-THE-ART LOW-POWER CMOS SL CONVERTERS

	[16]	[17]	[18]	[19]	[A][20]	This work
R_S	210 Ω	526 Ω	160 kΩ	–	1 MΩ	1 MΩ
Tech.	180 nm	28 nm	180 nm	180 nm	180 nm	180 nm
$v_{B(MAX)}$	2.4 V	1.8 V	1.8 V	4.1 V	0.9 V	1.8 V
$v_{IN(MIN)}$	30 mV	100 mV	25 mV	140 mV	20 mV	[*]25[B] / [*]28[C] mV
$P_{IN(MIN)}$	4.3 µW[D]	19 µW[D]	25 nW	10 nW[D]	1.1 nW	625[B] /784[C] pW
$P_{O(MAX)}$	24 mW	60 mW	2.4 mW	1 µW	4 nW	1.2 mW
$\eta_{I(MAX)}$	Not nano-Watt		23%[E]	75%[D]	53%	77%[BF] / 76%[CF]

[A]Boost only. [B]Measured without P_{CNTR}. [C]Simulated to include P_{CNTR}. [D]Estimate. [E]Estimate at P_{IN} = 60 nW. [F]When P_{MPP} = 62.5 nW. [*]With v_B = 1.8 V.

$P_{IN(MIN)}$ of the designs in [18–19] is 10–25 nW. But [19] only supports 1 µW $P_{O(MAX)}$, which is insufficient for complex sensor functions & data transmission [3]. Moreover, nW η_I is only 23% for the design in [18]. Also, detailed design theory is missing in [16–19]. [20] shows a high-R_S design. Its power stage is a boost only, and a theory on optimal L_X is absent.

This brief's key contribution is theoretical loss analysis & closed-form formulae that co-design switches, L_X, & $i_{L(PK)}$ for highest efficiency, which is absent in [16–20]. The other contribution is experimental validation with a 180-nm IC.

V. CONCLUSIONS

This brief proposes a theory on the highest-efficiency design of low-v_{IN} high-R_S nW CMOS SLCR for on-chip TEGs. The difficulty is to design a nW SLCR often needs prolonged trial-and-error process. So, this brief presents a theory with closed-form formulae that optimizes CMOS switches, inductor, & peak current, to achieve the highest efficiency possible. This brief also shows measured results of a 180-nm IC that harvests from 1-MΩ R_S with 25 mV $v_{IN(MIN)}$ & 77% peak efficiency.

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