High-PSR LDOs: Variations, Improvements, and Best Compromise

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***Abstract*— Low-Dropout Regulators (LDOs) are used to power noise sensitive applications. Power Supply Rejection (PSR) is a performance metric that measures the LDO's ability to reject noise. Improving PSR has been the focus of many research groups. However, the state of the art does not recognize the best PSR enhancement schemes and collate them under comparable grounds. Further, the pass transistor's diode connection (through the Gate-Drain capacitance) impacts the PSR, and this effect is not quantified in the state of the art. This research aims to bridge these gaps first by explicating the constitution of a high PSR LDO. Then, the impact of the pass transistor's parasitics on PSR are quantified. Following this, the best state of the art PSR enhancement schemes are analyzed and simulated over a high-PSR core under similar conditions. This study reveals the strengths and limitations of each scheme, which unfolds each technique's applications. Results convey that the LDO Filter yields the best PSR improvement at low frequencies, Series feedback at mid frequencies, and RC filter at high frequencies. Assessment concludes that Series Feedback provides the best compromise with respect to PSR enhancement.**

Index Terms– Analog, LDO, Linear Regulators, Power supply rejection (PSR), SPICE

I. LDOs In Analog Systems

Supplying and regulating power is fundamental to the operation of electric systems. The wide range of applications from Portable electronics, Defense applications, microsensors, Automotive electronics, etc. cannot sustain themselves without energy, and cannot function without a stable power supply [1].

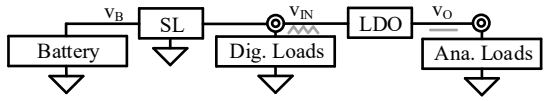

Fig. 1: Typical Power-Supply System.

Switching regulators (SL) efficiently regulate power but have limited bandwidths, typically around 370 kHz [2]. They suffer from poor load dump responses, causing the supply voltage to droop in the event of a load step. SLs have large ripple at their outputs, which manifests as Power Supply noise. Digital loads (logic gates) are not very sensitive to such noise and can function optimally under such supply conditions. Analog loads such as ADCs, PLLs, Amplifiers, and Mixers are susceptible to supply ripple and require low noise power supplies.

In typical applications, a low-dropout regulator (LDO) is used in series with SLs to reject noise and provide a clean regulated voltage [1]. Characterized with higher bandwidths, LDOs respond faster to load disturbances, yielding smaller voltage droops in the event of load steps. The LDO's regulated output can be used to power noise sensitive Analog loads. PSR is a measure of how much input ripple is suppressed by the LDO. Modern applications like medical imaging demand high PSR (>50 dB) [3], especially in mid frequencies (0.1–1 MHz), where SLs switch and induce noise. This has motivated researchers to investigate techniques to enhance the PSR of LDOs.

The State of the art presents numerous techniques to improve the PSR of LDOs [4-11], but fails to compare the best techniques under similar conditions and operating points. The State of the art also fails to establish the grounds on which LDOs achieve the best PSR. The parasitic gate-drain capacitance which diode connects the pass transistor can impact PSR even in the low-mid frequency range. [12] recognizes the noise coupling effects due to parasitics, but does not quantify how it impacts the PSR across frequency. This work aims to bridge this gap by quantifying these effects both mathematically and graphically.

The purpose of this research is to first recognize the design factors affecting PSR and establish a high-PSR core LDO. This is covered in Section II. Sections III and IV present the best State of the art techniques that improve PSR. These techniques are applied as layers of concepts over the established core, and SPICE simulations reveal the PSR improvements. The highlighted strengths and limitations assist in assessing the conditions under which the said techniques offer maximum benefits. Section V compares the techniques discussed in this work, followed by Conclusions in Section VI.

II. High-PSR Core

An LDO with high PSR is essential to reject supply noise generated by SLs. Fig. 2 depicts a typical LDO consisting of an Error Transconductor (G_E) and a low output impedance Buffer (A_B) that close a negative feedback loop around pass transistor M_P. If this loop is stabilized, the output voltage (v_O) is established as a function of the reference voltage (v_R) and the feedback resistors (R_{FB1}, R_{FB2}). Implementing M_P using PMOS transistors results in low dropout voltages when compared with NMOS pass transistors. Further, a replica LDO topology [13] offers a more predictable stability response, but suffers from poor load regulation due to the unregulated loading [14]. Thus, a single transistor M_P is suitable.

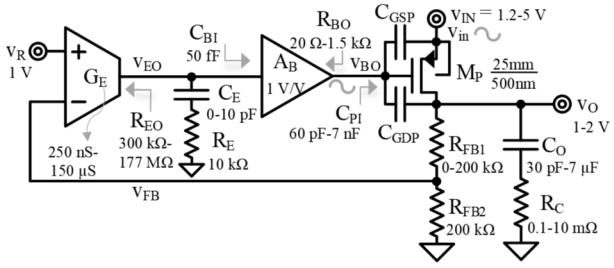

Fig. 2: Typical LDO composition.

A. Loop Gain

The LDOs loop gain depicted in Fig. 3 can be analyzed by considering the poles/zeroes established at each node. Each node contributes to a pole whose frequency is given by the RC frequency associated with that node, giving rise to poles p_E, p_{BO}, and p_O. Further, the current limiting effects of R_C (ESR of C_O) and resistance R_E establish zeroes (z_E, z_O) with their respective capacitances that boost phase margins. The DC loop gain (A_{LG0}) and the output impedance (R_O) can be expressed as:

$$A_{LG0} = G_E R_{EO} A_B g_{mP} R_O \left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right), \quad (1)$$

$$R_O = (R_{FB1} + R_{FB2}) || r_{dsP}. \quad (2)$$

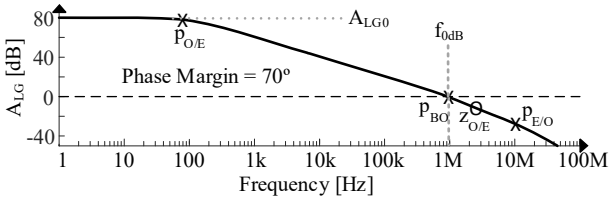

Fig. 3: LDO's Loop gain plot depicting poles and zeroes.

With a single pole roll-off, the unity gain bandwidth (f_{0dB}) is the product of the DC loop gain and the location of the dominant pole p_D. Depending on the location of the dominant pole, LDO designs could be either output stabilized ($p_D = p_O$) [15,16] or internally stabilized ($p_D = p_E$) [17,18]:

$$f_{0dB} = A_{LG0} p_D \,|_{p_D = p_E \text{ (or) } p_O}. \quad (3)$$

The PSR performance of output and internally stabilized designs are vastly different, and this will be evident in the following sub-sections.

B. Gate Ripple

Since M_P is a PMOS, and the input ripple is connected to M_P's source, it is desired to replicate this ripple at M_P's gate to ensure that there is no small signal source-gate voltage. This ensures that there is no noise injection through the g_m currents of M_P. There are two ways of replicating the input ripple at the gate:

1. Feed-Forward path

The input ripple is injected to the gate of M_P by using a feed-forward path [8,9] as shown in Fig. 4.

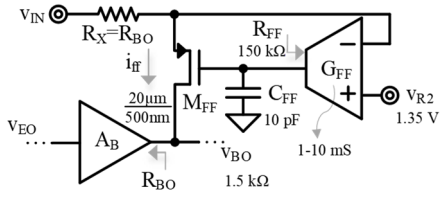

Fig. 4: Supply Noise replication through Feed-fw.

Transconductor G_{FF} closes a negative feedback loop around M_{FF}. This loop holds M_{FF}'s source at ac ground, generating feed-forward current i_{ff}. This feed-fw current is injected into the output of the buffer, and under the condition that R_X=R_{BO}, impresses a voltage at v_{bo} given by:

$$v_{bo} = i_{ff} R_{BO} = \left(\frac{v_{in}}{R_X}\right) R_{BO} = v_{in}. \quad (4)$$

The bandwidth of this loop (f_B) should be much greater than the Buffer pole p_{BO} to ensure that the feed-forward path does not hinder the ripple replication until p_{BO} shunts.

$$f_B = A_{BLG0} p_G \gg p_{BO}|_{p_G = \frac{1}{2\pi R_{FF} C_{FF}}}. \quad (5)$$

2. Current mirror

The other method to replicate supply ripple is to utilize the current mirror in the error transconductor (G_E) [1]. Fig. 5 shows the Differential stage of the error transconductor feeding a P-type current mirror, with its equivalent small signal model.

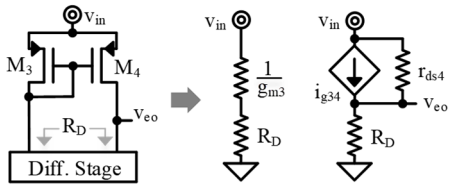

Fig. 5: Supply Noise replication through current mirrors.

The fraction of input ripple (v_{in}) reaching the output of the error transconductor (v_{eo}) is denoted by A_{DD}, and can be calculated by applying superposition:

$$A_{DD} = \frac{v_{eo}}{v_{in}} = \frac{v_{in} R_D}{R_D + r_{ds4}} + i_{g34}(R_D || r_{ds4}), \quad (6)$$

$$\frac{v_{eo}}{v_{in}} = \frac{v_{in} R_D}{R_D + r_{ds4}} + \left(\frac{v_{in}}{1/g_{m3} + R_D}\right)(R_D || r_{ds4}) \approx 1. \quad (7)$$

This indicates that the P-type mirror replicates the positive supply ripple at v_{eo} and this ripple can propagate to the gate of M_P through the buffer A_B. This technique is superior to the feed-fw technique since it eliminates the need for additional circuitry, that imposes its own bandwidth and gain constrains, in addition to power consumption. Thus, the designs discussed in this work will use a P-type mirror to replicate supply ripple.

C. PSR

PSR is the inability to amplify supply noise and can be analyzed as the reciprocal of the supply gain (A_{IN}) [19]. Fig. 6 depicts the voltage divider model of supply gain, where the supply gain is the fraction of the input ripple that reaches the output.

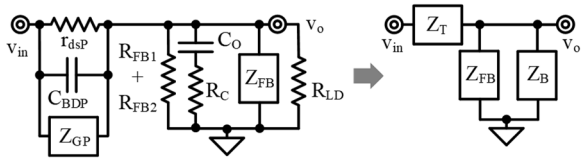

Fig 6: Voltage divider model of A_{IN}.

$$A_{IN} = \frac{1}{PSR} = \frac{v_o}{v_{in}} = \frac{Z_{FB} || Z_B}{(Z_{FB} || Z_B) + Z_T}. \quad (8)$$

Z_{GP} factors the noise coupling effects of M_P's diode connection through C_{GDP}. From the perspective of the output node, the network of C_{GSP}, C_{GDP}, and R_{BO} presents a voltage divided $1/g_{mP}$ impedance to the supply that decreases with operating frequency (f_O). This impedance overwhelms r_{dsP} at frequency f_{GP1}. Z_{GP} keeps decreasing until f_{GP2} where the effects of R_{BO} disappear, and Z_{GP} flattens out as per (11). Fig. 7(a) depicts the effective impedance Z_T as a function of frequency.

$$Z_{GP} = \frac{1}{G_P} = \frac{\left(\frac{1}{sC_{GSP}} || R_{BO}\right) + \frac{1}{sC_{GDP}}}{g_{mP}\left(\frac{1}{sC_{GSP}} || R_{BO}\right)}, \quad (9)$$

$$Z_{GP}|_{f_O \geq \frac{1}{2\pi R_{BO}[C_{GDP}(g_{mP} r_{dsP} - 1) - C_{GSP}]} = f_{GP1}} \leq r_{dsP}, \quad (10)$$

$$Z_{GP}\big|_{f_O \geq \frac{1}{2\pi R_{BO}(C_{GSP}+C_{GDP})} = f_{GP2}} \approx \frac{C_{GDP}+C_{GSP}}{g_{mP}C_{GDP}}, \quad (11)$$

$$Z_T = r_{dsP} \left|\left| \frac{1}{sC_{BDP}} \right|\right| Z_{GP}, \quad (12)$$

$$Z_B = (R_{FB1}+R_{FB2}) || \left(\frac{1}{sC_O}+R_C\right) || (R_{LD}), \quad (13)$$

$$Z_{FB} = \frac{1}{G_{LG}} = \frac{1}{G_E R_{EO} A_B\, g_{mP}}. \quad (14)$$

Z_{FB} captures the effects of shunt feedback at the output of the LDO. At low frequencies, Z_{FB} dominates the parallel combination described by (8), resulting in very low A_{IN} (and thus, high PSR). As f_{0dB} is approached, the effects of shunt feedback disappear, and the supply gain is a function of the external filter components connected at the LDOs output.

Fig. 7(b) shows the supply gain plots of internally and output stabilized LDOs across frequency. Crossing the dominant pole of the output stabilized design (p_O) has no effect on Z_{FB} as per (14), and A_{IN} remains constant. However, crossing the dominant pole of the internally stabilized design (p_E') increases Z_{FB}, and due to this A_{IN} increases beyond p_E'.

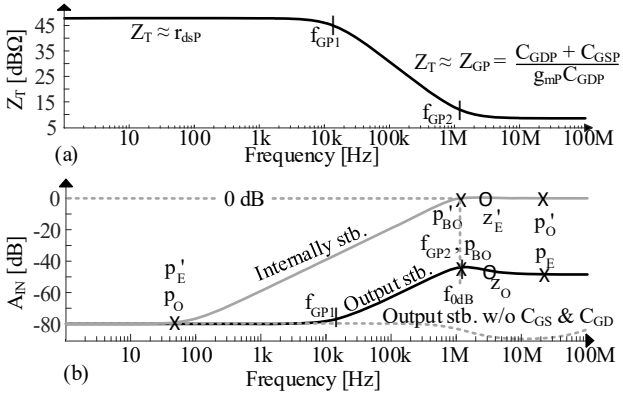

Fig. 7: (a) Z_T vs frequency, (b) A_{IN} for internally and output stabilized LDOs.

Beyond f_{GP1}, the decreasing Z_{GP} overwhelms r_{dsP}, and dominates the parallel combination. This couples noise to the output node, and the supply gain increases as shown in Fig. 7(b). This effect disappears at f_{GP2}, beyond which the noise Z_{GP} couples is constant. Pushing f_{GP1} to higher frequencies helps improve A_{IN}. Without parasitic coupling, this effect is not seen. Instead, Z_{CO} overwhelms Z_{FB} and improves A_{IN} near f_{0dB}.

Beyond f_{GP2} and f_{0dB}, the shunted C_O (p_O) decreases A_{IN} until z_O, at which point R_C's current limiting effects flatten A_{IN}. At f_{0dB}, the output stabilized design offers much lower A_{IN} since p_O has shunted, and thus the supply noise has a low impedance path to ground. However, the output pole (p_O') of the internally stabilized design has not shunted at f_{0dB}, and hence offers a higher A_{IN}. Thus, an output stabilized design is desired.

Thus, the established high-PSR core is an output stabilized design with the gate ripple replicated with the help of the P-type current mirror in the error transconductor. This core establishes the grounds on which the PSR enhancement techniques discussed in the next sections can be compared.

III. Pre-Filtered Input

In this section, three techniques are presented which improve the PSR of the LDO. These techniques are applied as layers of concepts over the core that was established in the previous section. Fig. 8 shows the schematics of the three pre-filter techniques, and Fig. 11 shows the simulations of the improved supply gains (A_{IN}) of the LDO upon applying these techniques.

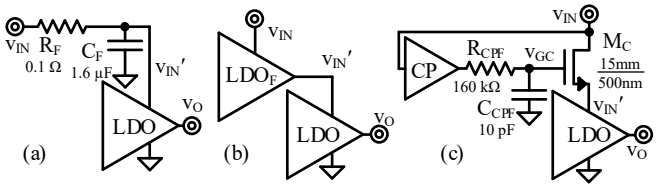

Fig. 8: (a) RC, (b) LDO, and (c) CP-NMOS Pre-Filter.

A. RC Filter

This technique uses a simple RC filter to clean up the supply ripple before it reaches the input of the LDO [4]. The cutoff frequency of this filter adds a pole in the supply gain response of the high-PSR core as shown in Fig. 11. The cutoff frequency is chosen to be a decade below f_{0dB} of the core:

$$p_{RC} = \frac{1}{2\pi R_F C_F} = \frac{f_{0dB}}{10}. \quad (15)$$

A low resistance of R_F is desired to minimize static power. This yields a large off-chip capacitor of 1.6 μF for C_F, which is a limitation. The ESR of C_F establishes a zero (z_{RC}) that flattens the A_{IN} response, and this limits the maximum improvement attainable. The other limitation relates to headroom- the voltage drop across R_F adds with the dropout voltage of the core, increasing effective dropout (V_{DO}).

B. LDO Filter

This technique cascades two LDOs in series [4]. The filtering regulator LDO_F shields the core from the supply ripple. LDO_F can be made on-chip, thus requiring an internally stabilized design. This can be designed as a Transconductor ($G_{E(F)}$) closing a negative feedback loop around pass transistor $M_{P(F)}$, establishing the dominant pole at the gate of $M_{P(F)}$ ($p_{BO(F)}$). The unity gain frequency ($f_{0dB(F)}$) of LDO_F is:

$$f_{0dB(F)} = \frac{G_{E(F)} g_{mP(F)} R_{O(F)}}{2\pi C_{PI(F)}}. \quad (16)$$

The design can be approached taking care that $f_{0dB(F)}$ and $A_{LG0(F)}$ should be at least equal to the core's parameters. This ensures that LDO_F effectively shields the core at least until f_{0dB} is reached. These yield $G_{E(F)}$ of 200 μS and $R_{EO(F)}$ of 250 kΩ. As seen in Fig. 11, this technique drastically improves the supply gain at lower frequencies. Being an internally stabilized design, A_{IN} of LDO_F degrades beyond the dominant pole $p_{BO(F)}$, thus degrading the supply gain of the cascaded pair.

Near and beyond $f_{0dB(F)}$, this technique provides little to no improvement in A_{IN}. Increasing $f_{0dB(F)}$ to orders of magnitude higher than f_{0dB} would present its own design challenges as parasitic poles would jeopardize the stability of LDO_F. Since two LDOs are in series, this technique also increases dropout.

C. Charge-Pumped NMOS Filter

In [5], an NMOS device was used to cascode the LDO. The gate of the NMOS was biased using an RC filter connected to the input supply. This source follower configuration shields the core from input ripple similar to the RC filter discussed earlier. The RC filter does not dissipate static power, so the resistance can be made large. The drawback is that the dropout is a Gate-Source voltage (500-600mV) above the dropout of the core.

An improvement to this technique is presented in [6]. As shown in Fig. 8(c), a Charge pump of N stages is used to boost the gate drive of the cascode transistor M_C. The effective dropout voltage is a $V_{DSC(SAT)}$ above the dropout of the core. R_{CPF} and C_{CPF} maintain the role of the RC filter to clean up supply ripple. To keep M_C in the saturated inversion region,

$$V_{GSC} = (N+1)V_{IN} - 2NV_{Diode} - V_{IN}', \quad (17)$$

$$V_{DSC} = V_{IN} - V_{IN}' \geq V_{GSC} - V_{TN0}, \quad (18)$$

$$V_{IN} < 2V_{Diode} + \frac{V_{TN0}}{N}. \quad (19)$$

This imposes a maximum input voltage constrain. If V_{IN} increases beyond this limit, M_C enters linear region, and the noise from V_{IN} directly couples to the input of the LDO. Thus, a single stage charge pump is chosen. Width of M_C can be designed from choosing $V_{DSC(SAT)}$ of 250 mV that yields W_C of 15mm. The pole of the RC filter can be chosen to be a decade below f_{0dB}, similar to (15).

The supply gain simulations reveal that while the diodes in the charge pump and the RC filter do filter the input ripple, the input ripple couples to the gate of M_C (v_{gc}) through the large gate-drain capacitance (C_{GDC}) of M_C:

$$v_{gc} = \frac{C_{GDC}}{C_{GDC} + C_{CP}}. \quad (20)$$

M_C has a large width and consequently a large C_{GDC} of 10pF. This capacitive coupling leads to a large fraction of input ripple being coupled to v_{gc}, and source follower M_{CP} replicates this ripple to the input of the core. This yields a minor supply gain improvement (5-6 dB), as depicted by Fig. 11.

The limitations stem from the noise coupling nature, making it unsuitable for high load current applications. Larger loads demand a larger W_C, which increases C_{GDC} (and noise coupling), thus decreasing the improvement in A_{IN}. The other limitation is the maximum input voltage constrain induced by the Charge pump mechanism. Finally, the dropout is increased by $V_{DSC(SAT)}$. [6] were able to obtain 30 dB of improvement using this technique, reaching 70 dB of PSR at DC. This high improvement is mainly due to the lower target load current.

IV. Series Feedback

The Series feedback (SFB) technique [7] can improve supply gain at mid-high frequencies, without dissipating additional ohmic losses or increasing V_{DO}. As seen from Fig. 6, lower A_{IN} can be achieved either by decreasing Z_{FB}, or by increasing Z_T. The LDO's shunt feedback action already decreases Z_{FB} in the low-mid frequencies. Extending the frequency range where Z_{FB} remains low can compromise stability due to parasitic poles. This technique introduces a high frequency series sampling loop that increases the impedance presented to the supply (Z_T). Fig. 9 depicts the LDO with series feedback.

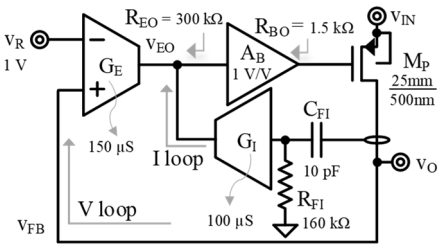

Fig. 9: Series Feedback.

Transconductor G_I and the high pass filter (R_{FI}, C_{FI}) close a series sampling loop (I loop) around M_P. Note that the series sampling action can be implemented with a mirror PMOS (M_P') that is scaled down in size, in series with a sense resistor.

The I loop gains maximum strength based on the cutoff frequency set by the high pass filter (p_{FI}), chosen to be a decade below the core's unity gain frequency. The peak loop gain of the I-loop ($A_{LGI(MAX)}$) is chosen to be 30, and is given by:

$$A_{LG(I)(MAX)} \approx G_I R_{EO}. \quad (21)$$

After attaining the peak value, the loop gain of the I-loop rolls off after p_{BO} shunts as shown in Fig. 10(a). The loop gain of the outer loop (V loop) that establishes v_O as a function of v_{REF} at low frequency is also shown. The 0-dB crossing point of the I loop creates a pole (p_I) in the V loop, which affects f_{0dB} (60 kHz) and Phase Margin (40°) of the V loop.

Fig. 10(b) depicts the plot of A_{IN} for the SFB LDO. Due to the effects of Z_{GP}, A_{IN} increases beyond f_{GP1} until f_{0dB}. Beyond f_{0dB}, the combined effects of the shunting output capacitor and the increasing strength of the I loop decreases A_{IN}, resulting in a "peaking" effect around f_{0dB}. Once $A_{LG(I)(MAX)}$ is reached, A_{IN} flattens. After p_{BO} shunts, f_{GP2} is reached and R_C current limits C_O, A_{IN} increases, and joins the core's response at f_{0dBI}.

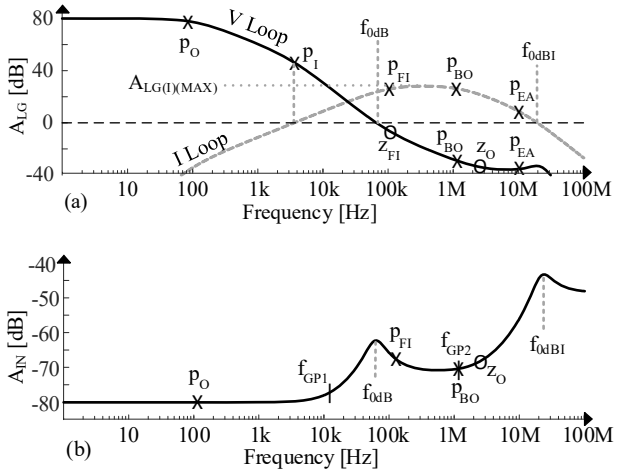

Fig. 10: (a) Voltage and Current loop gains, (b) Supply gain of SFB LDO.

To compensate for the drop in f_{0dB}, G_E would need to be raised proportionately to maintain the same f_{0dB} as the core. This would mean higher quiescent currents, which would impact the overall current efficiency of the LDO. This is not done in this work to maintain the same A_{LG0}. [7] were able to obtain 20 dB of improvement using this technique, reaching 50 dB of PSR around their unity gain frequency.

V. Comparison

This section presents a comparison of the various PSR enhancement techniques. Fig. 11 shows the A_{IN} plots for each technique, and Table 1 provides a quantitative comparison. The LDO filter drastically improves PSR at low frequencies but starts degrading towards the mid-high frequency range. The RC filter utilizes a large off-chip capacitor to improve PSR at high frequencies. The CP-NMOS provides little improvement in PSR due to the noise coupling through parasitics of the large cascoding NMOS. Series-FB improves PSR in the mid-high frequency range without compromising V_{DO}, but at the expense of reduced f_{0dB} and little quiescent power (P_{GI}) consumed by G_I.

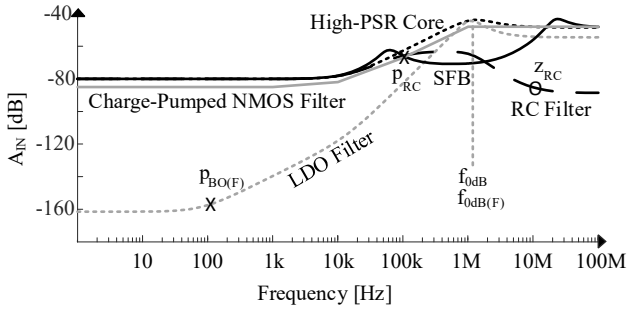

Fig. 11: Supply gain plots of the discussed PSR enhancement techniques.

TABLE I: PSR COMPARISON

Parameter	High PSR Core	RC Filter	LDO Filter	CP NMOS	Series Feedback
PSR(10 kHz)	78 dB	78 dB	118 dB	82 dB	78 dB
PSR(100 kHz)	62 dB	66 dB	82 dB	67 dB	66 dB
PSR(1 MHz)	44 dB	64 dB	44 dB	48 dB	71 dB
PSR(10 MHz)	48 dB	85 dB	54 dB	48 dB	57 dB
PSR(100 MHz)	48 dB	88 dB	54 dB	48 dB	48 dB
V_{DO}	0.2 V	0.4 V	0.7 V	0.45 V	0.2 V
Power	–	$+P_{RF}$	$+P_{LDO(F)}$	$+P_{CP}$	$+P_{GI}$
Space	–	$+R_F$, C_F	$M_{P(F)}+G_{E(F)}$	+ CP	G_I+M_P'

*Simulation results shown for same operating conditions.

Researchers have investigated techniques to improve PSR by bulk modulation [10,11]. Biasing the bulk terminal introduces substrate currents that contribute to power loss. Constrains exist to prevent the body diode from switching on. The solutions tend to complicate the circuit, and this increases Silicon area, cost, and test times while providing similar PSR improvements as the techniques previously discussed. For these reasons, these techniques have been excluded in this work.

Another area that has gained the attention of researchers is Digital LDOs [20, 21]. They use digital control to turn on a number of switches in a FET array to supply the load. The power transistors are driven to linear region; the supply ripple couples directly to the output. This makes digital LDOs exhibit poor PSR performance and have been excluded in this work.

VI. CONCLUSIONS

This work establishes a high PSR core, investigating the effects of the pass transistor's diode connection which the state of the art did not account for. By analyzing and simulating the best PSR enhancement techniques in the state of the art, improvements in PSR are revealed, elucidating their potential use cases. The LDO filter provides the best PSR improvement at low frequencies, Series-FB at mid frequencies, and RC filter at high frequencies. Improving PSR (>25 dB) without sacrificing dropout and with little additional power consumption makes Series-feedback utilizing a PMOS current mirror the best compromise with respect to PSR enhancement. Charge pumped NMOS regulators operate in a source follower configuration, and will exhibit frequency spurs at the regulator's output near and around the Charge pump's frequency, making PMOS based LDOs with Series feedback superior in performance.

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