180-nm 85%-Efficient Inductively Coupled Switched Resonant Half-Bridge Power Receiver

Nan Xing, Graduate Student Member, IEEE, and Gabriel A. Rincón-Mora, Fellow, IEEE

Abstract—Receiver coils in embedded microsensors are small and their transmitters are unpredictably distant and misaligned, so available power is low and variable. The 180-nm, 6.78-MHz switched resonant half bridge here, however, only uses two transistors with a transfer rate and duration that are both adjustable. This way, the prototype outputs 13%–85% of the power of transmitters (DSP), and power amplifiers (PA) in the system.

Sensors, amplifiers (AV), data converters (ADC), digital-signal processors (DSP), and use to recharge a battery vB and supply a system. The so available power is low and variable. The 180-nm, 6.78-MHz switched resonant half bridge here, however, only uses two transistors with a transfer rate and duration that are both adjustable. This way, the prototype outputs 13%–85% of the power of transmitters (DSP), and power amplifiers (PA) in the system.

Index Terms—Inductively coupled power receiver, switched resonant half bridge, weakly coupled charger, wireless power.

I. POWERING MICROSYSTEMS INDUCTIVELY

Structurally embedded microsensors and biomedical implants can sense, process, and transmit data that save energy, money, and lives. Embedded applications normally require smart, small, and immobile sensors that do not receive light. Meeting these demands is challenging because, with so much functionality, sensors easily drain their small onboard batteries. Since motion and light energy are absent and temperature gradients are so low that thermal energy is almost as absent, coupling power inductively like Fig. 1 shows is often the only viable means of powering these devices [1].

The transmitting coil LT and capacitor CT resonate at the operating frequency fO of the source VS. The alternating magnetic field that LT emanates induces a current in the nearby receiver coil LR that the power receiver can harness and use to recharge a battery vB and supply a system. The power supply draws and feeds power on demand to the sensors, amplifiers (AV), data converters (ADC), digital-signal processors (DSP), and power amplifiers (PA) in the system.

Small receiver coils in embedded applications are usually several radial distances away from their transmitter coils [1]–[4]. LR therefore harnesses a small fraction of the power that LT avails [1]–[2], [4]. As a result, LR normally under-damps its transmitting source VS. With so little power available, optimal maximum power-point (MPP) operation is vital [6].

Under-damping VS means that the electromotive force (EMF) voltage vE induced in LR is capable of supplying more power PE. This is why resonant receivers are popular in this space, because exchanging more energy between LR and a resonating capacitor CR raises the current iL with which LR draws PE from vE [6]. But since LR’s series resistance RR and transistors consume more power with higher iL, power losses limit how much of PE the receiver can output with PO.

The switched resonant half-bridge power receiver presented here is largely the result of theory presented in [6] and [7]. Losses are low and PO is high because the receiver switches only two CMOS transistors within and at specified cycles. To understand the details of this technology, Sections II–III discuss the operation and maximum output power and Sections IV–V compare and assess measured performance.

II. PROPOSED SWITCHED RESONANT HALF-BRIDGE RECEIVER

The basic principle in resonant receivers [6] is that LR resonates with CR at vE’s fO. This way, LR’s current iL and vE are in phase, so vE supplies power across positive and negative half cycles. LR and CR receive and exchange this incoming energy until the switching network drains the tank into vB.

In the receiver proposed in Fig. 2, the ground NMOS transistor MG is normally on. So LR and CR receive and exchange the power that vE continually supplies as PE. As a result, CR’s energy EC or 0.5CRV2C rise from cycle to cycle like Fig. 3 shows. After skipping NS cycles (6 cycles in Fig. 3), MO opens and MG closes for 37.5 ns to partially drain the LRCR tank into vB. MO opens and MG closes
after that. $E_C$ and $v_C$ grow again until the next time $M_O$ and $M_G$ partially drain the tank into $v_B$.

$$P_{O\text{(MAX)'}} = \frac{(0.5v_{E\text{PK}})^2}{2(R_L + R_R)},$$

which happens when $R_{LD}$ matches $R_C + R_R$ where $R_{LD}$ models the power the receiver absorbs, $v_{LD\text{PK}}$ is $R_{LD}$'s peak voltage, and $P_{O\text{(MAX)'}}$ is the maximum power that $L_R$, $R_C$, and $R_R$ avail.

## C. Ideality Index

Delivering $P_{O\text{(MAX)'}}$ is only possible without other losses. Transistors, however, burn power $P_{MR}$ when they conduct and gate-drive power $P_{MG}$ when they switch. Plus, inverters consume shoot-through power $P_{ST}$ when they transition. So the maximum power point (MPP) $P_{O\text{(MPP)}}$ results when added losses $P_{LOSS}$ ($P_{RC}$, $P_{RR}$, $P_{MR}$, $P_{MG}$, and $P_{ST}$) cancel incremental gains in drawn power. Ohmic losses $P_R$ ($P_{RC}$, $P_{RR}$, and $P_{MR}$) climb with output power and driver losses $P_D$ ($P_{MG}$ and $P_{ST}$) rise with transfer frequency. $P_{O\text{(MPP)}}$ is therefore the ideality index $\eta$ fraction of $P_{O\text{(MAX)'}}$ that losses set: $\eta = P_{O\text{(MPP)}}/P_{O\text{(MAX)'}}$. Note that this ideality index $\eta$ hinges on finding the MPP.

## D. Maximum Power Point

The receiver transfers energy packets across a duration $t_B$ and at a rate $f_X$ that the controller in Fig. 2 sets. For $f_X$, the controller determines the number of cycles to skip $N_S$ (in Fig. 3) between energy transfers. So $f_X$ is $f_0$ or a fraction of $f_0$.

To find the MPP, one variable ($f_X$ or $t_B$) is fixed and the other swept to find the local $P_{O\text{(MPP)}}$. Then, with a new fixed value, the other variable is swept and the sequence is repeated to find all other $P_{O\text{(MPP)}}$s (in Fig. 4). After this process, the controller applies the setting that outputs the highest $P_{O\text{(MPP)}}$.

Tracking $P_{O\text{(MPP)}}$ automatically adjusts for separation, alignment, process, and temperature variations.

$$\eta = \frac{f_X}{(N_S + 1)f_0}$$

When $t_B$ in Fig. 4 is 10 ns, output power $P_{O}$ maxes when $f_X$ is 2.6 MHz. However, $P_{O\text{(MPP)}}$ results at 25 ns and 1.2 MHz (and is 580 µW) because losses are lowest at 25 ns and 1.2 MHz. This is 84% ($\eta$) of the 700 µW ($P_{O\text{(MAX)'}}$) that $R_C$ and $R_R$ avail when $f_X$ is 6.78 MHz, $R_R$ at 6.78 MHz is 4.4 Ω, and $v_{E\text{PK}}$ and $R_C$ for 16 mm of separation are 178 mV and 1.4 Ω.

$P_{O\text{(MPP)}}$ is lower when the coils are farther apart because more separation reduces $L_T$: $L_R$'s coupling $k_C$. $P_{O\text{(MPP)}}$ in Fig. 5, for example, is 24 µW at 15 ns and 420 kHz when the coils are 29 mm apart and $R_C$ is 310 mΩ. So the system outputs 59% of the 40 µW that $R_C$ and $R_R$ avail with $v_{E\text{PK}}$'s 39 mV. $t_B$ is lower when farther apart because less power is available, so
the receiver needs less time to transfer power. \( f_X \) is also lower because ohmic and driver losses \( P_R \) and \( P_D \) balance at a lower \( f_X \) when delivering lower power.

Relative to fixing \( f_X \) to \( f_0 \), \( P_{O(MPP)} \) is 1.4× to 3.4× higher when fixing \( f_X \) to 1.2 MHz and adjusting \( t_B \) to \( t_B(MPP) \). This is not much lower than when also adjusting \( f_X \) to \( f_X(MPP) \). Losses are minimal across 16 mm at this \( f_X \) because \( f_X(MPP) \) is 1.2 MHz when \( V_{E(PK)} \) is 178 mV (at 16 mm). Losses, however, overwhelm drawn power at 28 mm when \( f_X \) is 1.2 MHz because \( f_X \) is no longer \( f_X(MPP) \). In other words, harvestable distance increases 1.4× when also adjusting \( f_X \) to \( f_X(MPP) \).

**E. Tuning Accuracy**

Maximum output power hinges on tuning the receiver's resonant frequency to the transmitter's \( f_0 \). This way, \( i_L \)'s and \( v_E \)'s phases match so \( v_E \) always supplies power. A deviation in \( C_R \) reduces the power that \( v_E \) supplies, and as a result, reduces the power that the receiver outputs. A 1-pF offset from 122 pF, for example, reduces \( P_{O(MPP)} \) up to 10% and a 5-pF offset reduces \( P_{O(MPP)} \) up to 75%, as simulations in Fig. 7 show.

Luckily, the controller can compensate for this loss by hastening or delaying transfers. When \( C_R \) is lower than targeted, for example, the tank becomes capacitive, so \( i_L \) lags \( v_E \). Connecting the battery \( v_B \) to the tank sooner with a negative time offset \( t_{OS} \), however, accelerates \( i_L \)'s transition, which allows \( i_L \) to catch up to \( v_E \). Delaying the transfer with a positive \( t_{OS} \) can similarly compensate a higher \( C_R \). This way, \( P_{O(MPP)} \) is 0.5% lower when \( C_R \) is off by 1 pF like Fig. 7 shows and 22% lower when \( C_R \) is off by 5 pF. \( C_R \) in Fig. 2 can therefore be laser-trimmed on chip with ±1-pF accuracy.

**III. PROTOTYPE**

The 180-nm CMOS die in Fig. 8 integrates \( C_R \), \( M_G \) and \( M_O \), the gate drivers, and the dead-time logic in Fig. 2. The board incorporates the packaged die, \( L_R \), and a 100-nF \( v_B \). The transmitter in Fig. 1 is a half-bridge inverter on a separate board. This half-bridge can supply up to 41 mW at 6.78 MHz (\( f_0 \)). The diameters of \( L_T \) and \( L_R \) are 8 mm, so when separated by an adjustable 13- to 38-mm vice, their coupling factor \( k_C \) is 0.09% to 1.1%. \( C_R \) is trimmed with a laser to 122 pF ±1 pF to ensure \( L_R \) and \( C_R \) resonate at 6.78 MHz. An off-chip field-programmable array (FPGA) controls the transmitter and the receiver. This FPGA adjusts \( t_B \) and \( f_X \) in open-loop fashion with interval steps of 5 ns and 53 kHz. For experimental and exploratory purposes, \( t_B \) and \( f_X \) are adjusted manually. A practical implementation of the controller, however, should find and track the maximum power point automatically.

**A. Power Losses**

Losses \( P_{RR} \) in \( R_R \) dominate in Fig. 9 because the diameter of the receiver coil is only 8 mm, so \( R_R \) is high at 4.35 Ω. Power lost \( P_{RC} \) to \( R_C \) is next, especially when the coils are within 18 mm (4.5 radial distances). At such short distances, the
damping effect of the receiver in the transmitter is appreciably more significant. Driver losses \( P_D \) follow because MOS ohmic losses \( P_{MR} \), match (by design) gate-drive losses \( P_{MG} \). So shoot-through losses \( P_{ST} \) raise \( P_D \) above \( P_{MR} \)'s level. The influence of process-, temperature-, and voltage-induced variations in MOS losses on \( P_{OMAX} \) is therefore minimal.

Generally, ohmic losses \( P_R \) in \( P_{RC} \), \( P_{RR} \), and \( P_{MR} \) overwhelm driver losses \( P_D \) when the coils are within 18 mm. \( v_B \) connected periodically behaves like a resistive load because \( i_L \) is nearly sinusoidal. So like a resistive load would, \( P_R \) loses as much power as the load receives at the MPP [12]. At close range, as the receiver skips fewer cycles, \( i_L \) grows less between energy transfers. As a result, the circuit deviates little from the MPP, so \( P_{OMAX} \approx P_{LOSS} \). When the coils separate farther, the circuit skips more cycles. As a result, the circuit deviates more from the MPP, so \( P_{OMAX} \) does not match \( P_{LOSS} \).

For reference, \( P_O \) in Figs. 4–6 and 9–10 is the product of the average current into the battery (which was measured) and the battery's voltage \( v_B \). Ohmic losses in Fig. 9 is derived from measured resistances and currents: \( P_R = i_{RMS}^2R_{EQ} \). Driver losses \( P_D \) were derived from the power supplied and lost to the drivers \( 1 \)–\( 6 \) in Fig. 2. A separate power supply fed the drivers for this purpose: to measure \( P_D \). Since \( v_E \) supplies \( v_B \), ohmic losses, and \( P_D \), sourced power \( P_E \) in Figs. 1–2 is \( P_{OMAX} \) plus \( P_{RR} \), \( P_{MR} \), and \( P_D \). But since the test probes used to measure these parameters also capacitance, measured losses are greater than actual losses by roughly 2–30 \( \mu W \).

B. Harvesting Performance

As Fig. 10 shows, the prototype outputs 70% to 84% of the power that \( R_C \)'s 0–1.9 \( \Omega \) and \( R_R \)'s 4.35 \( \Omega \) avail when the coils are 13 to 28 mm apart. \( P_R \) limits \( \eta_I \) to 70%–84% across this distance. Since \( P_D \) does not scale with power like \( P_R \), \( P_D \)'s influence on \( \eta_I \) is increasingly worse past 28 mm. Decreasing \( t_b \)'s and \( f_X \)'s interval steps should improve \( \eta_I \) across 28–38 mm.

IV. RELATIVE PERFORMANCE

\( P_O \) depends on the source \( v_S \), transmitter's \( R_T \), coil separation \( d_X \) and geometries, \( R_R \), and the receiver. \( k_C \) comprehends the effects of \( d_X \) and coil geometries. \( \eta_I \) compares \( P_{OMAX} \) with the power that \( v_S \), \( R_T \), \( k_C \)'s \( v_E \) and \( R_C \), and \( R_R \) avail. So \( \eta_I \) normalizes receiver performance to nearly all circumstances. This is why \( \eta_I \) is a good metric for comparing power receivers.

In this light, the switched bridge in [9] (in Table I) outputs up to 31% of the power that \( v_E \), \( R_C \), and \( R_R \) avail with \( P_{OMAX} \).

[2] outputs up to 47% because [2] invests battery energy into \( L_R \) so \( i_L \) is on average greater. With a higher \( i_L \), \( v_E \) supplies more power. The switched resonant bridge in [4] can output as much power as [2] because \( C_R \) stores and recycles the investment energy that raises \( i_L \) [6]. The switched resonant half bridge here, however, delivers up to 85% because, with only two switches, losses are lower. Plus, with two degrees of freedom (transfer duration \( t_b \) and rate \( f_X \)), \( P_{OMAX} \) is higher.

[1] integrates on chip a synchronizer that is off chip in [2], [4], [10], and the receiver here. So comparing [1]’s \( \eta_I \) is unfair. But since [1] is basically [2] with a synchronizer, \( \eta_I \) for [1] without the synchronizer should match [2]’s 47%. The switched capacitors in [13]–[14] are also not comparable because they do not require a synchronizer. Still, they use 12–16 capacitors and 16–32 power switches, so they require more silicon area and more power (to charge stray capacitances in on-chip capacitors and switches) than switched inductors [15]. Comparing the resonant bridge in [16] and the voltage doubler in [17] is also unfair because their coil separation is much shorter (at 1 mm) and \( k_C \) is much higher (at 10.5%) than the rest. Although data is missing in [16], conventional resonant bridges require an area- and power-consuming power stage that switched bridges do not [6]. So in all, the receiver here is 38% more efficient than the best comparable counterpart.

The FPGA drains the \( L_RC \) tank as \( C_R \)'s energy crosses zero. For this, the circuit can sense \( C_R \)'s voltage \( v_C \) to ground, which is an indicator of \( C_R \)'s energy 0.5\( C_Rv_C \). Sensing \( v_C \) this way, without interrupting the receiver like [1] does, is a significant improvement over [1] because, to synchronize the system, [1] sacrifices 1.5 of 8.5 cycles. So a synchronizer here should sacrifice less power than [1]’s. Although integrating the controller on chip should not affect the design of the power stage here, silicon area and power efficiency would suffer.

The advantage of the switched bridges in [1]–[2], [10] is that they do not require \( C_R \). Although \( C_R \) in the switched resonant bridge of [5] is 6 \( \mu F \) and off chip, \( C_R \) in [3] is 317 \( \mu F \) and here is 122 \( \mu F \) and on chip. Even with \( C_R \), power density here is 2.845 mW/mm\(^2\) or 6.21\( \times \), 1.33\( \times \), and 1.79\( \times \) greater than [10], [1]–[2]. This is because [10], [1]–[2] use two more power switches and only one degree of freedom when finding \( P_{OMAX} \). As a result, two switches and \( C_R \) here occupy less space than four switches in [1]–[2], [10]. Power density in [3] is higher because, although not reported, available power is also higher, which means switches consume more power. Plus, switched resonant full bridges like [3] use two more power-consuming switches, so they deliver a lower \( \eta_I \) fraction of the power that \( L_R \), \( R_C \), and \( R_R \) avail. Overall, the receiver here
TABLE I: RELATIVE PERFORMANCE

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</tr>
</thead>
<tbody>
<tr>
<td>Tech. 180 nm</td>
<td>180 nm</td>
<td>180 nm</td>
<td>180 nm</td>
<td>180 nm</td>
<td>350 nm</td>
<td>Board</td>
<td>180 nm</td>
<td>180 nm</td>
</tr>
<tr>
<td>$A_{S}$ 12.5 mm$^2$</td>
<td>0.12 mm$^2$</td>
<td>0.49 mm$^2$</td>
<td>0.245 mm$^2$</td>
<td>0.260 mm$^2$</td>
<td>$^3$3 mm$^2$</td>
<td>0.544 mm$^2$</td>
<td>0.471 mm$^2$</td>
<td></td>
</tr>
<tr>
<td>$f_{0}$ 6.78 MHz</td>
<td>13.56 MHz</td>
<td>125 kHz</td>
<td>125 kHz</td>
<td>2.00 MHz</td>
<td>1.00 MHz</td>
<td>50 kHz</td>
<td>6.78 MHz</td>
<td></td>
</tr>
<tr>
<td>$L_{r}$ 400 mm$^2$</td>
<td>707 mm$^2$</td>
<td>41 n$^2$</td>
<td>1.58 µH</td>
<td>12.8 mH</td>
<td>12.8 mH</td>
<td>345 µH</td>
<td>40 µH</td>
<td>0.250 µH</td>
</tr>
<tr>
<td>$R_{r}$ at $f_{0}$</td>
<td>0.55 Ω</td>
<td>110 Ω</td>
<td>110 Ω</td>
<td>1.4 Ω</td>
<td>12 Ω</td>
<td>25 Ω</td>
<td>7.1 Ω</td>
<td>5.0 Ω</td>
</tr>
<tr>
<td>$L_{b}$ 400 mm$^2$</td>
<td>380 mm$^2$</td>
<td>107 mm$^3$</td>
<td>107 mm$^3$</td>
<td>107 mm$^3$</td>
<td>3320 mm$^3$</td>
<td>707 mm$^3$</td>
<td>54.1 mm$^3$</td>
<td></td>
</tr>
<tr>
<td>$R_{b}$ at $f_{0}$</td>
<td>0.14 Ω</td>
<td>9.7 Ω</td>
<td>9.7 Ω</td>
<td>9.7 Ω</td>
<td>6.1 Ω</td>
<td>0.95 Ω</td>
<td>0.11 &amp; 0.13 Ω</td>
<td>4.4 Ω</td>
</tr>
<tr>
<td>$d_{s}$</td>
<td>1 mm</td>
<td>0–10.6 mm</td>
<td>10–50 mm</td>
<td>80 mm</td>
<td>70 mm</td>
<td>85 mm</td>
<td>13–38 mm</td>
<td></td>
</tr>
<tr>
<td>$k_{C}$</td>
<td>10.5%</td>
<td>0.59%–6.7%</td>
<td>0.9%–7.6%</td>
<td>5%</td>
<td>1.3%$^b$</td>
<td>0.09%–1.1%$^b$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table entries include:

- $v_{E(PK)}$ includes RCs' voltage so $P_{O(MAX)}$ includes pessimistic $v_{E}$.
- $v_{S}$, $v_{E}$, RT, and RR include projections from LR's quality factor.
- $P_{O(MPP)}$ is pessimistic if $v_{C}$, $v_{E}$, and $v_{R}$ are not included.
- $P_{O(MPP)}$ includes $R_{c}$'s voltage so $P_{O(MAX)}$ includes pessimistic $v_{C}$.
- $P_{O(MPP)}$ includes $R_{c}$'s voltage so $P_{O(MAX)}$ includes pessimistic $R_{c}$.

*Estimate for rectifier only.*