180-nm 85%-Efficient Inductively Coupled Switched Resonant Half-Bridge Power Receiver

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***Abstract*—Receiver coils in embedded microsensors are small and their transmitters are unpredictably distant and misaligned, so available power is low and variable. The 180-nm, 6.78-MHz switched resonant half bridge here, however, only uses two transistors with a transfer rate and duration that are both adjustable. This way, the prototype outputs 13%–85% of the 9.7–1580 µW that a 54.1-mm^2 receiver coil avails when 13 to 38 mm apart from its source. This is up to 38% more power and with 25% smaller footprint than the best comparable receiver.**

***Index Terms*—Inductively coupled power receiver, switched resonant half bridge, weakly coupled charger, wireless power.**

I. Powering Microsystems Inductively

Structurally embedded microsensors and biomedical implants can sense, process, and transmit data that save energy, money, and lives. Embedded applications normally require smart, small, and immobile sensors that do not receive light. Meeting these demands is challenging because, with so much functionality, sensors easily drain their small onboard batteries. Since motion and light energy are absent and temperature gradients are so low that thermal energy is almost as absent, coupling power inductively like Fig. 1 shows is often the only viable means of powering these devices [1].

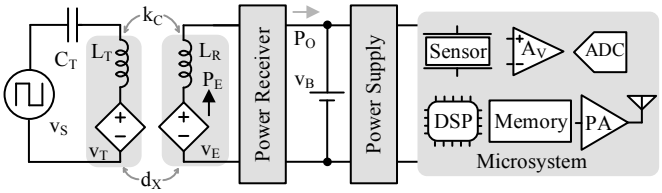

Fig. 1. Inductively powered microsystem.

The transmitting coil L_T and capacitor C_T resonate at the operating frequency f_O of the source v_S. The alternating magnetic field that L_T emanates induces a current in the nearby receiver coil L_R that the power receiver can harness and use to recharge a battery v_B and supply a system. The power supply draws and feeds power on demand to the sensors, amplifiers (A_V), data converters (ADC), digital-signal processors (DSP), and power amplifiers (PA) in the system.

Small receiver coils in embedded applications are usually several radial distances away from their transmitter coils [1]–[5]. L_R therefore harnesses a small fraction of the power that L_T avails [1]–[2], [4]. As a result, L_R normally under-damps its transmitting source v_S. With so little power available, optimal maximum power-point (MPP) operation is vital [6].

Under-damping v_S means that the electromotive force (EMF) voltage v_E induced in L_R is capable of supplying more power P_E. This is why resonant receivers are popular in this space, because exchanging more energy between L_R and a resonating capacitor C_R raises the current i_L with which L_R draws P_E from v_E [6]. But since L_R's series resistance R_R and transistors consume more power with higher i_L, power losses limit how much of P_E the receiver can output with P_O.

The switched resonant half-bridge power receiver presented here is largely the result of theory presented in [6] and [7]. Losses are low and P_O is high because the receiver switches only two CMOS transistors within and at specified cycles. To understand the details of this technology, Sections II–III discuss the operation and maximum output power and Sections IV–V compare and assess measured performance.

II. Proposed Switched Resonant Half-Bridge Receiver

The basic principle in resonant receivers [6] is that L_R resonates with C_R at v_E's f_O. This way, L_R's current i_L and v_E are in phase, so v_E supplies power across positive and negative half cycles. L_R and C_R receive and exchange this incoming energy until the switching network drains the tank into v_B.

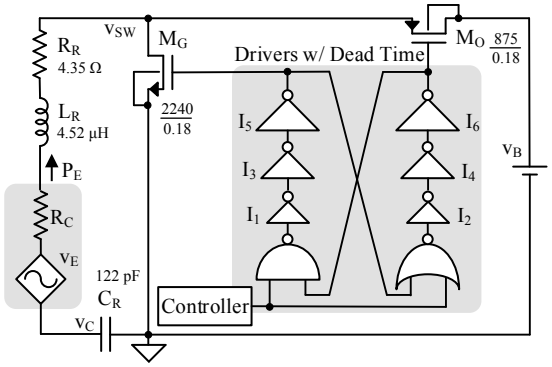

Fig. 2. Switched resonant half-bridge power receiver proposed.

In the receiver proposed in Fig. 2, the ground NMOS transistor M_G is normally on. So L_R and C_R receive and exchange the power that v_E continually supplies as P_E. As a result, C_R's energy E_C or $0.5C_Rv_C^2$ and voltage v_C rise from cycle to cycle like Fig. 3 shows. After skipping N_S cycles (6 cycles in Fig. 3), M_G opens and M_O closes for 37.5 ns to partially drain the L_RC_R tank into v_B. M_O opens and M_G closes

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after that. E_C and v_C grow again until the next time M_O and M_G partially drain the tank into v_B.

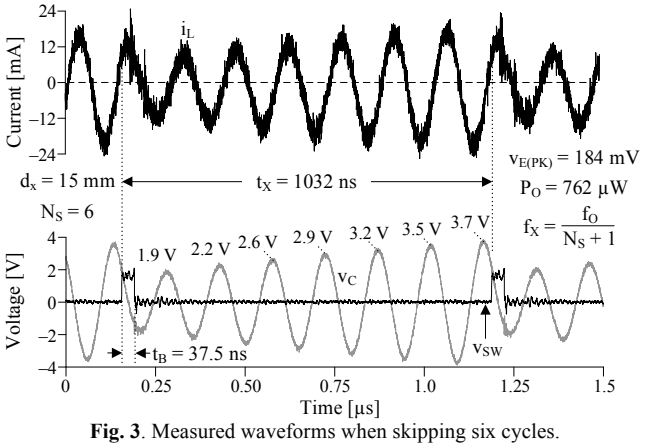

Fig. 3. Measured waveforms when skipping six cycles.

A. Design

M_G and M_O require gate-drive power P_{MG} to switch between states. They also burn ohmic power P_{MR} when they conduct i_L. Since MOS resistance R_{DS} and gate capacitance C_G rise with channel length, M_G's and M_O's channel lengths are minimum length: 180 nm. But since R_{DS} falls and C_G rises with channel width, M_G's and M_O's widths 875 and 2240 µm balance P_{MR} and P_{MG} when the receiver outputs 300 µW. This is the most probable power level for the blood-pressure monitors and glucose sensors targeted here [8]. Optimizing M_G and M_O for the most likely setting saves (over time) the most energy.

The logic inserts dead time between M_G's and M_O's conduction periods to keep M_O and M_G from inadvertently draining v_B to ground. One minimum-sized gate and three inverters with transistors of increasing dimensions drive M_G and M_O. I_1 and I_2 are 2× larger than NAND and NOR gates, I_3 and I_4 are 4× larger than I_1 and I_2, and I_5 and I_6 are 4× larger than I_3 and I_4. Although 3× is the optimal gain for shortest propagation delay, a higher gain reduces the number of inverter stages and the shoot-through power they consume [9].

The controller determines when to draw energy from the L_RC_R tank into v_B. It basically dictates when, how long, and how often M_O should drain L_R. To deliver as much power as possible in the shortest time, M_O steers L_R's *peak* current (at 200 ns) into v_B. Since L_R's energy E_L and current i_L peak when C_R's energy E_C and voltage v_C are zero, the controller bleeds L_R as v_C crosses zero. The duration t_B and frequency f_X of these energy transfers depend on how much power L_R avails.

B. Available Power

The transmitter's resistance R_T limits how much current and power the source v_S can supply. Separation d_X and geometries of the coils then determine (via coupling factor k_C) what fraction of that power couples to L_R in the form of v_E. Although over-damping v_S is possible, d_X is so high and L_R is so small that only a small fraction of what the transmitter can supply loads v_S [6]. v_E is therefore low at hundreds of mV's.

With millimeter geometries, L_R's resistance R_R is high at 1–10 Ω [1]–[4], [10]. Such a high R_R often overwhelms L_T's coupled (reflected) resistance R_C in L_R [11] and limits the current and power that v_E supplies to a level that hardly ever over-damps v_S. So the maximum power $P_{O(MAX)}'$ that a sinusoidal v_E (with peak $v_{E(PK)}$) can supply a load R_{LD} is

$$P_{O(MAX)}' = \frac{v_{LD(PK)}^{\ 2}}{2R_{LD}} \equiv \frac{\left(0.5v_{E(PK)}\right)^2}{2\left(R_C + R_R\right)}, \quad (1)$$

which happens when R_{LD} matches $R_C + R_R$ where R_{LD} models the power the receiver absorbs, $v_{LD(PK)}$ is R_{LD}'s peak voltage, and $P_{O(MAX)}'$ is the maximum power that L_R, R_C, and R_R avail.

C. Ideality Index

Delivering $P_{O(MAX)}'$ is only possible without other losses. Transistors, however, burn power P_{MR} when they conduct and gate-drive power P_{MG} when they switch. Plus, inverters consume shoot-through power P_{ST} when they transition. So the maximum power point (MPP) $P_{O(MPP)}$ results when added losses P_{LOSS} (R_C's P_{RC}, R_R's P_{RR}, P_{MR}, P_{MG}, and P_{ST}) cancel incremental gains in drawn power. Ohmic losses P_R (P_{RC}, P_{RR}, and P_{MR}) climb with output power and driver losses P_D (P_{MG} and P_{ST}) rise with transfer frequency. $P_{O(MPP)}$ is therefore the η_I fraction of $P_{O(MAX)}'$ that losses set: $\eta_I \equiv P_{O(MPP)}/P_{O(MAX)}'$. Note that this ideality index η_I hinges on finding the MPP.

D. Maximum Power Point

The receiver transfers energy packets across a duration t_B and at a rate f_X that the controller in Fig. 2 sets. For f_X, the controller determines the number of cycles to skip N_S (in Fig. 3) between energy transfers. So f_X is f_O or a fraction of f_O.

To find the MPP, one variable (f_X or t_B) is fixed and the other swept to find the local $P_{O(MPP)}$. Then, with a new fixed value, the other variable is swept and the sequence is repeated to find all other $P_{O(MPP)}$'s (in Fig. 4). After this process, the controller applies the setting that outputs the highest $P_{O(MPP)}$. Tracking $P_{O(MPP)}$ automatically adjusts for separation, alignment, process, and temperature variations.

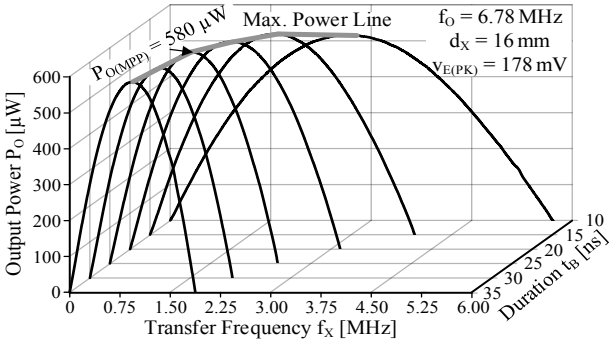

Fig. 4. Measured output-power space when the coils are 16 mm apart.

When t_B in Fig. 4 is 10 ns, output power P_O maxes when f_X is 2.6 MHz. However, $P_{O(MPP)}$ results at 25 ns and 1.2 MHz (and is 580 µW) because losses are lowest at 25 ns and 1.2 MHz. This is 84% (η_I) of the 700 µW ($P_{O(MAX)}'$) that R_C and R_R avail when f_O is 6.78 MHz, R_R at 6.78 MHz is 4.4 Ω, and $v_{E(PK)}$ and R_C for 16 mm of separation are 178 mV and 1.4 Ω.

$P_{O(MPP)}$ is lower when the coils are farther apart because more separation reduces L_T:L_R's coupling k_C. $P_{O(MPP)}$ in Fig. 5, for example, is 24 µW at 15 ns and 420 kHz when the coils are 29 mm apart and R_C is 310 mΩ. So the system outputs 59% of the 40 µW that R_C and R_R avail with $v_{E(PK)}$'s 39 mV. t_B is lower when farther apart because less power is available, so

the receiver needs less time to transfer power. f_X is also lower because ohmic and driver losses P_R and P_D balance at a lower f_X when delivering lower power.

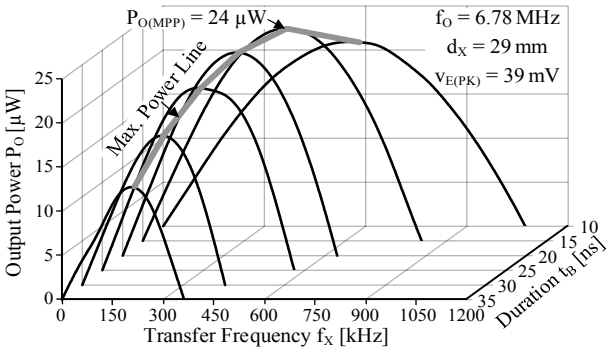

Fig. 5. Measured output-power space when the coils are 29 mm apart.

The two-variable space in Figs. 4 and 5 captures more settings than a single variable can. With more settings, $P_{O(MPP)}$ can be closer to what R_C and R_R can avail with $P_{O(MAX)}$'. In Fig. 6, below 17 mm, $P_{O(MPP)}$ is 1.5× to 3.6× higher than when fixing f_X to v_E's 6.78 MHz and adjusting t_B to t_B's maximum power point $t_{B(MPP)}$. By adjusting both t_B and f_X, the system extends harvestable distance 2.1× from 18 to 38 mm.

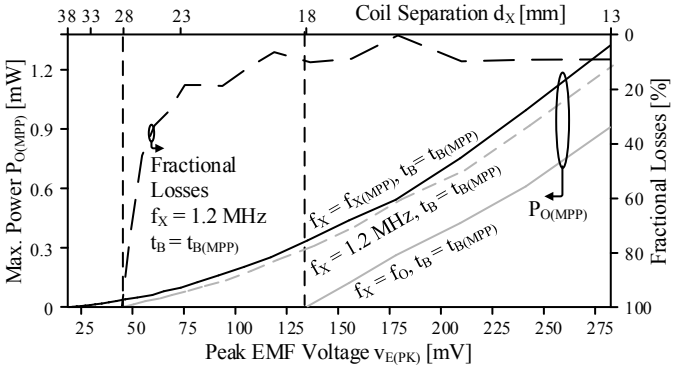

Fig. 6. Measured maximum power when adjusting one and two variables.

Relative to fixing f_X to f_O, $P_{O(MPP)}$ is 1.4× to 3.4× higher when fixing f_X to 1.2 MHz and adjusting t_B to $t_{B(MPP)}$. This is not much lower than when also adjusting f_X to $f_{X(MPP)}$. Losses are minimal across 16 mm at this f_X because $f_{X(MPP)}$ is 1.2 MHz when $v_{E(PK)}$ is 178 mV (at 16 mm). Losses, however, overwhelm drawn power at 28 mm when f_X is 1.2 MHz because f_X is no longer $f_{X(MPP)}$. In other words, harvestable distance increases 1.4× when also adjusting f_X to $f_{X(MPP)}$.

E. Tuning Accuracy

Maximum output power hinges on tuning the receiver's resonant frequency to the transmitter's f_O. This way, i_L's and v_E's phases match so v_E always supplies power. A deviation in C_R reduces the power that v_E supplies, and as a result, reduces the power that the receiver outputs. A 1-pF offset from 122 pF, for example, reduces $P_{O(MPP)}$ up to 10% and a 5-pF offset reduces $P_{O(MPP)}$ up to 75%, as simulations in Fig. 7 show.

Luckily, the controller can compensate for this loss by hastening or delaying transfers. When C_R is lower than targeted, for example, the tank becomes capacitive, so i_L lags v_E. Connecting the battery v_B to the tank sooner with a negative time offset t_{OS}, however, accelerates i_L's transition, which allows i_L to catch up to v_E. Delaying the transfer with a positive t_{OS} can similarly compensate a higher C_R. This way, $P_{O(MPP)}$ is 0.5% lower when C_R is off by 1 pF like Fig. 7 shows and 22% lower when C_R is off by 5 pF. C_R in Fig. 2 can therefore be laser-trimmed on chip with ±1-pF accuracy.

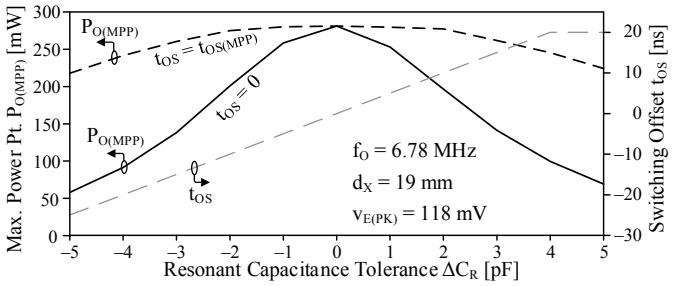

Fig. 7. Simulated sensitivity of output power to tuning accuracy.

III. PROTOTYPE

The 180-nm CMOS die in Fig. 8 integrates C_R, M_G and M_O, the gate drivers, and the dead-time logic in Fig. 2. The board incorporates the packaged die, L_R, and a 100-nF v_B. The transmitter in Fig. 1 is a half-bridge inverter on a separate board. This half-bridge can supply up to 41 mW at 6.78 MHz (f_O). The diameters of L_T and L_R are 8 mm, so when separated by an adjustable 13- to 38-mm vice, their coupling factor k_C is 0.09% to 1.1%. C_R is trimmed with a laser to 122 pF ±1 pF to ensure L_R and C_R resonate at 6.78 MHz. An off-chip field-programmable array (FPGA) controls the transmitter and the receiver. This FPGA adjusts t_B and f_X in open-loop fashion with interval steps of 5 ns and 53 kHz. For experimental and exploratory purposes, t_B and f_X are adjusted manually. A practical implementation of the controller, however, should find and track the maximum power point automatically.

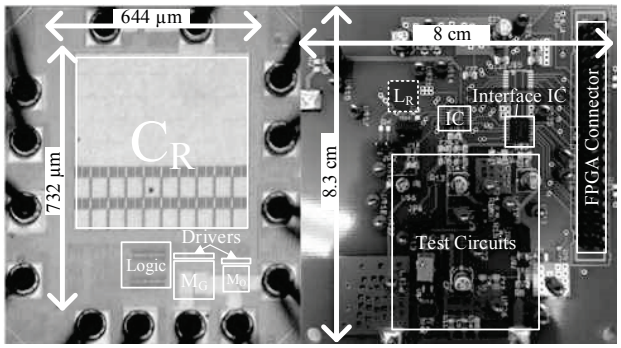

Fig. 8. Photographs of the 180-nm die and board prototyped.

Since v_E is the unloaded EMF voltage induced in L_R, v_E is the open-circuit voltage across L_R. R_C models the receiver's damping effect on the transmitter's reflected source v_E [11]. So when short-circuiting v_E and R_C, R_C consumes the same power that v_S supplies when the transmitter is unloaded. $v_{E(PK)}$ and R_C in measurements are therefore L_R's peak open-circuit voltage and the equivalent resistance that burns v_S's power when the transmitter is unloaded.

A. Power Losses

Losses P_{RR} in R_R dominate in Fig. 9 because the diameter of the receiver coil is only 8 mm, so R_R is high at 4.35 Ω. Power lost P_{RC} to R_C is next, especially when the coils are within 18 mm (4.5 radial distances). At such short distances, the

damping effect of the receiver in the transmitter is appreciably more significant. Driver losses P_D follow because MOS ohmic losses P_{MR} match (by design) gate-drive losses P_{MG}. So shoot-through losses P_{ST} raise P_D above P_{MR}'s level. The influence of process-, temperature-, and voltage-induced variations in MOS losses on $P_{O(MPP)}$ is therefore minimal.

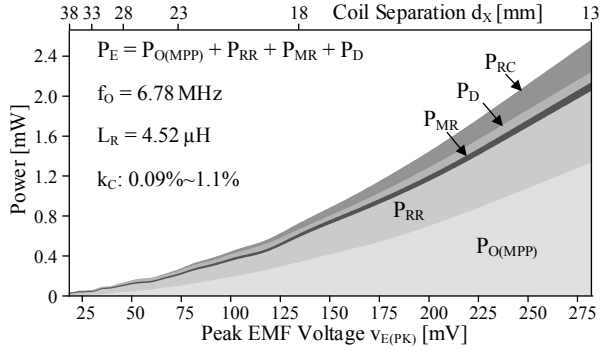

Fig. 9. Measured losses and resulting maximum power.

Generally, ohmic losses P_R in P_{RC}, P_{RR}, and P_{MR} overwhelm driver losses P_D when the coils are within 18 mm. v_B connected periodically behaves like a resistive load because i_L is nearly sinusoidal. So like a resistive load would, P_R loses as much power as the load receives at the MPP [12]. At close range, as the receiver skips fewer cycles, i_L grows less between energy transfers. As a result, the circuit deviates little from the MPP, so $P_{O(MPP)} \approx P_{LOSS}$. When the coils separate farther, the circuit skips more cycles. As a result, the circuit deviates more from the MPP, so $P_{O(MPP)}$ does not match P_{LOSS}.

For reference, P_O in Figs. 4–6 and 9–10 is the product of the average current into the battery (which was measured) and the battery's voltage v_B. Ohmic losses in Fig. 9 is derived from measured resistances and currents: $P_R = i_{RMS}^2 R_{EQ}$. Driver losses P_D were derived from the power supplied and lost to the drivers I_1–I_6 in Fig. 2. A separate power supply fed the drivers for this purpose: to measure P_D. Since v_E supplies v_B, ohmic losses, and P_D, sourced power P_E in Figs. 1–2 is $P_{O(MPP)}$ plus P_{RR}, P_{MR}, and P_D. But since the test probes used to measure these parameters add capacitance, *measured* losses are greater than *actual* losses by roughly 2–30 µW.

B. Harvesting Performance

As Fig. 10 shows, the prototype outputs 70% to 84% of the power that R_C's 0–1.9 Ω and R_R's 4.35 Ω avail when the coils are 13 to 28 mm apart. P_R limits η_I to 70%–84% across this distance. Since P_D does not scale with power like P_R, P_D's influence on η_I is increasingly worse past 28 mm. Decreasing t_B's and f_X's interval steps should improve η_I across 28–38 mm.

IV. Relative Performance

P_O depends on the source v_S, transmitter's R_T, coil separation d_X and geometries, R_R, and the receiver. k_C comprehends the effects of d_X and coil geometries. η_I compares $P_{O(MPP)}$ with the power that v_S, R_T, k_C's v_E and R_C, and R_R avail. So η_I normalizes receiver performance to nearly all circumstances. This is why η_I is a good metric for comparing power receivers.

In this light, the switched bridge in [9] (in Table I) outputs up to 31% of the power that v_E, R_C, and R_R avail with $P_{O(MAX)}'$. [2] outputs up to 47% because [2] invests battery energy into L_R so i_L is on average greater. With a higher i_L, v_E supplies more power. The switched resonant bridge in [4] can output as much power as [2] because C_R stores and recycles the investment energy that raises i_L [6]. The switched resonant half bridge here, however, delivers up to 85% because, with only two switches, losses are lower. Plus, with two degrees of freedom (transfer duration t_B and rate f_X), $P_{O(MPP)}$ is higher.

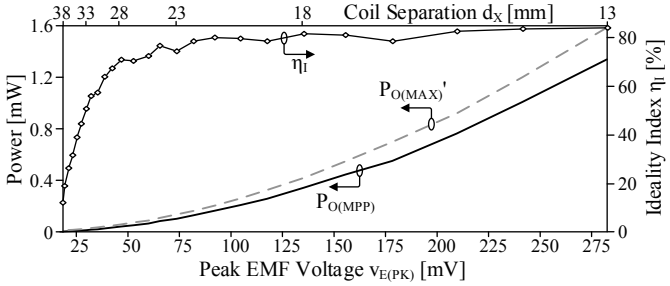

Fig. 10. Available and measured output power and resulting ideality index.

[1] integrates on chip a synchronizer that is off chip in [2], [4], [10], and the receiver here. So comparing [1]'s η_I is unfair. But since [1] is basically [2] with a synchronizer, η_I for [1] without the synchronizer should match [2]'s 47%. The switched capacitors in [13]–[14] are also not comparable because they do not require a synchronizer. Still, they use 12–16 capacitors and 16–32 power switches, so they require more silicon area and more power (to charge stray capacitances in on-chip capacitors and switches) than switched inductors [15]. Comparing the resonant bridge in [16] and the voltage doubler in [17] is also unfair because their coil separation is much shorter (at 1 mm) and k_C is much higher (at 10.5%) than the rest. Although data is missing in [16], conventional resonant bridges require an area- and power-consuming power stage that switched bridges do not [6]. So in all, the receiver here is 38% more efficient than the best comparable counterpart.

The FPGA drains the L_RC_R tank as C_R's energy crosses zero. For this, the circuit can sense C_R's voltage v_C to ground, which is an indicator of C_R's energy $0.5C_Rv_C^2$. Sensing v_C this way, without interrupting the receiver like [1] does, is a significant improvement over [1] because, to synchronize the system, [1] sacrifices 1.5 of 8.5 cycles. So a synchronizer here should sacrifice less power than [1]'s. Although integrating the controller on chip should not affect the design of the power stage here, silicon area and power efficiency would suffer.

The advantage of the switched bridges in [1]–[2], [10] is that they do not require C_R. Although C_R in the switched resonant bridge of [5] is 6 nF and off chip, C_R in [3] is 317 pF and here is 122 pF and on chip. Even with C_R, power density here is 2.845 mW/mm^2 or 6.21×, 1.33×, and 1.79× greater than [10], [1]–[2]. This is because [10], [1]–[2] use two more power switches and only one degree of freedom when finding $P_{O(MPP)}$. As a result, two switches and C_R here occupy less space than four switches in [1]–[2], [10]. Power density in [3] is higher because, although not reported, available power is also higher, which means switches consume more power. Plus, switched resonant full bridges like [3] use two more power-consuming switches, so they deliver a lower η_I fraction of the power that L_R, R_C, and R_R avail. Overall, the receiver here

TABLE I: RELATIVE PERFORMANCE

	JSSC [17]	JSSC [16]	JSSC [10]	TCAS II [2]	JESTPE [1]	JSSC [3]	TCAS I [4]	JSSC [5]	This Work
	Volt. Doubler	Res. Brdg.	Switched Bridge			Sw. Res. Brdg.	Switched Resonant Half Bridge		
Tech.	180 nm	180 nm	180 nm	180 nm	180 nm	350 nm	Board	180 nm	180 nm
A_{SI}	12.5 mm^2	0.12 mm^2	0.490 mm^2	0.245 mm^2	0.260 mm^2	[A]3 mm^2	–	0.544 mm^2	0.471 mm^2
f_O	6.78 MHz	13.56 MHz	125 kHz	125 kHz	125 kHz	2.00 MHz	1.00 MHz	50 kHz	6.78 MHz
L_T	400 mm^2	707 mm^2				15400 mm^2	22700 mm^2		54.1 mm^2
	41 nH	1.58 µH	12.8 mH	12.8 mH	345 µH	40 µH	250 µH	7.2 mH	4.6 µH
R_T at f_O		0.55 Ω	110 Ω	110 Ω	1.4 Ω	12 Ω	25 Ω	7.1 Ω	5.0 Ω
L_R	400 mm^2	380 mm^2	107 mm^3	107 mm^3	107 mm^3	3320 mm^2	707 mm^2	107 mm^3	54.1 mm^2
	2.58 µH	265 nH	400 µH	400 µH	400 µH	20 µH	4.4 µH	6.5 µH	4.5 µH
R_R at f_O		0.14 Ω	9.7 Ω	9.7 Ω	9.7 Ω	6.1 Ω	0.95 Ω	0.11 & 0.13 Ω	4.4 Ω
d_X	1 mm		0–10.6 mm		10–50 mm	80 mm	70 mm	85 mm	13–38 mm
k_C		10.5%	0.59%–6.7%	0.9%–7.6%		5%	1.3%[A]		0.09%–1.1%[B]
R_C			0.18–16 Ω[C]	0.23–25 Ω[C]	0.04–3.7 Ω[C]				0–1.9 Ω[C]
$v_{E(PK)}$			39.5–386 mV	46–480 mV	66–585 mV		41 mV[D]		18.5–282 mV[B]
$P_{O(MAX)}$'			19.7–724 µW	26.6–830 µW	55.9–3190 µW		224 µW[D]		9.72–1580 µW
$P_{O(MPP)}$	1 W	40 mW	0–224 µW	8–390 µW	16–557 µW	1.45 W	96.1 µW	0–2.84 µW	1.2–1340 µW
η_I			0%–30.9%	29.6%–46.9%	17.5%–28.6%		42.9%		12.3%–84.8%
$P_{O(MPP)}/A_{SI}$	80 mW/mm^2	333 mW/mm^2	0.457 mW/mm^2	1.59 mW/mm^2	2.14 mW/mm^2	483 mW/mm^2		5.22 µW/mm^2	2.84 mW/mm^2
Parts	L_R, C_R, 4 FETs	L_R, C_R, 4 FETs	L_R, 4 FETs	L_R, 4 FETs	L_R, 4 FETs	L_R, C_R, 5 FETs	L_R, C_R, 1 FET, 1 Diode	L_R, C_R, 2 FETs	L_R, C_R, 2 FETs

[A]Estimate for rectifier only. [B]Projections from L_R's quality factor. [C]Calculated from v_S, v_E, R_T, and R_R. [D]$v_{E(PK)}$ includes R_C's voltage so $P_{O(MAX)}$' is pessimistic.

outputs 38% more power with 25% smaller footprint.

[4]–[5] and this system are the most compact because only C_R and two switches are necessary. [4], however, uses a diode for one of the switches, only adjusts f_X, drains the tank entirely each time it transfers, and is a board implementation, so power density is much lower and losses are higher. The switches in [5] connect L_R to v_B or C_R. Since C_R exposes the switches to C_R's v_C, v_C cannot surpass the switches' breakdown level V_{BD}. The switches in Fig. 2 and in [4], however, connect L_R and C_R to v_B or ground, so V_{BD} does not limit v_C. If v_E, R_C, and R_R can avail more power, v_C can therefore rise (so that a higher i_L can draw this power). This is why the power range for the receiver proposed is vast and wider at 1.2–1340 µW than the others'.

V. CONCLUSIONS

The 180-nm, 6.78-MHz switched resonant half-bridge power receiver presented here outputs 1.2–1340 µW of the 9.72–1580 µW that a 54.1-mm^2 receiver coil with 4.35 Ω avails when 13 to 38 mm apart from the 54.1-mm^2 transmitter coil. The system delivers 38% more power with 25% smaller footprint than the best comparable receiver. Transferring this much and this range of power is important because structurally embedded microsensors are small, immobile, distant, and often misaligned with their transmitting sources.

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