Drawing the Most Power from Low-Cost Single-Well 1-mm^2 CMOS Photovoltaic Cells

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***Abstract*—PV cells can generate 100× more power from light than other transducers can from motion, radiation, and heat. Although custom multi-junction non-silicon and multi-well CMOS cells output more power, single-well process technologies cost less. Amorphous cells cost even less, but output less power. But with only a small window of light available, tiny CMOS cells output little. This paper explores and proposes open-terminal single-well CMOS PV cell configurations that output more power than competing low-cost CMOS cells in literature. Measurements with 0.35-µm 1 × 1-mm^2 single-well CMOS cells show that deeper and lighter doped junctions generate higher power than shallower junctions and double-junction configurations output even higher power. This is why sunlight on N$^+$ in P substrate and N well in P substrate cells outputs 6 and 98 µW and on shorted and open-terminal P$^+$ in N well in P substrate structures outputs 132 µW. Opening the P$^+$ terminal outputs even more power because P$^+$ metal, which blocks light, is no longer necessary.**

***Index Terms*—Wireless microsensors, ambient light, energy harvesters, low-cost single-well CMOS photovoltaic (PV) cells.**

I. CMOS Photovoltaic Systems

Wireless microsensors can monitor, process, and report information in small and large infrastructures like hospitals, homes, and factories that can save lives, energy, and money [1]. And for this, nowadays, they only need microwatts [1]. The challenge is that their tiny batteries deplete easily, so lifetimes are short. But since ambient energy is vast, small harvesters can supplement and recharge these exhaustible batteries, and in the process, extend their lifetimes.

Of possible alternatives, photovoltaic (PV) cells can at 100–400 µW/mm^2 output over 100× more power from sunlight than piezoelectric, electrostatic, and electromagnetic transducers, antennae, thermoelectric piles can from motion, radiation, and heat [1]–[2]. Although amorphous silicon costs less than crystalline single-well complementary metal–oxide–semiconductor (CMOS) [3], single-cell CMOS cells generate 10%–13% higher power. Multi-well CMOS junctions generate more power than single-well junctions [4]–[5], but require additional steps in the fabrication process, so they cost more [6]. Custom mono-crystalline cells output as much as single-well cells and custom multi-junction non-silicon cells can output 10%–15% more [7]–[9], but investing to establish and maintain a custom fabrication facility is not always possible.

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Still, tiny cells capture a small fraction of the incoming light, and CMOS cells only output 15%–25% of the light power they receive. This is why using the CMOS PV cell configuration that produces the most power is so important. This way, the PV cell in Fig. 1 can supply the load with the least assistance from the battery C_{BAT}. And when the cell outputs more power than the load requires, the system can recharge C_{BAT} with the maximum possible excess power.

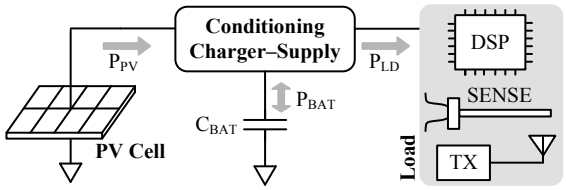

Fig. 1. Typical CMOS photovoltaic system.

This paper introduces single-well open-terminal double-junction CMOS PV-cell configurations absent in literature and compares them with conventional structures from the same process technology. To establish a common groundwork, Section II first reviews how CMOS cells generate charge and lose power. Section III then describes and evaluates all possible single-well CMOS configurations. Sections IV and V end the paper by assessing and comparing the cells.

II. Photovoltaic P–N Junction Cells

A. Generation of Photonic Current

A CMOS PV cell is essentially a P–N junction, so immersing N- into P- or P- into N-type semiconductor regions like Fig. 2a illustrates is the basic recipe for building cells. The sharp charge-carrier concentration gradients across the junction cause electrons and holes to migrate into the opposing regions. This diffusion process depletes parent atoms near the junction of charge carriers. The immobile atoms therefore ionize and impose a *built-in* electric field E_{PN} across the depletion region. In steady state, E_{PN} induces a drift current that is equal and opposite to the diffusion current that produced E_{PN} in the first place. As a result, net current flow is zero.

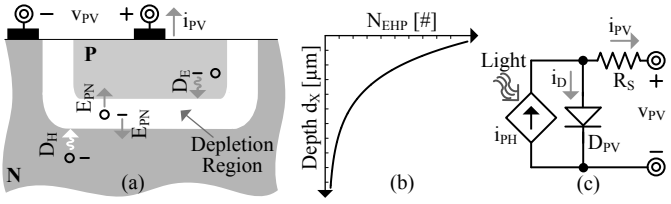

Fig. 2. PV P–N junction (a) profile, (b) carrier concentration, and (c) model.

When light passes through the semiconductor material, photons excite loosely bound electrons with sufficient energy

to break them away from their home sites. Under the influence of E_{PN}, liberated electron–hole pairs (EHPs) in the depletion region separate and drift in opposite directions: holes to the P side and electrons to the N side. The net result is the photonic current i_{PH} shown in Fig. 2c. Because wider depletion regions collect more EHPs, higher depletion widths W_D raise i_{PH}.

Minority electrons liberated in the P side and minority holes liberated in the N side diffuse, on average, one diffusion-length L_E or L_H before recombining with majority carriers. This means, a fraction of EHPs liberated within L_E and L_H of the depletion boundaries of the junction reach the depletion space to add to i_{PH}. Farther-away EHPs recombine, so they do not contribute to i_{PH}. In other words, longer diffusion lengths L_E and L_H aid the generation process.

Because the material absorbs light energy, light intensity is greatest near the exposed surface. Photons therefore liberate more EHPs near the surface than deeper in the material. In fact, EHP concentration N_{EHP} falls exponentially with depth, as Fig. 2b shows. And when wavelengths are short, light does not penetrate the material as far, so N_{EHP} is higher near the surface and penetration depth is shallower [10]. All this means, depletion regions near the surface collect and generate more i_{PH}, especially when wavelengths are short.

B. Loss Mechanisms

Liberating EHPs is how P–N junctions convert light energy into the electrical domain, and collecting and steering them to the load is how they output power. The first loss in this process is the fraction of light energy lost to heat. Blocked and reflected light, ohmic power, uncollected EHPs, and collected EHPs lost are other losses. This is why conversion efficiency, which is the fraction of input light power that reaches the load, is normally low at 15%–20% [8]–[12].

Shading: Standard semiconductor technologies diffuse and implant dopants into a silicon substrate to define N- and P-type regions and deposit metal layers above the regions to interconnect them. Unfortunately, these same metal layers shield a cell from incoming light, so the exposed window is smaller than the actual cell. Blocked light is therefore a loss.

Ohmic Loss: The semiconductor and metallic links that connect the edges of the depletion region to the load impose series resistance R_S to PV current i_{PV}. So when i_{PV} flows, R_S burns power. Although adding metal and raising doping concentrations reduce resistance, more metal blocks light and more majority carriers shorten diffusion length. This means, ohmic losses fall as shading losses and uncollected EHPs rise.

Uncollected EHPs: Liberated minority carriers that recombine with majority carriers constitute a loss to photonic current i_{PH}. Because higher doping concentrations raise the number of majority carriers with which minority carriers can recombine, EHPs in highly doped regions diffuse less. And with shorter diffusion lengths, less EHPs reach the depletion region. So higher donor and acceptor doping concentrations N_D and N_A in the N- and P-type regions generate less i_{PH}.

Irregularities on the surface can also trap liberated EHPs long enough for EHPs to recombine [13]. Filling the gaps with dopant atoms can reduce this loss, but not without supplying majority carriers near the surface. So heavily doped surfaces help only when the loss to traps is more severe than the loss to majority carriers near the surface.

Diode Leakage: As just described, PV output current i_{PV} in Figs. 2a and 2c flows out of the cell and into a load, so the voltage across the load and the cell v_{PV} is positive. This means, the P–N junction that generates i_{PH} forward-biases, and the diode D_{PV} in the junction steers a fraction of i_{PH} away from the load to ground. Leaked power climbs with higher doping concentrations N_A and N_D because they strengthen the diode.

C. Maximum Output Power

For a given light, photonic current i_{PH} delivers more power P_{PH} when the voltage across the cell v_{PV} is higher. Unfortunately, the same is true for the power lost in the diode P_D. But since P_{PH} rises linearly and P_D rises exponentially with v_{PV}, gains first outpace losses when a low v_{PV} rises and losses then outpace gains when a high v_{PV} rises. So like Fig. 3 shows, output power P_{PV} rises with v_{PV} when v_{PV} is low and falls when v_{PV} is high. The maximum power point (MPP) $P_{PV(MPP)}$ results when the rise in losses cancels the rise in gains, at the optimum PV voltage $v_{PV(OPT)}$ for that particular light setting.

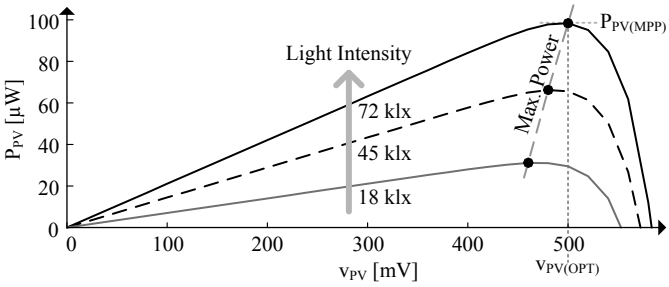

Fig. 3. Measured PV power across PV voltage for several light levels.

III. CMOS CELLS

Standard low-cost CMOS technologies normally incorporate no more than shallow N^+ and P^+ diffusions for the source, drain, and bulk terminals of NFETs and PFETs and a deeper N well to isolate PFETs from the P substrate [11]–[14]. Although doping concentrations are not always the same, N^+ and P^+ are always more heavily doped than the well, and the well is similarly more heavily doped than the epitaxial region beneath. The epitaxial layer is deeper and usually above a heavily doped P region. So the only ways to build P–N junctions are to immerse N^+ or N well into the P substrate or P^+ into an N well that is in the P substrate, as Fig. 4 shows.

To compare cells under equivalent constraints, all cells in Fig. 5 occupy 1 mm^2 of the same 0.35-µm single-well CMOS die, so the cost of each configuration is the same. Since the aim of this research is to design the highest power-generating configuration, comparing cells from the same technology is the most important consideration. Although power and cost vary with pitch, relative performance changes less because pitch affects all cells in similar ways. As a result, comparing power levels and power-conversion efficiencies to others in literature is less relevant, and less appropriate when doping concentrations, junction depths, and substrate thicknesses constitute proprietary information that is often unavailable.

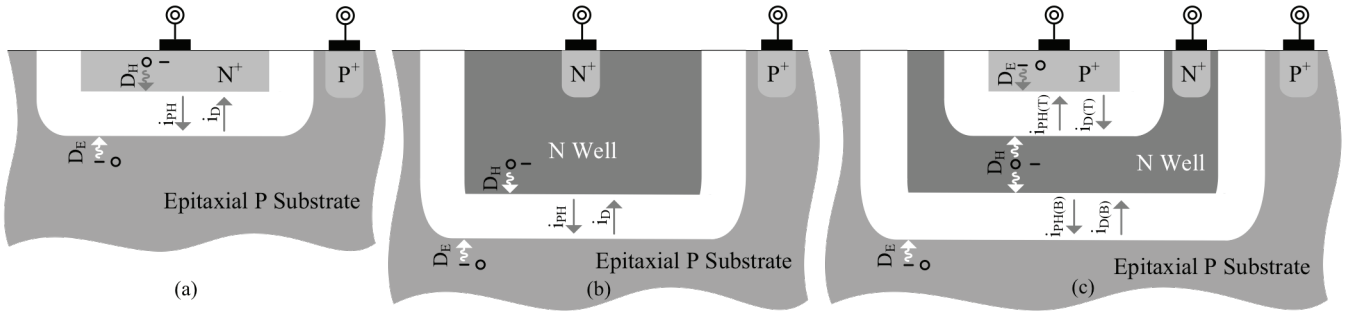

Fig. 4. Profile view of available PV P–N junctions in standard, low-cost CMOS process technologies.

A. Standard N+ in P Substrate Cells

Immersing N^+ into the P substrate like Fig. 4a shows creates a charge-collecting P–N junction. Since the doping concentration of N^+ is high and dopants are near the surface, donor atoms tend to fill surface irregularities. Minority charge carriers are therefore less likely to linger long enough to recombine. Higher majority-carrier concentration, however, also means minority holes recombine with majority electrons within a relatively short diffusion length L_H. So only a fraction of holes in the N^+ region reach the depletion space beneath. And although the region is near the surface, N^+ is also shallow, so light produces few EHPs.

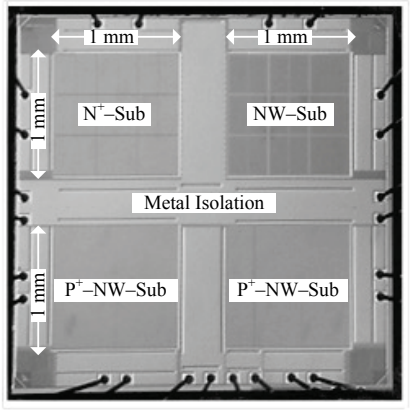

Fig. 5. Die photograph of the single-well CMOS PV cells fabricated.

The doping concentration of the substrate is lower, so the diffusion length of minority electrons is longer. Plus, the region is vast, which under equivalent light intensity, means more EHPs are likely to appear. But since light intensity falls exponentially with depth, EHPs are less prevalent. And since the cell can only collect EHPs within a diffusion length of the depletion space, farther-away EHPs ultimately recombine.

When subjecting a prototyped 1-mm^2 0.35-µm CMOS structure of this sort to 1 klx, 10 klx and 80 klx, the cell generated 0.2, 1.2 and 5.9 µW. At 80 klx, the equivalent of direct sunlight, the maximum power point was at 0.40 V and 15 µA, like Fig. 6 shows. Since photonic current i_{PH} was 16 µA (with zero volts), i_{PH} lost 1 µA to diode current i_D.

B. Standard N Well in P Substrate Cells

Immersing an N well into the P substrate like Fig. 4b shows also creates a charge-collecting P–N junction. Since the well's doping concentration is lower than that of N^+, the average diffusion distance L_H that minority holes traverse before recombining with majority electrons is longer, so more holes can reach the depletion space beneath. Plus, lower doping concentration means the junction is easier to deplete, so the depletion space is wider and therefore capable of collecting more EHPs. The junction, however, is farther away from the exposed surface, so EHP concentration is generally lower. And like before, only substrate EHPs within a diffusion length of the junction can reach the depletion space.

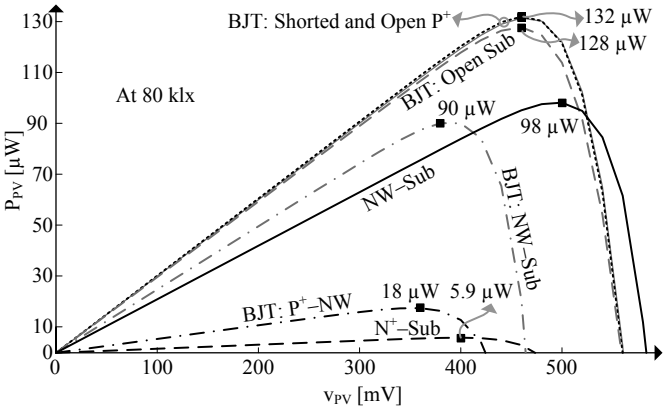

Fig. 6. Measured PV power across PV voltage at 80 klx.

When subjecting a 1-mm^2 0.35-µm CMOS structure of this sort to 1 klx, 10 klx and 80 klx, the cell generated 3.0, 20 and 98 µW. At 80 klx, the maximum power point in Fig. 6 was at 0.50 V and 196 µA. Since photonic current i_{PH} was 210 µA (with zero volts), i_{PH} lost 14 µA to diode current i_D.

C. P+ in N Well in P Substrate Cells

Interestingly, immersing P^+ in N well in a P substrate like Fig. 4c illustrates creates not only two P–N junctions: P^+–well and well–substrate, but also the P^+–N well–P substrate bipolar-junction transistor (BJT) in Fig. 7. As a PV cell, nearby P^+ and N-well EHPs reach the top P^+–well junction and nearby N-well and P-substrate EHPs reach the bottom well–substrate junction. So the well contributes to the photonic currents of both junctions, to $i_{PH(T)}$ and $i_{PH(B)}$ [12]–[14].

As with N^+, the doping concentration of P^+ is high, many dopants are near the surface, and the region is shallow, so surface recombination is low, minority diffusion length L_E is short, and light produces few EHPs. And although the lower well–substrate junction is farther away from the surface, longer diffusion lengths and a wider depletion region counter the effects of lower EHP concentration. Ultimately, the performance of this cell hinges on which photonic current the structure outputs and under what conditions.

Top Junction: Shorting the N well to the substrate with a metallic link steers bottom photonic current $i_{PH(B)}$ around a

zero-volt loop that keeps $i_{PH(B)}$ from producing power. So when subjecting a standard 1-mm^2 0.35-µm CMOS structure to 1 klx, 10 klx and 80 klx, the cell generated 0.4, 3.1 and 18 µW. At 80 klx, the maximum power point in Fig. 6 was at 0.36 V and 49 µA. Since top photonic current $i_{PH(T)}$ was 55 µA (with zero volts), $i_{PH(T)}$ lost 6 µA to top diode current $i_{D(T)}$.

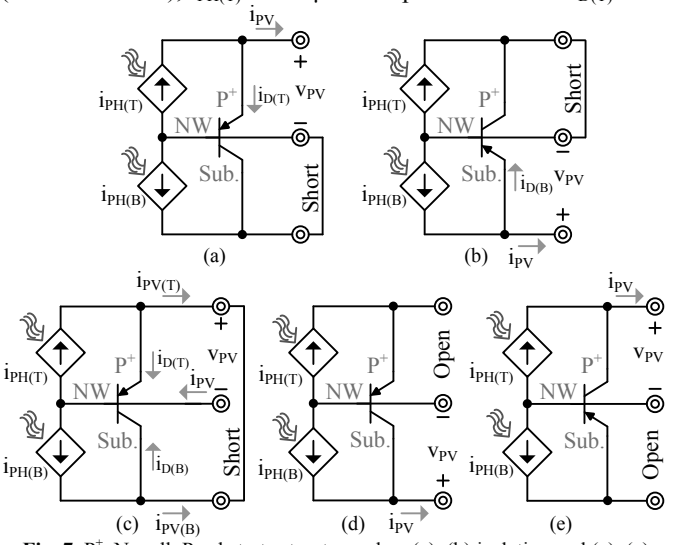

Fig. 7. P^+–N well–P substrate structure when (a)–(b) isolating and (c)–(e) combining top and bottom junctions with shorts and open terminals.

Bottom Junction: Shorting P^+ to the N well with a metallic link similarly steers top photonic current $i_{PH(T)}$ around a zero-volt loop that keeps $i_{PH(T)}$ from producing power. So when subjecting a standard 1-mm^2 0.35-µm CMOS structure to 1 klx, 10 klx and 80 klx, the cell generated 3.0, 20 and 91 µW. At 80 klx, the maximum power point in Fig. 6 was at 0.38 V and 239 µA. Since bottom photonic current $i_{PH(B)}$ was 250 µA (with zero volts), $i_{PH(B)}$ lost 11 µA to diode current $i_{D(B)}$.

Combined Junctions: With three terminals and two junctions, three cell configurations draw EHPs from both junctions. Shorting P^+ to P substrate is one way. When subjecting a standard 1-mm^2 0.35-µm CMOS structure to 1 klx, 10 klx and 80 klx, the cell generated 4.0, 28 and 132 µW. At 80 klx, the maximum power point in Fig. 6 was at 0.46 V and 286 µA. Since top and bottom zero-volt photonic currents $i_{PH(T)}$ and $i_{PH(B)}$ were 55 and 248, $i_{PH(T)}$ and $i_{PH(B)}$ lost 17 µA to diode currents $i_{D(T)}$ and $i_{D(B)}$. Of these, $i_{D(B)}$ was almost nil because the bottom junction is far weaker than the top.

Another way to combine EHPs from both junctions is to disconnect the P^+ terminal. This way, top photonic current $i_{PH(T)}$ has no other path than the diode, so $i_{PH(T)}$ flows back into the well as $i_{D(T)}$. Although some of $i_{D(T)}$ recombines in the well, the distance between the depletion regions is not long. So most of $i_{D(T)}$ reaches the bottom depletion space, whose field sweeps the incoming carriers to the substrate. $i_{PH(T)}$ therefore adds to the current that the bottom junction outputs. So when open-circuiting P^+ and exposing the cell to light, output power nearly matches that of the previous case.

Similarly, disconnecting the substrate circulates bottom photonic current $i_{PH(B)}$ through the bottom diode as $i_{D(B)}$ into the well. Although like before, some of $i_{D(B)}$ recombines in the well, much of $i_{D(B)}$ reaches the top junction. $i_{D(B)}$ therefore feeds the top junction, whose field then sweeps $i_{D(B)}$ along with top photonic current $i_{PH(T)}$ to combine their effect. So when open-circuiting the substrate and subjecting the unconventional structure to 1 klx, 10 klx and 80 klx, the cell generated almost as much power at 3.9, 27, and 128 µW like Table I reports. Output power was slightly lower because the bottom junction collects more current, and losing a fraction of this higher current to recombination in the well reduces output power further.

TABLE I. MEASURED POWER FROM SINGLE-WELL 0.35-µm CMOS CELLS

Single-Well PV Cells			$P_{PV(MPP)}$ [µW]		
			1 klx	10 klx	80 klx
N^+ in P Sub.			0.2	1.2	5.9
N Well in P Sub.			3.0	20	98
P^+ in N Well in P Sub.	Single Junction	P^+–N Well	0.4	3.1	18
		N Well–P Sub.	3.0	20	91
	Combined Junctions	Shorted	4.0	28	132
		Open P^+	4.0	28	132
		Open P Sub.	3.9	27	128

Experimental Validation: A 10-W, 12-V halogen bulb under a variable voltage produced the light levels used to test the cells and a LX1330B luxmeter measured the illuminance quoted. Voltages and currents from no less than ten repetitions of each experiment were within 10 mV and 1 µA of the values reported. Since all measurements were at room temperature and power levels were below 140 µW, the effects of duration on ambient and junction temperatures were minimal.

IV. COMPARISON

Power: Although not exactly the same, conventional N^+- and P^+-derived cells generated similar power. This is because their doping profiles are similar: both heavily doped and shallow. But because donor and acceptor atoms and the processing steps used to deposit them are not exactly alike, the P^+-derived PV cell produced 3× more power than the N^+ counterpart.

The cells that collected EHPs in the deeper well–substrate junction produced 5× to 7× more power. One reason for this is longer diffusion length, because further-away EHPs can reach the depletion space. A wider depletion region is another factor because, with more atoms available, light frees more EHPs.

The standard stand-alone well–substrate cell produced 8% higher power at 80 klx than the bottom junction of the P^+–well–substrate device. Why this was the case at 80 klx and not at 1 or 10 klx may be current density. Since the physical structures are not *exactly* alike, parasitic resistances are different. As a result, higher substrate currents drop voltages that accentuate the effects of these differences on the depletion fields that collect EHPs to generate power.

Combined junctions produced more power than their isolated counterparts combined. The 18 and 91 µW that the top and bottom junctions of the P^+–well–substrate structure produced, for example, when isolated and exposed to 80 klx add to 117 µW, 23 µW less than the 132 µW the combined structure produced. This is because the same diffusion current the stand-alone structures lose to the diode the combined structure feeds to the opposing junction. Although some of it recombines in the well, much of it reaches the other junction. In other words, opposing junctions recover diode power.

Of combined junctions, the open-terminal configurations proposed require less metal. Eliminating the need to connect one terminal removes top-surface metal that would otherwise block light. With less metal, the cell receives more light, and as a result, produces more collectable EHPs. Plus, with less metal constraints, open-circuiting and partitioning P^+ into islands extend the depletion space to the sides of the islands to collect more EHPs. The cells prototyped for these experiments, however, connect all terminals to pins, so they do not reap these advantages. So removing the metal that connects to P^+ or substrate in the P^+–well–substrate prototype would generate more power than Fig. 6 and Table I show.

Outside of doping concentrations and diffusion depths, other processing factors affecting output power are passivation and silicided surfaces. Since these sit above the semiconductor, they filter some of the incoming light to liberate less EHPs. Keeping these layers off the surface of a CMOS PV cell raise output power, but not without increasing series resistance and risking some reliability.

MPP: The maximum power points (MPP) in Fig. 6 for the well–substrate and N^+- and P^+-derived cells were 0.50, 0.40, and 0.36 V, respectively. The voltage of the well–substrate cell was higher because doping concentration is lower, and the corresponding diode is therefore weaker. As a result, diode losses balance photonic gains at higher PV voltages.

The maximum power points for the combined junctions were higher at 0.46 V than their constituent junctions at 0.36 and 0.38 V. This is probably because opposing junctions recover some diode power, so diode losses cancel photonic gains at a higher PV voltage. The maximum power point for the isolated well–substrate junction in the P^+–well–substrate structure was lower at 0.38 V than for the stand-alone counterpart at 0.50 V. Why this is the case is not clear.

Integration: CMOS circuits normally connect the P substrate to the most negative potential to isolate components, or more to the point, to keep substrate P–N junctions from forward biasing. Of available configurations, only the isolated P^+–well junction in the P^+–well–substrate structure connects the substrate to the most negative potential. So only this cell can share the substrate with integrated CMOS circuits, which is the second lowest power-producing configuration tested.

Thankfully, sharing the substrate is normally undesirable because a tiny PV cell captures a very small fraction of the incoming light. As a result, artificial and obstructed lighting generates power levels that are too low to be practicable. This is why increasing the surface area of the cell is so critical, and why dedicating one die for the cell and stacking it above the circuit captures more light and outputs more power than integrating the cell into the circuit. Plus, dedicating a single-well die saves money because coarse-pitched single-well area costs less than finer-pitched multi-well real estate. These winnings often outweigh the conduction losses and cost of 10–100 mΩ intra-die connections and multi-die packaging [15].

V. Conclusions

Since lower doping concentrations extend diffusion lengths and depletion regions, the prototyped 0.35-µm single-well CMOS N well–P substrate PV cell generates 5× more power at 91–98 µW than P^+ in N well at 18 µW when exposed to the equivalent of direct sunlight. Two-junction cells generate 7× more power at 128–132 µW than P^+ in N well and 31%–45% more power than N well in P substrate. The configuration proposed that opens the P^+ terminal to combine the shallower and deeper junctions eliminates top-surface metal from the structure, so more light can penetrate to generate even more power. Although using the substrate junction keeps the proposed structures from sharing the substrate with a CMOS circuit, sharing the substrate is normally undesirable. Since microsystems can only avail a few millimeters, dedicating one die to the PV cell and stacking it above the CMOS circuit produces much more power than placing the PV cell alongside the circuit, especially when drawing power from multiple junctions. Plus, using a coarser single-well CMOS cell costs less than its finer and multi-well counterparts.

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