A Feed-Forward 10× CMOS Current-Ripple Suppressor for Switching Power Supplies

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***Abstract*—With the advent of wireless micro-sensors and other micro-scale applications, switching supplies fully integrated on chip or into the package are desirable and often necessary. The problem with small inductors is that they exhibit low inductance and larger equivalent series resistance (ESR); in other words, they induce larger ripples in the output and higher conduction power losses. This paper presents and verifies a current-ripple suppression technique in which a discrete 2 × 2 × 1 mm^3 4.7µH inductor is effectively multiplied by subtracting a replica of the inductor's ac ripple current, allowing only a residual ripple to reach the output. Experimental results from a CMOS IC prototype demonstrate a current- and output-ripple reduction of 10.8× and 25.8×, respectively. The ESR power savings in the smaller inductor favorably offset the quiescent power lost in the multiplier (128mW), outperforming its higher non-multiplied 47µH counterpart at high loads (above 250mA).**

***Index Terms*—Active Filter, DC-DC Power Conversion, Inductor, Multiplier, Power Electronics, Switching Supply**

I. Integrated Inductors

Due to their versatility and efficiency, switched-inductor regulators are commonly featured in portable and stationary electronics. Unfortunately, the inductors are large and bulky when compared to other parts of the circuit. Their size cannot be reduced easily because the inherent switching action of these converters creates an undesirable output voltage ripple that is inversely proportional to the inductance. The buck converter in Fig. 1, for example, alternately connects v_{SW} to dc input supply V_{IN} and ground to produce a square voltage that L_O and C_O filter. Filtered v_O is therefore equivalent to v_{SW}'s average (dc portion) plus a small ripple Δv_O, whose ripple amplitude depends on L_O and C_O. A lower L_O, as a result, generates larger current and voltage ripples Δi_L and Δv_O:

$$\Delta i_L \approx \frac{V_{IN} d_{MP} d_{MP}'}{L_O f_{SW}} \quad \text{and} \quad \Delta v_O \approx \frac{V_{IN} d_{MP} d_{MP}'}{8 L_O C_O f_{SW}^2}, \quad \textbf{(1, 2)}$$

where d_{MP} is M_P's duty cycle, d_{MP}' is $1 - d_{MP}$, and Δi_L's effects on C_O's capacitance often overwhelm those of C_O's equivalent series resistance (ESR) [1]. Although integrating inductors would increase power density and facilitate ultra-portable micro-systems, the inductance required is large and difficult to include on chip or in the package.

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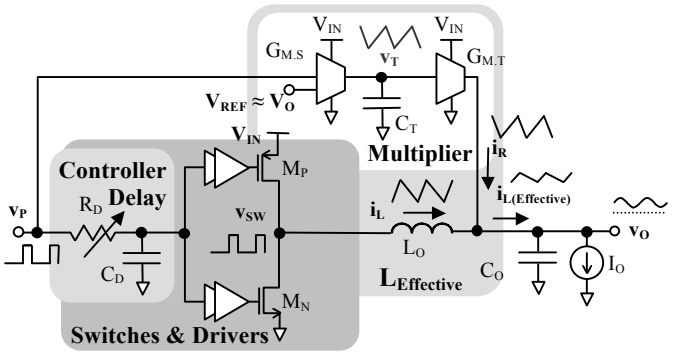

Fig. 1. Inductor-multiplied buck (R_D, L_O, and C_O are off chip).

Some techniques for reducing the required inductance have already been presented in literature (Section II), but not without their shortcomings. Section III therefore describes the proposed inductor-multiplying technique and an integrated CMOS embodiment. Section IV then documents the experimental performance of the prototype, Section V discusses the results, and Section VI draws relevant conclusions.

II. Reducing Required Inductance

The most straightforward means of reducing the inductance required is by increasing the switching frequency f_{SW} [2]-[6]. This approach, however, superimposes significant and often impractical tradeoffs in switching supplies, like the need for deep sub-micron technologies to limit parasitic switching losses [2]-[5] or high-voltage transistors to withstand the large oscillations in high-frequency resonant converters [6].

Without increasing frequency, inductor current ripple Δi_L can still be supressed, and there are a number of on-chip strategies involving additional active (power-consuming or lossy) filter circuitry. Adding a linear regulator between the switching regulator and the load, for instance, can suppress the ripple, if the ripple's frequency is within the regulator's bandwidth. Unfortunately, the output voltage has to be reduced (i.e., dropped or bucked) by at least the amplitude of the ripple Δv_{SUPPLY} (plus $V_{DS(sat)}$ of the series power device), which constitutes another conduction loss ($I_{LOAD}\Delta v_{SUPPLY}$).

Alternatively, the active circuitry can be added in parallel [7]-[12]. Such circuitry must generate a ripple current that complements Δi_L such that when the two currents combine at the output, output capacitor C_O only absorbs a small residue, producing, in theory, a negligibly small output ripple Δv_O, as if the inductance itself were larger [8]. Reducing the voltage across inductor L_O also suppresses Δi_L, but this requires additional voltage sources [8], [13]. Similarly, multiphase converters employ several simple converters in parallel that switch out of phase so that their respective inductor currents combine

and cancel, except the decrease in ripple varies greatly with duty cycle (and therefore, with load current), and each added phase requires its own inductor and power switches, whereas inductor multiplication suffers neither problem.

III. Proposed Inductor Multiplier

A. Feed-Forward Approach

A feedback-based inductor multiplier senses Δi_L and generates a current to cancel Δi_L. The delay of inverted replica current i_R, however, creates a current offset that limits current multiplication factor M_I, which represents the ratio of Δi_L to the current ripple that reaches C_O ($\Delta i_{L(eff)}$). For instance, M_I cannot exceed 12.5× when the delay is 1% of switching period T_{SW} [14].

Predicting Δi_L can eliminate the systematic delay associated with a feedback loop. To that end, just as L_O produces triangular ripple Δi_L by integrating its square voltage v_L (i.e., $\Delta i_L = \int v_L/L_O \, dt$), C_T in the proposed circuit (Fig. 1) produces a triangular voltage Δv_C that emulates Δi_L by injecting a proportionally equivalent square current i_C into C_T (i.e., $\Delta v_C = \int i_C / C_T \, dt = \int v_L G_{M.S}/C_T \, dt$). Because v_P is in phase with v_{SW} and swings from 0 to V_{IN}, just as v_{SW} does, and the converter regulates v_O to V_{REF}, the voltage that $G_{M.S}$ translates into i_C is roughly equivalent to v_L (i.e., $v_L \equiv v_{SW} - v_O \approx v_P - V_{REF}$). Therefore, converting Δv_C back to a current via transconductor $G_{M.T}$ produces the desired (and predicted) inductor-emulating replica current i_R (i.e., $i_R = \Delta v_C G_{M.T}$), as long as i_R's amplitude matches Δi_L's. The circuit ensures the amplitudes equal by tuning C_T, $G_{M.S}$, or $G_{M.T}$ to equate $C_T/(G_{M.S}G_{M.T})$ to L_O. Notice the circuit adjusts i_R automatically to changes in V_{IN} and V_O (as it does i_L) because v_P and V_{REF} emulate v_{SW} and V_O, where v_P and v_{SW} carry V_{IN}.

The tuning process requires trimming, calibration during startup and power-on-reset events, or an additional correcting low-bandwidth feedback loop to accommodate process variations in $G_{M.S}$, C_T, and L_O. In the prototype, the resistors that set $G_{M.T}$ were off chip and adjusted (trimmed) manually for testability and proof of concept. Employing negative feedback to continually tune the system, however, would also adjust for thermal and aging effects. Note the bandwidth of such a correcting loop need not be high because its response time would not affect the converter and its multiplier during load dumps.

B. Two-Stage IC Embodiment

Replica current i_R must reach v_O in time to cancel Δi_L so the transconductors must be fast. To ease their speed requirements, their switching input is derived from further back in the signal chain (i.e., with some lead time), from signal v_P instead of v_{SW} because v_P not only mimics (i.e., is in phase) but also precedes v_{SW} slightly. Additionally, $G_{M.S}$ must accommodate a rail-to-rail input common-mode range (ICMR) because v_P (as does v_{SW}) switches from ground to V_{IN}, and since $G_{M.T}$ generates i_R, $G_{M.T}$ must be efficient and able to source large currents (equivalent to Δi_L).

First Stage Transconductor $G_{M.S}$: Achieving rail-to-rail ICMR operation with a standard differential pair is not trivial, which is why $G_{M.S}$'s input stage (Fig. 2) is slightly different. In this case, unity-gain amplifier A_{UG} ensures the voltage across resistor R_i is $v_P - V_{REF}$, which as mentioned earlier, is the equivalent of $v_{SW} - v_O$, so $G_{M.S}$ reduces to $1/R_i$. In this way, the differential pair's input common-mode voltage is always at V_{REF}, which is considerably easier to accommodate, while allowing the overall circuit to sustain wide swings in v_P.

As v_P transitions from V_{IN} to zero, current through R_i and M_{NdA} changes from $(V_{IN} - V_{REF})/R_i$ to $-V_{REF}/R_i$, increasing in one direction and decreasing in the other. Complementary differential transistor M_{NdB} therefore changes by the same amount, but in the opposite direction. M_{PmA}-M_{PmC} then mirror M_{NdB}'s current to the output, where C_T integrates it. The square-wave voltage at v_P thus causes a square-wave current through R_i and a triangular voltage across C_T.

In practice, $G_{M.S}$'s average output current is not zero, and because v_T is a high-impedance node, v_T's average voltage drifts to V_{IN} or ground, which means mirror or bias-current transistors M_{PmC}-M_{PcC} or M_{NdC}-M_{NbE} are not saturated and distort v_T. A slow, low-gain feedback loop is consequently included to regulate the dc voltage of this node well within the supplies. In Fig. 2, differential pair M_{PdA}-M_{PdB} and current mirror M_{NlA}-M_{NlC} comprise that feedback loop, which regulates v_T to a fraction of V_{IN} at $V_{IN}R_{bB}/(R_{bB} + R_{bA})$, or in this case, $3V_{IN}/5$. This shunt-feedback loop also decreases the impedance at v_T, but only within its bandwidth (as set by filter R_f and C_f and enhanced by the Miller Effect through gain stage M_{NlB}-M_{NcA}-R_a), which is designed well below switching frequency f_{SW}. Maintaining the impedance high at f_{SW} is important to preserve v_T's

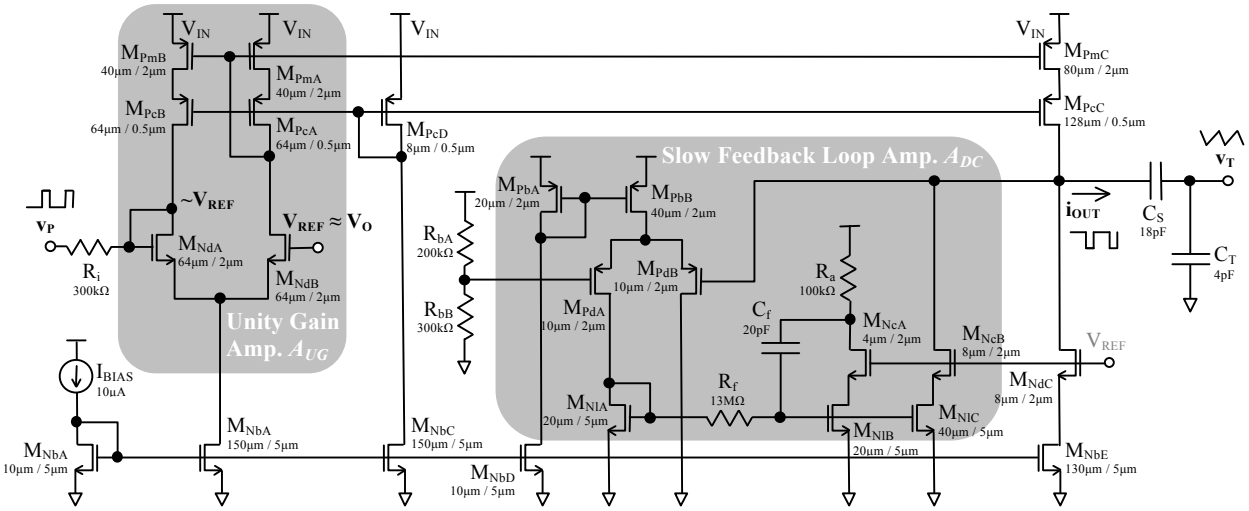

Fig. 2. Fully integrated (on-chip) first-stage transconductor $G_{M.S}$.

piecewise-linear shape. The prototype includes a series coupling capacitor C_s to allow v_T's average to be controlled externally, without affecting the operation of the transconductor.

Second-Stage Transconductor $G_{M.T}$: With amplifier A_1 in negative-feedback configuration (Fig. 3), $G_{M.T}$ superimposes triangular voltage v_T across R_1 so the resulting triangular current i_C flows through M_{NfB}. M_{NfB}-R_1 drives sourcing output transistor M_{PmB} via input mirror transistor M_{PmA}. Thus, R_1 ultimately sets transconductance $G_{M.T}$. Similarly, M_{NfC}-R_2, which mirrors M_{NfB}-R_1, drives sinking output transistor M_{NmB} via M_{NmC}. Note amplifiers A_{BUF1} and A_{BUF2} diode-connect (as unity-gain buffers) M_{PmA} and M_{NmC} to ensure they mirror M_{NfB} and M_{NfC}'s currents. They accelerate the response of the output mirrors by decoupling the large parasitic capacitances at the gates of M_{PmB} and M_{NmB} from the drains of M_{NfB} and M_{NfC}, which exhibit high resistance. M_{NmC} is necessary to sink the difference between I_{BIAS} and I_{R1} and keep the current source transistors in saturation during the phase of v_T when v_R/R_1 is less than I_{BIAS}.

Since $G_{M.T}$ only drives an ac output current (i.e., i_R equals $-\Delta i_L$), its average must equal zero, which means the circuit must cancel (subtract) the average current v_T's dc component V_T produces in M_{NfB} and M_{NfC}. M_{PbB} and M_{PbC} with M_{PbA}'s help accomplish this by sourcing M_{NfB}-M_{NfC}'s average current (i.e., M_{NfA}'s current) back into M_{NfB} and M_{NfC}. Notice M_{NfA}'s gate voltage is a low-pass filtered version of M_{NfB}-M_{NfC}'s so M_{NfA}-R_3 mirrors M_{NfB}-M_{NfC}'s average current. As a result, when M_{NfB} or M_{NfC}'s instantaneous current rises above its average, M_{PmA} sources or M_{NmA} sinks the difference between its instantaneous and average currents, half-wave rectifying M_{PmA} and M_{NmA}'s respective out-of-phase drain currents and removing the dc component V_T would otherwise produce in i_R. A dc offset here impacts both L_O's current i_L and power dissipation so the mirrors employ common-centroid geometries and include offset-reducing cascode transistors.

Integrated System: **Error! Reference source not found.**a presents the die photograph of the system, which includes $G_{M.S}$ and $G_{M.T}$, the complementary power switches of the buck converter, their respective drivers, dead-time logic, PTAT current-bias generator, various I/O buffers, and duplicates of individual blocks in the multiplier for testing purposes. While the entire die is 1.6 × 1.8 mm^2, the power switches use most of the total area. Because no single V_{IN}-to-V_{OUT} conversion ratio was more important, the switches were designed to introduce no more than 300mΩ and enlarged to exploit the die area available, which is why the aspect ratios of both n- and p-type transistors were 224mm/0.5µm. Resistors R_1, R_2, and R_3 in **Error! Reference source not found.**b, which determine transconductance $G_{M.T}$, are off chip and on the printed-circuit board (PCB) to increase testing flexibility. Three extra resistors are needed to bias $G_{M.T}$'s duplicate circuit so six resistors appear in total.

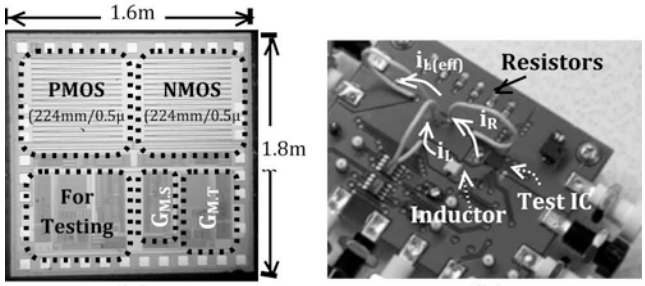

Fig. 3. (a) Die photograph and (b) PCB prototype.

The prototyped PCB (Fig. 1) includes a series RC delay block in the converter path to match i_L's total delay to i_R's because $G_{M.S}$ and $G_{M.T}$'s combined bandwidth slows i_R more than large power switches M_P and M_N delay i_L. This delay was adjusted manually in the experiments for testability and proof of concept but a low-bandwidth feedback loop could modify it automatically. Nevertheless, the ability to equate delays in any way (with a slow correcting loop, for instance) highlights a key advantage that results from a feed-forward derived i_R, because the delay of a feedback-derived i_R is uncorrectable. Similarly, R_1, R_2, and R_3 in $G_{M.T}$ (Fig. 3) adjusts i_R's amplitude to match i_L's, and again, a low-bandwidth feedback loop could tune them automatically so a calibration step during startup and power-on-reset events would be unnecessary. Incidentally,

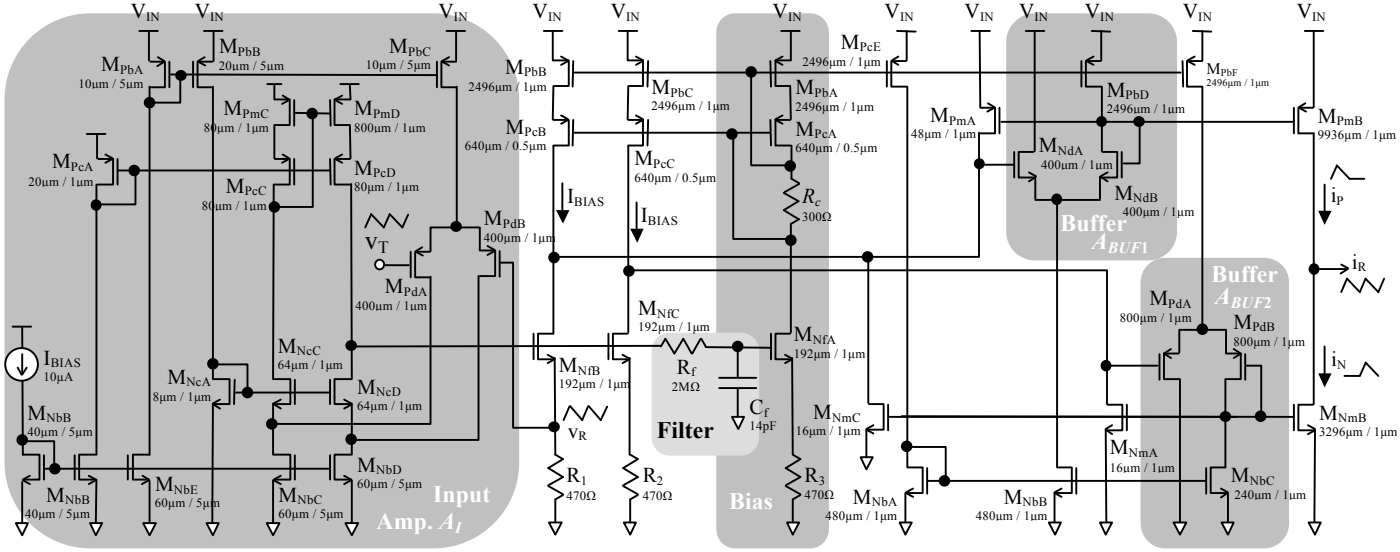

Fig. 3. Second-stage transconductor $G_{M.T}$ (R_1, R_2, and R_3 were off chip).

notice v_P in Fig. 1 is a good approximation of v_{SW}, except for the brief dead-time diode voltage drops in v_{SW} and the slight Ohmic drops across M_P and M_N when conducting i_L. These variations, however, constitute negligible errors in i_R, when compared against the residual delay and nonlinearity of i_R.

IV. Results

A. Inductor Multiplication

Although the technique is ultimately aimed at integrated inductors, the objective here is to test the viability and efficiency of CMOS inductor multiplication. Therefore, the system used a 2 × 2 × 1 mm^3 discrete 4.7µH inductor and a 16nF capacitor. Note higher capacitances are typical because C_O suppresses output ripple, but the proposed circuit relaxes that requirement because a smaller C_O achieves similar performance with the proposed multiplier. Also note L_O is nearly the size of the IC–as close to an integrated inductor as anything else readily available, except integrated inductors today are not as good. Without the multiplier, when f_{SW} is 1MHz, Δi_L and Δv_O were 216mA and 1.76V, and note Δv_O is so large that Eqs. (1) and (2) are no longer accurate. By contrast, when using a 47µH inductor, Δi_L and Δv_O were 18.6mA and 140mV.

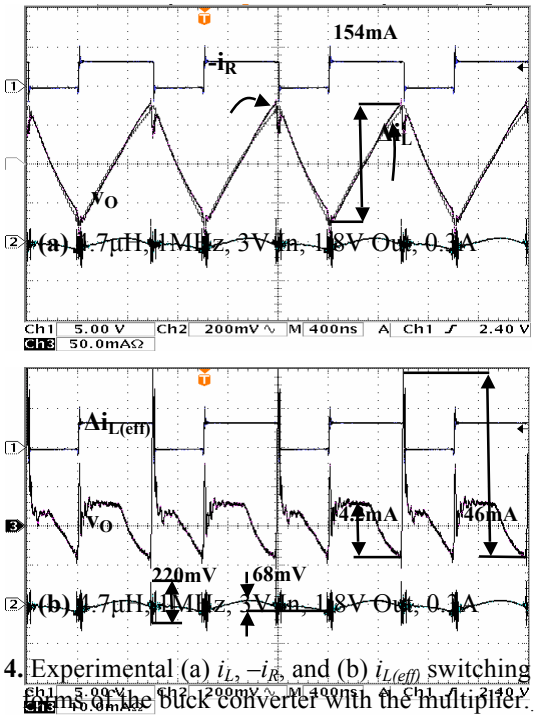

Fig. 4. Experimental (a) i_L, $-i_R$, and (b) $i_{L(eff)}$ switching waveforms of the buck converter with the multiplier.

Fig. 4a illustrates the experimental waveforms of the inductor-multiplied buck converter with 4.7µH when I_O is 0.3A. Note i_R is inverted and superimposed on i_L to illustrate how well they match. They are nearly perfectly in phase, and almost equal in amplitude. Fig. 4b shows the resulting $\Delta i_{L(eff)}$, which flows into C_O. Combined, the results are comparable with those of the converter with 47µH: $\Delta i_{L(eff)}$ is 14.2mA and Δv_O is 68mV. Current-mode multiplication factor M_I is therefore 10.8 (154mA/14.2mA), as also corroborated across a 0-830mA load range but not shown because of space constraints.

Notice the graph of $-i_R$, although close to i_L's, crosses i_L's more than once per period as a result of crossover distortion in $G_{M.T}$ so $\Delta i_{L(eff)}$, which only refers to $i_{L(eff)}$'s ac portion, similarly crosses zero multiple times, developing higher frequency components in $\Delta i_{L(eff)}$. Fortuitously, because C_O's impedance is lower at higher frequency, ripple Δv_O is lower than expected. As a result, voltage-mode inductor multiplication factor M_V was 25.8 (1.76V/68mV), higher than M_I. Note that if C_O's ESR R_{ESR} is high enough to overwhelm C_O's capacitive droop, Δv_O would be the Ohmic drop of $\Delta i_{L(eff)}$ across R_{ESR} (i.e., $\Delta v_O \approx \Delta i_{L(eff)} R_{ESR}$), so Δv_O would follow $\Delta i_{L(eff)}$ and M_V would equal M_I. Nonetheless, both metrics verify the proposed inductor multiplier outperforms a similar converter with ten times the inductance. Note the transient spikes in $\Delta i_{L(eff)}$ and Δv_O, which measure 46mA and 220mV, are the products of high-frequency noise in the PCB that loads are often able to filter.

B. Power Efficiency

The multiplier (i.e., $G_{M.S}$, C_T, and $G_{M.T}$) is an additional circuit that dissipates power, especially output power transistors M_{PmB} and M_{NmB} (in $G_{M.T}$ in Fig. 3) because they source and sink considerable current (i_R). The power lost in M_{PmB} and M_{NmB} is proportional to the voltage across them and the portion of i_R they conduct. The voltages across M_{PmB} and M_{NmB} are nearly constant in steady-state, and their respective Ohmic power losses $P_{C.PmB}$ and $P_{C.NmB}$ [15] are

$$P_{C.PmB} = (V_{IN} - V_O)\left(\frac{\Delta i_R}{8}\right) \quad \text{and} \quad P_{C.NmB} = V_O\left(\frac{\Delta i_R}{8}\right). \quad \textbf{(3, 4)}$$

In other words, most of the power lost in the multiplier is proportional to i_R, and by translation, Δi_L. Additionally, if i_R is offset by a small amount I_{OS}, the supply power will increase by approximately $0.5 V_{IN} I_{OS}$ (e.g. 16.5mW with 10mA I_{OS}), but power equal to $V_{IN} d_{MP} I_{OS}$ will be supplied to the output. The difference, which may be negative, is additional loss incurred by the multiplier circuitry, but if the duty cycle is near 0.5 then the difference is very small. Although these losses cannot be neglected, they do not increase with I_O, unlike switching and dc conduction losses P_{SW} and $P_{C.DC}$ in the converter [15]:

$$P_{SW} = \frac{I_O V_{IN} t_x f_{SW}}{4} \quad \text{and} \quad P_{C.DC} = (R_{SW} + R_{L.ESR}) I_O^2, \quad \textbf{(5, 6)}$$

where R_{SW} is the effective (total) switch resistance, $R_{L.ESR}$ is L_O's ESR, and t_x is the switch transition time. $P_{C.DC}$ is reduced slightly if I_{OS} is positive, increased if I_{OS} is negative, but this affects efficiency by less than 1% (Fig. 5a). All of this is to say efficiency degradation is less severe higher loads, because output power increases but multiplier losses do not (Fig. 5a: from 10% lower at 0.5A to 5% lower at 0.8A).

V. Discussion

Although the multiplier significantly reduces Δi_L and Δv_O, it does so at the expense of efficiency. In all fairness, however, while increasing L_O may achieve the same ripple attenuation, power efficiency may likewise decrease with higher L_O's because their ESRs are necessarily higher when constrained to the same volume. The 4.7µH inductor used, for example, has 280mΩ of ESR (roughly equivalent to the on-resistance of the switches) whereas the ESR of a 47µH inductor in a similar footprint is 2.18Ω. As a result (Fig. 5b), the efficiency of the

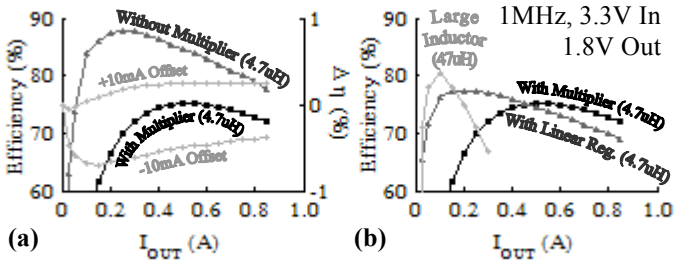

Fig. 5. Exp. eff. of (a) the multiplier and (b) other schemes. (Power lost in series device in linear regulator is simulated.)

same converter with the larger inductor decreases at a faster rate with respect to increasing I_O than its multiplied counterpart (because $P_{C.DC}$ increases with I_O^2 whereas multiplier losses remain constant). In this case, the multiplier is more efficient when I_O is greater than 250mA.

Inductor multiplication also compares favorably to adding a linear regulator in series with the converter. For a fair comparison, the series regulator must step down the incoming voltage enough to keep its pass device in saturation when the ripple is at its negative peak. As a result, the power lost across the series device depends on the converter's Δv_O, which varies with C_O. Typical linear regulators, for instance, require a step-down (dropout) voltage of at least 300mV ($V_{DS(sat)}$) so, at best, regulating the converter's output to 2.1V (1.8V + 300mV) to accommodate the series regulator produces a loss that increases linearly with I_O:

$$P_{C.MP(LDO)} = V_{DS(sat)} I_O . \quad \textbf{(7)}$$

The multiplier's loss remains unchanged as I_O increases, therefore the multiplier outperforms the regulator past 450mA. What is more, the linear regulator may not attenuate the ripple as much because its bandwidth, which determines power-supply rejection, does not typically extend far enough beyond the converter's f_{SW} to suppress noise. Nevertheless, since the multiplier is less efficient at light loads, sometimes a hybrid of the two techniques may be optimal. Applying this technique to integrated inductors, which exhibit lower inductances and higher ESRs, is possible but with either lower accuracy or reduced efficiency because of higher Δi_L and Δv_O.

Ultimately, a comparison with the state of the art should normalize the application, but that is almost impossible. Still, comparing the number and size of passives ($\#_{LC}$ and $L_O C_O$), and accuracy (Δv_O) to the proposed (with $\#_{LC}'$, L_O', C_O', and Δv_O) yields an informative figure of merit (FOM):

$$FOM = \left(\frac{L_O' C_O'}{L_O C_O}\right)\left(\frac{\Delta v_O'}{\Delta v_O}\right)\left(\frac{\#_{LC}'}{\#_{LC}}\right). \quad \textbf{(8)}$$

This FOM (Table 1) indicates the proposed circuit compares favorably with [7] and [11] and slightly unfavorably with [6], which relies on higher f_{SW} to keep $L_O C_O$ lower. However, [6] produces large oscillations at L_O's switching node.

Table 1. Design Specifications and FOM Comparison

	Proposed	**[6]Resonant**	**[7]Hybrid**	**[11]FF i_R**
V_O/V_{IN} f_{SW}	1.8V/3.3V 1MHz	7V/3.6V 30MHz	4V/9V 145kHz	5V/12V 67kHz
$\#_{LC}$ **L•C** Δv_O	2 4.7µH·16nF 3.8%	10 553nH·44nF 1.1%	2 17µH·20µF 0.2%	2 16µH·26µF 0.8%
FOM	**1**	**2.135**	**0.004**	**0.001**

VI. Conclusions

This paper proposed, presented, and experimentally verified a CMOS inductor current-ripple suppressor IC that reduced the current ripple of a discrete 2 × 2 × 1 mm^3 4.7µH inductor by a factor of 10.8 and the converter's output voltage ripple by a factor of 25.8. Although the added quiescent power losses to the converter degraded the overall efficiency by 5% at the peak load, a 10× larger inductor in the same package degraded the converter efficiency even more (as a result of a higher ESR). Similarly, as load current increases, the power dissipated across the pass device $M_{P(LDO)}$ of a linear regulator, when added in series with the existing converter, eventually becomes even larger than the constant losses that the multiplier prototype incurs. Therefore, current-ripple suppression can avoid the high-ESR losses associated with high inductances constrained to small volumes by multiplying the low inductances of integrated inductors without degrading the accuracy of the converter, albeit with lower light-load efficiency.

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