A Fast, Sigma–Delta (ΣΔ) Boost DC-DC Converter Tolerant to Wide LC Filter Variations

Neeraj A. Keskar, *Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Senior Member, IEEE*

Abstract: **Power supplies in portable electronics must adapt to their highly integrated environments and, more intrinsically, respond quickly to fast load dumps. However, frequency compensation must cater to the worst-case design LC combination, be it because of tolerance and/or variable design targets, limiting speed and regulation performance to the worst-case scenario, even under best-case conditions. ΣΔ control, which addresses this issue in buck converters, has not been able to *concurrently* achieve both high speed and wide LC compliance in boost converters. This paper presents a dual-loop ΣΔ boost converter whose prototype (5± 5%V, 1A) was 20% faster and at least nine times more LC compliant than its leading current-mode PWM counterpart, and this without a compensation circuit. Light load efficiency, intrinsic for battery life, was also better (2% higher at 0.5W, 600kHz) because of lower switching losses. The tradeoffs for these benefits were higher output ripple voltage (5V± 1.7%) and lower high load efficiency (less than 1.9% lower at 5W, 300kHz).**

Keywords: **LC filter compliance, ΣΔ boost converters.**

I. INTRODUCTION

In portable applications like cellular phones, laptops, and others, integrated switching DC-DC supply circuits reduce cost, size, component count, and design complexity. One of the critical bottlenecks in obtaining a fully integrated solution, however, is the frequency-compensation circuit, which for optimal performance, is designed around off-chip power LC filter devices [1]. An off-the-shelf DC-DC converter IC is exposed to wide LC filter variations because of various design requirements, manufacturing tolerances, and parameter drifts, leading to loop-gain variations and compromising transient response and stability. Hence, to guarantee stability and high bandwidth with a fixed on-chip frequency-compensation circuit, the LC filter values must be constrained within a narrow design range [1].

Unclocked ΣΔ buck converters [2-7] are self-compensating and free of the speed-stability tradeoffs of most DC-DC converters. Besides being stable in the classical sense due to hysteretic modulation, the control loop in these converters mimics current-mode control by indirectly sensing the inductor current ripple via the ripple voltage it drops across the capacitor ESR. The resulting single-pole response makes the voltage ripple controllable and extends bandwidth [5].

Extending this technique and its benefits to boost converters, which are popular in portable electronics for boosting battery voltages to 3.3 and 5V applications, is not straightforward because the inductor current does not fully flow to the output capacitor. This paper proposes a circuit and control scheme that overcomes this basic limitation by adopting two asynchronous (unclocked) ΣΔ loops, for output voltage and inductor current. To validate the scheme, Section II discusses the role of ΣΔ control in switching supplies and Section III presents the particulars of the proposed topology. Sections IV and V then show and discuss various experimental measurements, drawing relevant conclusions.

II. SIGMA-DELTA (ΣΔ) CONTROL

A. ΣΔ Basics

Qualitatively, the two summers in a ΣΔ-controlled negative-feedback loop (Fig. 1) [4] ensure (1) v_{OUT} is regulated to V_{REF} and (2) the average of v_U to R. Since the comparator output v_U can only swing between 0 and V_{PK}, the loop can only regulate the same range so:

$$0 < R < V_{PK}. \quad (1)$$

In [4], ΣΔ control is associated with sliding-mode control to show that a sliding plane exists at the surface v_{out} equals 0, provided R is within the above-specified range. As a result, any system controlled as in Fig. 1 is *always stable* and the average ac error integral v_{out} reaches zero and stays at zero (dv_{out}/dt is 0).

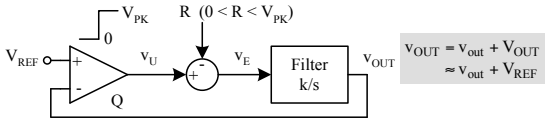

Fig. 1. Basic block diagram of a ΣΔ modulator.

B. ΣΔ in Buck Converters

In applying ΣΔ control to a buck converter (Fig. 2), output voltage v_{OUT} is fed to comparator Q, whose binary output sets the frequency and duty cycle of switch MPP1 (Fig. 2(a)). Operationally, inductor current ac ripple i_l flows into output capacitor C_O and its R_{ESR} (which is relatively large in these converters) [5-6] as i_c, forcing output ripple voltage v_{out} to mimic inductor ripple current i_l (i.e., $v_o \approx v_{ESR} = i_l \cdot R_{ESR}$). As a result, the inductor's ac current is also regulated, simplifying the control to a single-pole-like response (at high frequencies, due to the ESR zero), as in current-mode control, which

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The authors are with the School of Electrical and Computer Engineering and Georgia Tech Analog, Power, and Energy ICs Lab at the Georgia Institute of Technology, Atlanta, GA 30332, USA. (email: nkeskar@ece.gatech.edu, rincon-mora@ece.gatech.edu).

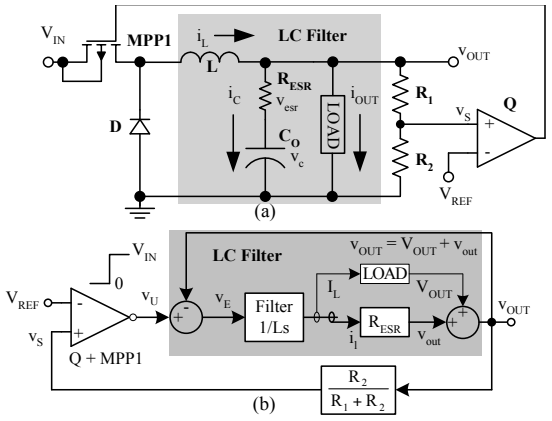

Fig. 2. ΣΔ Buck converter (a) circuit and (b) high-frequency block diagram.

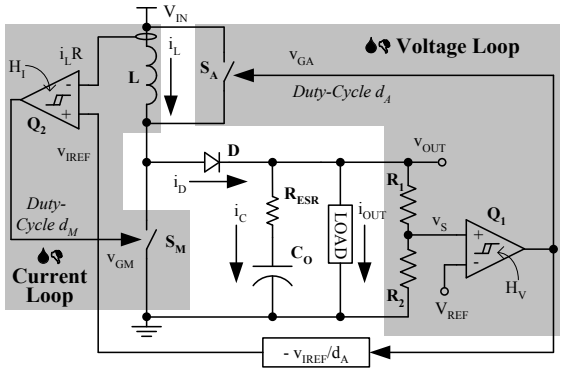

Fig. 3. Proposed ΣΔ-boost converter circuit.

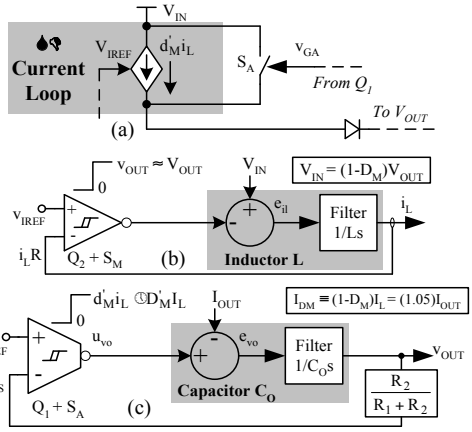

Fig. 4. (a) Equivalent low-frequency circuit and its corresponding (b) current and (c) voltage ΣΔ-loop models.

guarantees stability, irrespective of LC values.

When rearranged (Fig. 2(b)), the buck converter simplifies to a basic first-order ΣΔ loop (Fig. 1) at high frequencies. Inductor L adds the second summer and the 1/Ls filter to the loop with R equal to V_{OUT} (dc value of v_{OUT}), since ripple v_{out} is negligible as compared to V_{OUT}. Thus, since the output of a buck converter is always less than V_{IN}, R (i.e., target V_{OUT}) is constrained within (0 and V_{IN}), satisfying inequality (1).

C. *ΣΔ in Boost Converters*

In boost converters, since the output capacitor is disconnected from the filter inductor when the latter is energized, inductor ripple current i_l is not fully reflected in v_{out}. Hence, v_{OUT} cannot be used as an independent ΣΔ variable [8]. For inherent stability, as in ΣΔ buck converters, sliding-mode controllers sense and combine scaled errors in state variables i_L and v_{OUT} to generate a new composite variable that is regulated by a single ΣΔ loop [8-10]. The two state variables being necessarily coupled, the bandwidth of one is limited by the other. Although widely LC-compliant, this approach limits the transient response (i.e., bandwidth) to the response of the slowest loop, be it i_L or v_{OUT} [11].

With the proposed strategy, unlike conventional sliding-mode controllers, state variables i_L and v_{OUT} are decoupled via two independent ΣΔ control loops, uncorrelating their bandwidths and allowing i_L to respond quickly to transient load-dump events without significantly affecting v_{OUT}. Consequently, stability is achieved for a wide LC range without sacrificing transient-response performance.

III. CIRCUIT

A. *Operation*

To achieve the LC compliance desired with no compensation circuit, v_{OUT} and i_L are sensed and controlled separately. i_L is regulated with main switch S_M (Fig. 3) in a higher bandwidth loop to produce a current that is 5% more than necessary to support i_{OUT}. As a result, the inductor acts like a current source at lower frequencies (Fig. 4(a)). The lower-bandwidth voltage loop that regulates v_{OUT}, switches auxiliary switch S_A to bypass the 5% excess current from the inductor-current-source and supply the load with only the current required. In the ΣΔ-loop models (Figs. 4(b) and 4(c)), the comparator-switch combination (Q_2-S_M or Q_1-S_A) is represented by an equivalent comparator, which in the case of the voltage loop is a transconductor, whose output (diode current i_D) is zero when switch S_A is turned on. In comparing Fig. 4 with Fig. 1, the current and voltage ΣΔ loops are observed to be stable because their corresponding "R" values (i.e., V_{IN} and I_{OUT}, respectively) lie within (0 and V_{OUT}) and (0 and $D'_M I_L$), where $D'_M = (1-D_M)$, satisfying inequality (1).

B. *Duty-Cycle-to-Voltage Demodulator (v_{IREF}/d_A)*

Inductor current reference v_{IREF} is derived from the voltage loop with a duty-cycle-to-voltage demodulator (Fig. 5) such that the regulated inductor current is 5% higher than that necessary to support the load current, i.e., d_A is 5%. C_1 is charged and discharged by complementary switching current sources I_1 and I_2 and synchronized to duty cycle d_A. Steady state is achieved when the charge injected into C_1 by I_1 during S_A's off time equals the charge removed by I_2 during S_A's on time. Because I_2 is 19 times larger than I_1, v_{IREF} reaches steady state when S_A's off time is 19 times greater than S_A's on time, that is, when d_A is 5%.

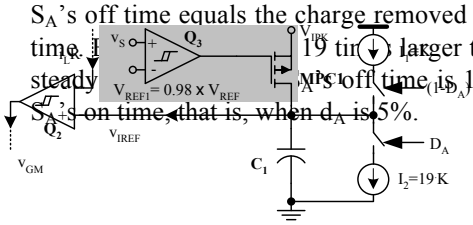

Fig. 5. Charge-based duty-cycle-to-voltage demodulator.

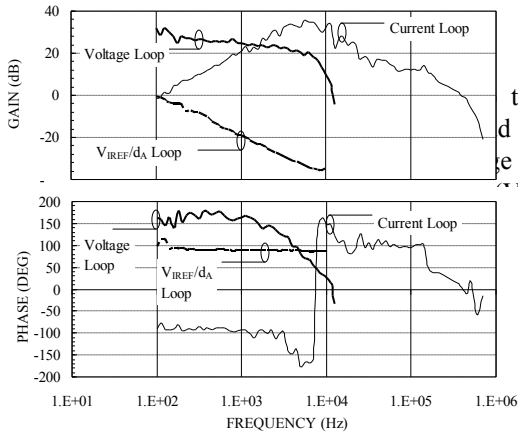

Fig. 6. Experimental Bode plots for the proposed converter.

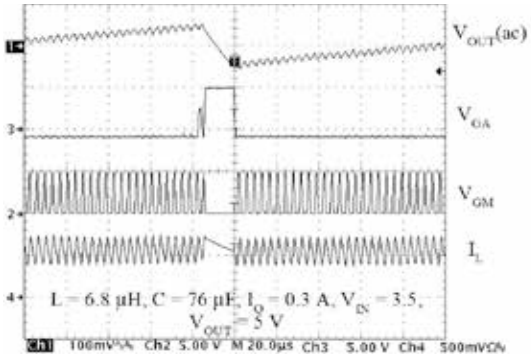

Fig. 7. Measured steady-state waveforms for the ΣΔ converter.

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C. *ΣΔ Loop Gain*

The unity-gain bandwidths of both self-oscillating, ΣΔ-control loops (Fig. 6) are at their respective switching frequencies, with zero phase margin [7, 12]. The resulting output (Fig. 7) is therefore the high-frequency (400kHz), low-voltage ripple ($30mV_{p-p}$) generated by the current loop riding on the lower frequency (12kHz), higher voltage ripple ($170mV_{p-p}$ or ±1.7% of V_{OUT}) generated by the voltage loop. To act as a stable reference for the current loop, the bandwidth of the duty-cycle demodulator (100Hz) that filters S_A's gate signal must be less than S_A's switching frequency.

In general, the switching frequencies of both the control loops vary with the slopes of the regulated current or voltage ripples, which depend on V_{IN} and/or I_{OUT}. Specifically, the rising and falling slopes of the current ripple vary in opposite directions with increasing V_{IN}; hence, the S_M's switching frequency exhibits a parabolic variation that peaks when the slopes are equal in magnitude – 50% duty cycle. In the voltage loop, the rising/falling slopes and the switching frequency increase with I_{OUT}. Solutions to switching frequency variations including variable hysteresis [2], variable delay [13], dither [14] etc., are found in literature.

The ripple performance above is on par with commercial ICs, e.g., [15], employing burst-mode or similar techniques in applications with similar ripple requirements. However, burst-mode control, which charges the inductor and discharges it to the load, involves high peak-to-average inductor current ratios, limiting its usage to low load currents. In the proposed technique, inductor discontinuous-conduction (as in burst-mode) is emulated by shorting the switch S_A. Therefore, unlike burst-mode where the excess inductor energy has to flow to the load, curbing the allowable excess energy, here the difference between the peak and desired-average inductor currents is diverted through S_A thereby maintaining output regulation. This feature not only improves the transient response by sustaining a higher peak-to-desired-average current ratio during transients, but it also allows operation at higher load currents.

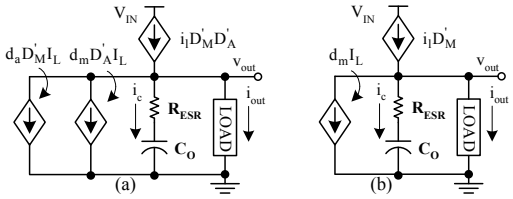

Fig. 8. Averaged and linearized models of (a) proposed and (b) conventional boost converters.

D. *Small-Signal and Steady-State Analyses*

The voltage loop senses v_{OUT} and modulates duty-cycle d_A to ensure that only the demanded load current flows through the diode to the output, and the rest of the inductor current freewheels. Hence, the diode current is

$$i_D = (1 - d_A)(1 - d_M) i_L = i_c + i_{OUT}. \quad (2)$$

For ac analysis, Eq. (2) can be written in terms of its dc and ac components:

$$I_D + i_d = (D'_A - d_a)(D'_M - d_m)(I_L + i_l) = I_{OUT} + i_c + i_{out}, \quad (3)$$

and linearized against small-signal stimuli:

$$i_d = -d_a D'_M I_L - d_m D'_A I_L + i_l D'_M D'_A, \quad (4)$$

to define the small-signal equivalent circuit model shown in Fig. 8(a) that simplifies to Fig. 8(b) in standard boost converters, where S_A is absent (i.e., d_A is 0). Therefore, in traditional boost converters, any small-signal variation (e.g., change in i_{out}) requires a corresponding change in inductor current i_L to meet the new load requirement. This change in i_L is brought about by a change in d_M, which also introduces an out-of-phase feed-forward path to the output, creating a right-hand plane (RHP) zero. On the other hand, a similar load change in the proposed converter is met simply by modulating auxiliary duty-cycle d_A, keeping d_M and i_L virtually unchanged and eliminating the RHP zero effect.

As to steady state, the dc equivalent of Eq. (2) gives

$$I_L = \frac{I_D}{(1 - D_M)(1 - D_A)} = \frac{I_{OUT}}{(1 - D_M)(1 - D_A)} = \frac{I_{L(MIN)}}{(1 - D_A)}. \quad (5)$$

where $I_{L(MIN)}$ is the minimum I_L, as in a standard boost converter when D_A reduces to zero in Eq. (5). In the proposed circuit, D_A is set to 5%, increasing the average inductor current by approximately 5%.

ΣΔ control of v_{OUT} requires i_L be regulated throughout the voltage loop bandwidth to ensure the inductor acts like a current source, i.e., the current loop's bandwidth (switching frequency) must exceed that of the voltage loop. This requirement implies a minimum output capacitance (C_{MIN}) for stability, for an inductor [16]:

$$C_O \geq \left(\frac{H_I}{H_V}\right)\left(\frac{I_{OUT}L}{V_{OUT}R_S(D'_M)}\right)\left(\frac{R_1+R_2}{R_2}\right) = C_{MIN}, \qquad (6)$$

where R_S is the current-sense resistor, and H_V and H_I are the hysteresis windows of Q_1 and Q_2, respectively, which can be designed for either a desired C_{MIN}, or for current and voltage loop bandwidths (switch frequencies).

The dc switch-conduction power loss, easily seen to be

$$P_{DC} = I_L^2\left(RD'_A + R_{ONSA}D_A\right) = \frac{I_{L(MIN)}^2 R}{D'_A}\left(1 + \frac{R_{ONSA}}{R}\frac{D_A}{D'_A}\right), \qquad (7)$$

where R_{ONSA} and $R=R_{ONSM} \approx R_{ONSD}$ are the on-resistances of switches S_A and S_M, S_D respectively, is clearly higher than that in a conventional boost converter ($I^2_{L(MIN)}R$), and hence is kept small by designing D_A at 5%. In an IC implementation, the switch S_A can be reduced to a fraction of S_M, to save die area and cost, so long as S_A's on-state voltage drop is small compared to (V_{OUT}-V_{IN}), i.e., S_A acts as a short. The increased power loss due to a higher R_{ONSA} can be partially compensated by reducing D_A to less than 5%. Additional energy loss is also incurred in switch S_A during a transient while the inductor current settles from its peak to its steady-state value (section III(B)); however, load/line transients are typically infrequent events and the impact on overall power efficiency is considered negligible.

IV. EXPERIMENTAL RESULTS

A prototype printed-circuit board (PCB) of the proposed solution was built and evaluated to validate and quantify its operational limits and compare its performance against a reference boost converter built using the LM3488 peak-current-mode controller [17] with internal ramp compensation. The feedback compensation of the reference controller is realized with an external series R_C-C_C circuit connected to the output pin of the internal error amplifier. In this design, for simplicity, current sensing is achieved by a sense resistor, but the reader is encouraged to consider lower power alternatives [18]. Table 1 provides a summary of the important parameters of the experimental setup.

TABLE I. Summary of parameters used in measurements.

Parameter	Value	Parameter	Value
V_{IN}	3.5V	V_{OUT}	5V
L	3.9-15μH	C_O	3.3-250μF
R_{ESR}	30-110mΩ	f_{OUT}	0.5-1MHz
R_{ONSD}	22mΩ	R_{ONSM}	58mΩ
R_S	50mΩ	R_{ONSA}	44mΩ
Q_2 Hyst.	400mV	Q_1 Hyst.	80mV
C_1 (Fig. 5)	0.6pF	V_{OUT} to M	0.5
I_1 (Fig. 5)	50μA	I_2 (Fig. 5)	0.8mA

A. LC Compliance

The reference circuit is designed with an R_C-C_C compensation of 7.5kΩ and 47nF to yield a maximum bandwidth of 25kHz and phase margin (PM) of 72° with LC filter values of 3.9μH and 90μF. Then, with R_C-C_C values unchanged, LC values were varied until stable operation limits (10° PM) were reached. The worst-case stability condition was observed to be at the highest load, when the RHP zero is at its lowest frequency point [17].

The same stability-testing procedure was repeated for the proposed ΣΔ converter. Its stability limit was reached when the current- and voltage-loop bandwidths were near one another (L no longer was a current source for the voltage loop). The smallest acceptable value of C_O was determined at the highest load, as predicted by (6).

The resulting regions of stability are described by the $R_{ESR}LC$ "stability-space volume" enclosures of Fig. 9, which show that the proposed approach encloses about an order of magnitude more $R_{ESR}LC$ *volume* than the reference circuit, indicating significantly greater LC compliance. At L and R_{ESR} of 6.8μH and 30mΩ, the minimum output capacitance was roughly 50μF for the reference boost converter, which was more than 10 times the corresponding minimum value for the proposed ΣΔ converter (4.5μF). With increasing R_{ESR} values (110mΩ), however, an increase in the resistive component of the v_{OUT} ripple has to be offset by increasing the minimum C_O to 5.5μF to decrease the capacitive ripple component in the proposed converter. On the other hand, the LHP zero of the reference boost converter shifts to lower frequencies at higher R_{ESR} values, decreasing the required minimum capacitor value to 45μF. Nonetheless, the stability volume of the proposed circuit remains about an order of magnitude better.

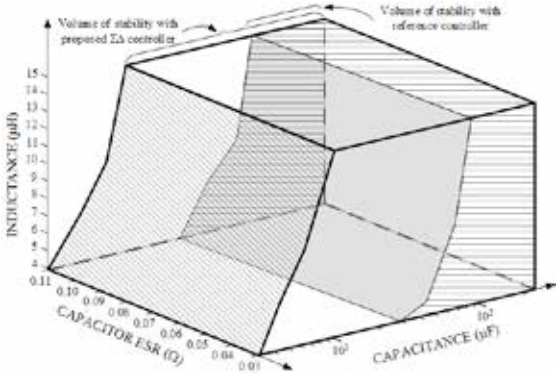

Fig. 9. 3-D contour curves of stability for the proposed and reference boost converter circuits under various L, C, and R_{ESR} conditions.

B. Transient Response

The step response for a single 0.1-1A load-pulse event (Fig. 10) shows that the reference circuit, which is limited by its loop bandwidth, suffers a larger voltage droop of 292mV (with a response time of 400μs). The proposed ΣΔ regulator's response, only limited by the inductor's current slew rate (which is allowed to slew until it reaches 2.8A, as determined by V_{IPK} in Fig. 5), produces a sag of 230mV (with a response time of 50μs). Note that the compensation circuit for the reference converter was designed for specific LC values to

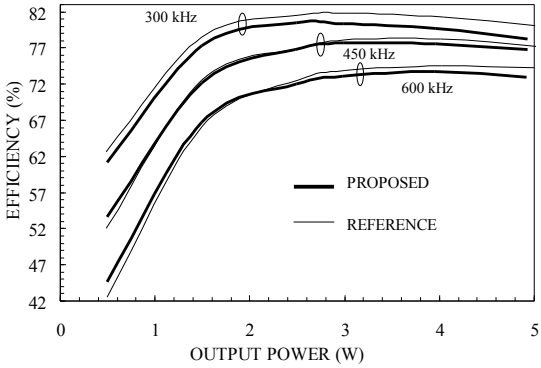

Fig. 11. Experimentally measured performance of the proposed converter and reference converters, both at 300, 450, and 600kHz.

ı-optimal, generic response.

of the proposed % lower at 5W, rter (at the same sses. However, as l below 2.5W, the efficiency of the proposed converter improves and even outperforms (2% better under 0.5W, 600kHz) that of the reference because switching losses dominate at lighter loads. During S_A's on time, S_M and S_D are off for several switching cycles, eliminating their switching/gate-drive losses, thus improving low-load efficiency as in burst-mode [15].

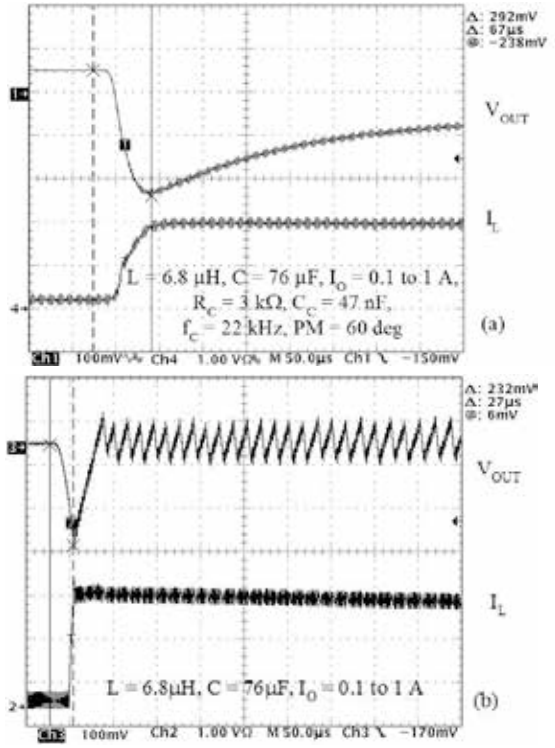

Fig. 10. Transient response to a 0.1-1A load step for the (a) reference and (b) proposed ΣΔ-boost converter.

V. CONCLUSION

The proposed dual ΣΔ-loop boost converter has 10 times better $R_{ESR}LC$ compliance and about 20% better transient response than the reference by independently regulating the inductor current and output voltage with two ΣΔ loops, in the process eliminating the RHP zero of traditional boost converters. The tradeoff is slightly higher conduction losses, which are offset at higher switching frequencies and lighter loads by lower switching losses. The other drawback is slightly larger steady-state output ripple voltage (5V± 1.7%), but it is still well within typical specifications limits (5V± 5%). In all, the proposed ΣΔ-boost converter is close to concurrently achieving "unconditional stability" and "high bandwidth," all without additional frequency-compensation circuits, which is optimal for user-friendly, small form-factor, and low-cost portable applications.

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